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Flexible thin-film transistors using multistep UV nanoimprint lithography

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ABSTRACT

A multistep imprinting process is presented for the fabrication of a bottom-contact, bottom-gate thin-film transistor (TFT) on poly(ethylene naphthalate) (PEN) foil by patterning all layers of the metal–insulator–metal stack by UV nanoimprint lithography (UV NIL). The flexible TFTs were fabricated on a planarization layer, patterned in a novel way by UV NIL, on a foil reversibly glued to a Si carrier. This planarization step enhances the dimensional stability and flatness of the foil and thus results in a thinner and more homogeneous residual layer. The fabricated TFTs have been electrically characterized as demonstrators of the here developed fully UV NIL-based patterning process on PEN foil, and compared to TFTs made on Si with the same process. TFTs with channel lengths from 5 μm down to 250 nm have been fabricated on Si and PEN foil, showing channel length-dependent charge carrier mobilities, μ, in the range of 0.06–0.92 $cm^2\,V^{-1}\,s^{-1}$ on Si and of 0.16–0.56 $cm^2\,V^{-1}\,s^{-1}$ on PEN foil.

1. Introduction

In a world following the ever demanding decrease of feature sizes for the fabrication of faster electronic circuits and devices according to Moore's law [1], research and development of tools allowing reproducible patterning at an ever decreasing scale gain increasing attention. On the other hand, electronics manufacturers focus on reducing fabrication costs and addition of device functionalities. Of great interest in this direction are organic plastic electronics, allowing potentially low-cost fabrication, in combination with the introduction of light-weight, flexibility and transparency, in high throughput roll-to-roll (R2R) or roll-to-plate [2] manufacturing lines. Transparent, bendable and even rollable flexible electronic devices such as organic light-emitting diode (OLED)-based displays [3], radio-frequency identification (RFID) tags [4,5], and organic solar cells (OSCs) [6] are being pursued. However, flexible electronic devices face new challenges, not necessarily originating from the small dimensions of the device, but from deformations and the dimensional instability of the substrate [7].

In combination with R2R manufacturing for low-cost fabrication of plastic electronics, the high-resolution [8,9] patterning technique nanoimprint lithography (NIL) is an excellent candidate. The classical thermal NIL [10–12] has been further developed into UV-based NIL [13], and as repetitive technique into step-and stamp [14] and step-and-flash imprint lithography (SFIL) [15], allowing better control over the residual layer thickness and throughput, by crosslinking a low-viscosity resist by UV irradiation through a fused silica template. Flexible organic thin-film transistors (OTFTs) have been fabricated by photolithographic patterning [7,16–18], stamping methods [19] and inkjet printing [20–23], all showing different advantages and disadvantages regarding layer registration, process temperature, feature sizes and device performance [20,24,25]. With conventional printing techniques, typical

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channel lengths on the order of 10 μm are obtained, limiting the bandwidth to 10 kHz for printable semiconductors with typical mobilities of 0.01 $cm^2 V^{-1} s^{-1}$ [26]. Fast, submicron transistors are, other than with conventional patterning techniques such as photolithography, readily available by NIL, being an intrinsically sub-micron and truly nanometer patterning technique.

In literature, TFTs have been reported with source–drain features patterned by UV NIL on flexible foil in a common gate architecture [27] and on glass with a photolithographically defined gate [28]. TFTs with the source–drain features patterned by thermal NIL and a photolithographically defined gate have also been reported [29]. Common gate TFTs cannot be addressed individually and suffer from parasitic effects (capacitances, resistances, inductances). Multilayered, patterned gate TFTs on the other hand, can be addressed individually in an array and show an improved performance. Fabricating a multilayer electronic device requires a good layer registration and overlay accuracy. Patterning on flexible and wavy foils, showing in-plane instabilities and a high sensitivity to thermal as well as pressure changes, remains a big challenge. With the low-cost and sub-micron patterning technique UV NIL, precise nano- to sub-micron alignment are just as important as critical control over the residual layer thickness (RLT) for the performance of a layer-by-layer fabricated, complex electronic device such as a bottom-contact, bottom-gate TFT. To our knowledge, a fully UV NIL-patterned TFT on foil has not been reported to date.

Here we report a method for fabricating bottom-contact, bottom-gate TFTs on Si and on flexible PEN foil with all functional layers patterned with the fast and low-cost patterning strategy SFIL. The complexity of the device layout is strongly increased with respect to the earlier reported flexible, common-gate TFTs [27] in which only the source–drain layer was patterned by SFIL. In this multilayered device the gate, source–drain and gate via are patterned by SFIL, showing a good layer definition and registration accuracy, even on the dimensionally instable, flexible PEN foils. The flexible TFTs were fabricated with the foil reversibly glued to a carrier (foil-on-carrier; FOC), enhancing the dimensional stability and flatness of the foil to result in a thinner and more homogeneously distributed RLT. An even further improved control over the residual layer was required to transfer all imprinted features of each device layer (gate, contact hole, source–drain) into the underlying functional material (metal, dielectric, metal). The here targeted solution of field-by-field planarization creates for every imprint an individual and flat plateau, ensuring complete removal of the residual layer. The transfer and output characteristics of the here fabricated TFTs on foil will be compared with TFTs fabricated on Si with the identical, fully SFIL-based process.

2. Results and discussion

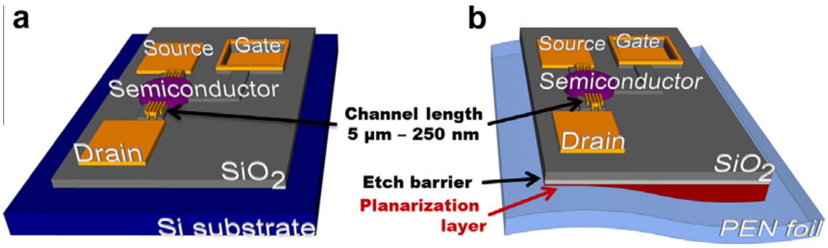
2.1. Design and process scheme

Scheme 1 shows a schematic three-dimensional view of the here fabricated TFTs on Si and foil in a bottom-contact, bottom-gate architecture. The gate, source–drain and contact hole features are patterned by SFIL, while the semiconductor is deposited by inkjet printing. In case of patterning on foil, also the planarization layer is patterned by SFIL. The 200 × 200 μm^2 contact pads of the source and drain are connected to three or two 5-μm wide interdigitated fingers separated by a space of 5 μm down to 250 nm, representing the channel length.

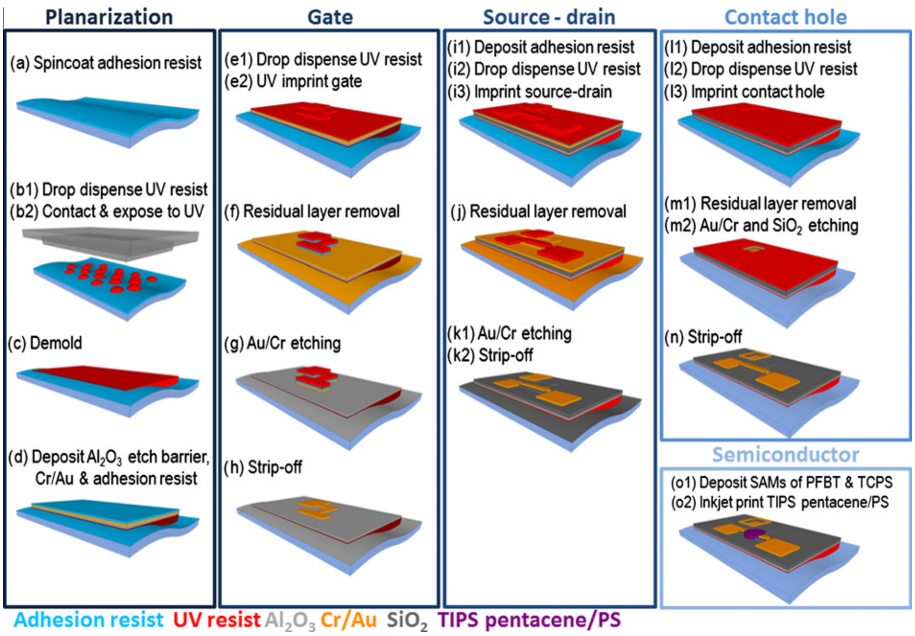
Scheme 2 shows the here developed multistep UV imprinting process on PEN foil, with a TFT on flexible foil as the resulting demonstrator. The process scheme for the TFT on Si is the same, except for the planarization layer. For better understanding, the carrier to which the foil has been reversibly glued is not drawn in the scheme. In the first step, the planarization layer is formed on the wavy PEN foil. The UV resist is drop dispensed on adhesion resist-coated (DUV30 J) PEN, followed by contacting with a UV transparent, non-patterned template (Scheme 2b). After UV exposure, the template is demolded and a planarized plateau of 25 × 25 mm^2 remains (Scheme 2c). An alumina etch barrier, Cr and Au for the gate layer, and adhesion resist DUV30 J are subsequently deposited (Scheme 2d). To pattern the gate, the UV resist is drop dispensed on the adhesion resist (Scheme 2e1) followed by contacting with the gate template. After UV exposure, an inverse replica of the gate template features remain on the foil (Scheme 2e2). The residual layer is removed by oxygen-based anisotropic reactive ion etching (O_2 RIE) (Scheme 2f), and unprotected Au and Cr are removed by ion beam etching (IBE) (Scheme 2g). The remaining resist is stripped off in O_2 RIE, leaving the patterned gate on the substrate (Scheme 2h). The source–drain layer is patterned in a similar fashion. First, the dielectric (150 nm SiO_2), Cr and Au for the source–drain layer, and adhesion resist are deposited. The source–drain features are patterned by exposure of drop dispensed UV resist with the source–drain template aligned to the previously deposited gate layer (Scheme 2i1–3). Residual layer removal (Scheme 2j) is followed by IBE and resist strip-off, resulting in a patterned source–drain layer (Scheme 2k). Contact holes are made through the dielectric by imprinting the contact hole features in UV resist, with the contact-hole template aligned to the previously patterned gate layer (Scheme 2l). Residual layer removal and IBE of deposited Au, Cr and SiO_2 (Scheme 2m) are followed by resist strip-off, resulting in direct access to the gate contact pad (Scheme 2n). The semiconductor is deposited as the last processing step. Two self-assembled monolayers (SAMs), of pentafluorobenzenethiol (PFBT) and trichlorophenylsilane (TCPS), are applied prior to deposition of the semiconductor by inkjet-printing of a blend of 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS pentacene) and polystyrene (PS) [30] (Scheme 2o).

2.2. Fabrication

In the fabrication process of the TFTs on flexible foil, the dimensionally instable foil plays a crucial role. A wavy substrate results during the imprinting process in an inhomogeneous residual layer, being thicker in the wave valleys and thinner on the wave hills. Removing the residual layer



Scheme 1. Schematic view of the here fabricated bottom-contact, bottom-gate TFTs on (a) Si and (b) PEN foil. Gate, source–drain and contact hole have been subsequently patterned by SFIL. For the flexible TFTs, a planarization layer of $25 \times 25\ mm^2$ has been formed by imprinting, and an oxide etch barrier has been deposited before imprinting the gate. The semiconductor has been inkjet-printed on the five 5 μm wide, interdigitated source–drain fingers, with channel lengths of 5 μm down to 250 nm. The square contact pads are $200 \times 200\ \mu m^2$.



Scheme 2. Process flow for the fabrication of flexible TFTs with the planarization, gate, source–drain and contact hole layers patterned by SFIL. The semiconductor is patterned by inkjet printing. TFTs on Si are made in a similar fashion, leaving out the planarization step.

of features in the wave valleys partially coincides with complete removal of the features on the hills if the feature height is less than the wave height. Reversible lamination of the foil on a Si carrier improved handling and reduced the overall waviness to <1 μm with a total wafer bowing of <10 μm. FOC bowing is induced by a difference in coefficients of thermal expansion between the foil, glue and Si wafer [31], and has been observed for planarization materials and glues tested for reversible gluing of the foil to the carrier [7,32,33]. An earlier reported FOC fabrication process [27], made by thermal flat-embossing of the foil on a poly(methylmethacrylate) (PMMA)-coated Si wafer with a non-patterned Si wafer as the mold, was replaced by a FOC made by reversible lamination of a thinner and therefore less stress-inducing 25 μm PEN foil. However, the substrate was still found to be insufficiently flat, with an overall waviness of ~1.0 μm, to pattern all three layers by SFIL due to a too inhomogeneous RLT.

Therefore, we developed a fast and simple method for field-by-field planarization of wavy substrates. With SFIL, a $25 \times 25\ mm^2$ flat area was imprinted on the wavy substrate by pressing, at room temperature under low pressure, a non-patterned template against the foil. The self-leveling capability of the template during imprinting, caused by capillary forces pulling down the template against the foil, resulted in an imprinted, flat plateau on the foil surface. Surface contour maps recorded before (Fig. 1a) and after (Fig. 1b) imprint planarization of the same area on the FOC show the decrease of the surface waviness from 700 nm in the non-planarized state to 260 nm on the planarized foil over an area of $12 \times 12\ mm^2$. Planarization provides a sufficiently flat

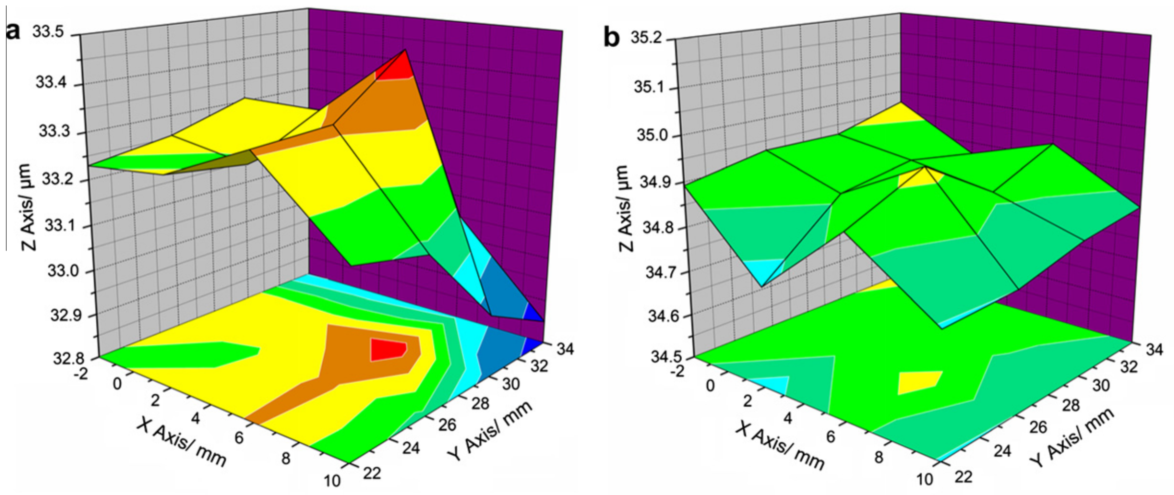


Fig. 1. Surface contour maps of a FOC showing a surface waviness over an area of $12 \times 12\ mm^2$ of (a) 700 nm without and (b) 260 nm with an imprinted planarization layer.

surface to obtain a thin and homogeneous residual layer, thus allowing multiple imprint steps.

The set of three UV-transparent fused silica templates used here for subsequent imprinting of the gate, source–drain and contact hole layers, contained features in the dimensional range of 100 nm up to 750 µm with a depth of 300 nm on an active area of $11 \times 11\ mm^2$.

Before patterning the first layer of the TFT on the FOC, an etch stop of 50 nm Al_2O_3 was evaporated on the planarization layer, to protect the planarization layer made of imprint resist from being etched during gate processing or resist strip-off. Without etch stop, a higher current leakage or even shorts between the source–drain and gate layer were observed and some TFTs burned through after multiple I/V measurements right at the edge of the gate. With an etched planarization layer, the source–drain fingers had to cover a step height of about 150 nm, which is 100 nm more than initially designed (See Supporting Information Fig. S1a). The source–drain fingers thus became very thin at this large step and heated up quickly due to resistance, while the source–drain contact pad was very close to the gate causing a high leakage current. Introduction of the oxide etch stop resulted in a step height of only 50 nm (See Supporting Information Fig. S1b), whereafter no shorts or burned TFTs were observed anymore.

For the gate layer itself, 3 nm Cr adhesion metal and 47 nm Au were deposited by e-gun evaporation on the etch stop layer. Sputtering was not an option, as it would heat up the foil too strongly. The SFIL patterning process, being the same for all three layers, will be exemplarily explained for the gate layer in the following lines. Where applicable, differences in the patterning process between the three layers will be noted.

As adhesion promoter for the imprint resist, a 60 nm thick layer of DUV30J was spincoated on the entire sample. A low-viscosity, organic, and UV-curable resist (MonoMat™) was field-by-field drop-dispensed in pL amounts onto the substrate. The template was brought into contact with the resist droplets under low pressure (2–3 N) at room temperature. Capillary force action pulled the template further down spreading the resist over the active area and filling thereby the structures in the template within 60 s. Broadband UV light was guided through the template curing the resist within 3 s, leaving an inverse replica of the template features on the substrate after demolding. An anti-sticking layer (RelMat™) applied to the template before imprinting allowed easy demolding and complete pattern transfer with no residues remaining on the template. The residual layer of approximately 80 nm, recorded by profilometry, was removed by anisotropic oxygen-based reactive ion etching (O_2 RIE) after imprinting. The gate (or source–drain) features remained covered with resist, allowing selective removal of the unprotected Au and Cr within 4 min by Ar ion beam etching (IBE). Wet etching of the metal layers was not an option, especially for the sub-micron features, as it created a line edge roughness (LER) of around 100 nm and induced pattern destruction by partial lifting or entire removal of the features. In case of patterning the source–drain layer, the underlying dielectric was also negatively affected by wet etching, predominantly by oxide removal. The third imprinted layer of the TFT left a protective resist mask over the entire sample, except for a window of $180 \times 180\ \mu m^2$ exactly above the gate contact pad. The residual layer was removed by O_2 RIE and the underlying metals and dielectric were removed by ion beam etching within 10 min, creating a contact hole to the gate. After pattern transfer of the imprinted features into the underlying layer by ion beam etching, the remaining resist was stripped off.

The different stages of the multilayer fabrication of the TFT on foil by UV NIL are shown in Fig. 2. The first layer patterned was the 70 µm wide gate (Fig. 2a and b), followed by the source–drain layer with source–drain fingers separated by a line spacing of 5 µm down to 200 nm. The smallest channel lengths fabricated on PEN foil, separating the 5 µm wide source–drain fingers, were 500 nm and

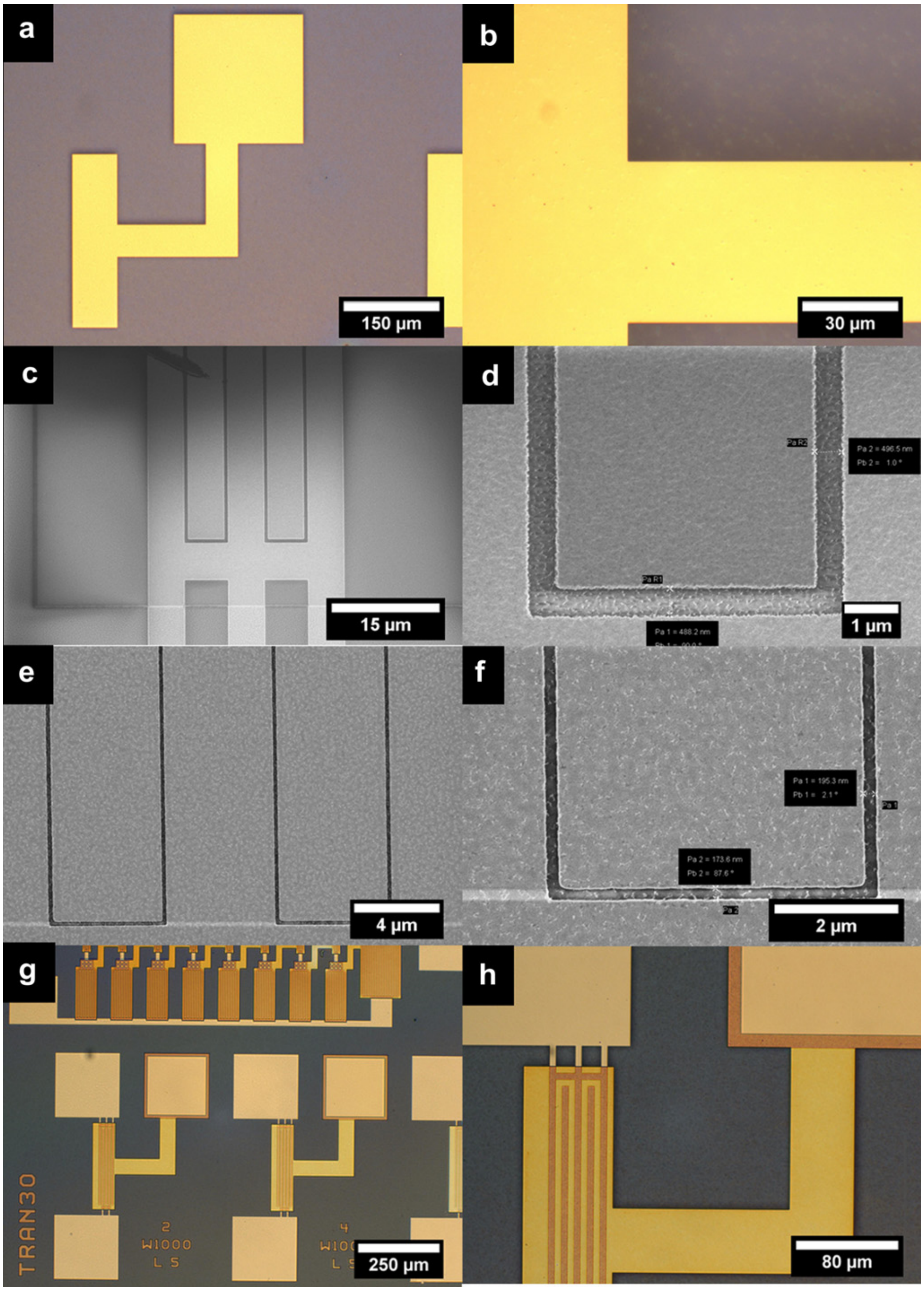


Fig. 2. (a, b, g and h) Optical microscopy and (c–f) SEM images of the different stages of the fully UV NIL-patterned TFTs on PEN foil. (a and b) First imprinted layer: 70 µm wide gate. (c–f) Second imprinted layer: 5 µm source–drain fingers with a line spacing of (c and d) 500 nm and (e and f) 200 nm. (g and h) Third imprinted layer: $180 \times 180\ \mu m^2$ contact holes through the dielectric to the gate. Also shown are the 5 µm wide and spaced source–drain fingers.

200 nm (Fig. 2c–f). As third and last patterned layer, contact holes of $180 \times 180\ \mu m^2$ were made through the dielectric (Fig. 2g and h).

The images in Fig. 2 show that all layers of our multilayer device have been successfully patterned on PEN foil with the above described patterning strategy. The subsequently deposited and patterned layers adhered well to each other and to the substrate. The patterned features exhibit sharp edges and rectangular corners, from the largest channel dimensions of 5 µm down to the smallest 200 nm channels. A small line edge roughness of around 40 nm (Fig. 2d) is visible, dominated by the ion beam etching process to remove unmasked metal. Wet etching would have created, as reported above, a LER of $\sim$100 nm. Alignment of the gate to the source–drain layer was achieved by overlay of two gratings with a difference in line periodicity of 25 nm creating a moiré interference pattern. An alignment accuracy of the source–drain to the gate of 25–200 nm on Si and 50–300 nm on FOC has thus been obtained. The overlay of the source–drain fingers to the gate was made asymmetric on purpose (Fig. 2g and h), allowing the gate to control a larger area of the inkjet-printed semiconductor during device operation.

The gate dielectric was, as in many electronic devices, a critical parameter strongly influencing the quality of the TFTs. As dielectrics for the TFTs on foil, oxides (Al_2O_3 and SiO_2) and organic materials (SU8, Parylene C) have been tested. SU8 is readily available in the semiconductor industry, has a high chemical resistivity, thermal stability and dielectric strength [34]. However, in our case, SU8 was disqualified as dielectric due to the thermal expansion mismatch to the FOC, resulting in a too strongly bowed FOC after SU8 spincoating and soft bake at 95 °C. Parylene C on the other hand, could be deposited in a 150 nm thick layer by vapor deposition polymerization at a substrate temperature near room temperature. Parylene C has a high dielectric strength, high chemical and moisture resistance, and provides a hydrophobic surface beneficial for pentacene growth [35]. Unfortunately, as Parylene C is an organic material, it appeared sensitive to the here performed etching steps. Resist strip-off after source–drain and contact hole patterning simultaneously removed the dielectric due to a nearly identical etch rate of 100 nm/min of resist and Parylene C. Regarding the two tested electron beam-evaporated oxides, SiO_2 appeared superior over Al_2O_3. Therefore, SiO_2 was used as the dielectric in all devices described below.

As the TFTs were made in a bottom-contact, bottom-gate architecture, the final layer added to the device was the organic semiconductor. A PFBT SAM was deposited on all gold contacts to improve the charge injection [36]. TCPS was deposited on all oxide surfaces to reduce electron trapping at the oxide interface. SAMs are known to improve the molecular order of the deposited semiconductor [37]. A blend of TIPS pentacene:PS in a 2:1 w/w ratio was inkjet-printed onto the interdigitated source–drain fingers, leading to TIPS pentacene crystals grown from the edge to the center of the inkjet-printed droplets [30] (see Supporting Information, Fig. S2). Photographs of the finished TFTs on foil using multistep UV NIL after debonding from the Si carrier are shown in Fig. S3.

2.3. Electrical characterization

To demonstrate the feasibility of the here developed multilayer imprinting process, SFIL-patterned TFTs on Si and PEN foil were electrically characterized in a non-illuminated glove box under N_2 atmosphere. The gate voltage was varied from 10 V to −10 V in a double scan and the bias over source and drain (V_{DS}) was held at −10 V. Transfer and output characteristics of fully UV NIL-patterned TFTs with a channel width of 1000 μm and length of 5 μm arranged in a comb structure, and the corresponding square route of I_{DS}, were recorded.

First, results for the TFTs on Si will be shown and discussed (Fig. 3a and b). From the semi-logarithmic plot (I_{DS} vs. V_G; Fig. 3a), an on/off ratio of 5×10^5, a sub-threshold swing of 0.7 V/dec and a low switch-on voltage of $V_{SO} = 1.3$ V for the TFT on Si have been calculated. The switch-on voltage was taken as the gate voltage at which the drain current is one order of magnitude higher than the off-current I_{off} [28]. From the plot of the square root of I_{DS} vs. V_G (Fig. 3a), a high gate-dependent mobility of $\mu = 0.65 \pm 0.16$ $cm^2\,V^{-1}\,s^{-1}$ (average over four TFTs) and maximum of $\mu = 0.92$ $cm^2\,V^{-1}\,s^{-1}$ at $V_G = -0.75$ V has been determined. The field-effect mobility was thereby calculated from Eq. (1), with $V_{DS} = -10$ V:

$$\mu_{sat}(V_G) = \frac{2L}{W \cdot C_i}\left(\frac{\partial\sqrt{I_{SD}(V_G)}}{\partial V_G}\right)^2 \tag{1}$$

where C_i is the capacitance per unit area of the gate dielectric layer, and L and W are channel length and width, respectively. The electrical characteristics of the here fabricated fully UV NIL-patterned, bottom-contact, bottom-gate TFTs on Si are in good agreement, and in many cases improved in comparison to reported values in literature. Common gate TFTs with the same TIPS pentacene/PS blend (67 wt%) inkjet-printed on photolithography patterned, golden source–drain electrodes on highly doped n^{++} Si wafers with a 140 nm thermally grown SiO_2 gate dielectric, showed a slightly higher mobility of $\mu_{sat} = 0.72 \pm 0.17$ $cm^2\,V^{-1}\,s^{-1}$ (average over 73 TFTs) for a channel length of 5 μm [30].

The here developed UV NIL-based patterning strategy allowed downscaling of the channel length into the low sub-micron regime. TFTs with a channel length as small as 250 nm have been fabricated. To our knowledge, this is the first report of such a small channel length with the here utilized, inkjet-printed blend of semiconductor TIPS pentacene and PS. Further downscaling is limited by the e-beam written patterns in the template, not by the imprint process itself. The plot of the mobility at $V_{DS} = -1$ V and −10 V as a function of the channel length L (with 250 nm < L < 5 μm) (Fig. 4), shows a decrease in the mobility with decreasing channel length. The trend line (Fig. 4, only a guide to the eye) indicates the existence of a contact resistance, turning more dominant for smaller channel lengths. The non-linear slope in the corresponding I_{DS}/V_{DS} plot (Fig. 3b) confirms this contact resistance. A thin PS layer deposited directly on top of the Au contacts by phase separation from the semiconductor blend upon inkjet printing might be the origin of the experienced contact resistance [30]. Very recently [38], it has been reported that PS accumulates at the center of the droplet upon evaporation of the TIPS pentacene/PS blend, resulting in less semiconductor in the center of the droplet. The exact spread of this PS enriched zone, however, is not clear up to now. The droplet was printed off-center on purpose (Fig. S2b), to move the PS-enriched zone away from the TFT channels and to control the crystal orientation of the TIPS pentacene. In case the PS-enriched zone spreads as

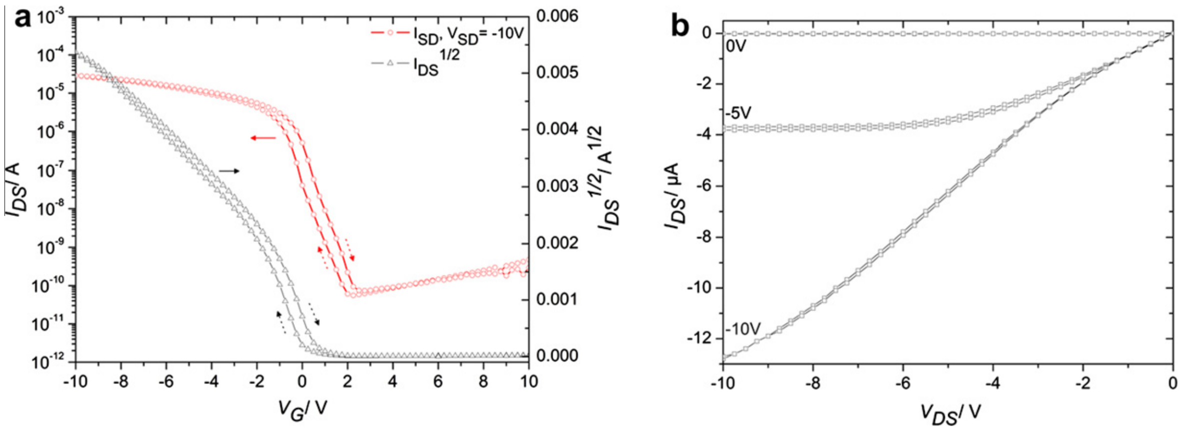


Fig. 3. (a) Transfer characteristics and the corresponding plot of the square root of I_{DS} of one fully UV NIL-patterned bottom-contact, bottom-gate TFT on Si. Channel length and width are 5 and 1000 μm respectively. A 150 nm thick SiO_2 layer served as the gate dielectric, and a blend of TIPS pentacene/PS as the semiconductor. (b) The output characteristics of a TFT on Si with a gate voltage between 0 and −10 V at a step of 5 V.

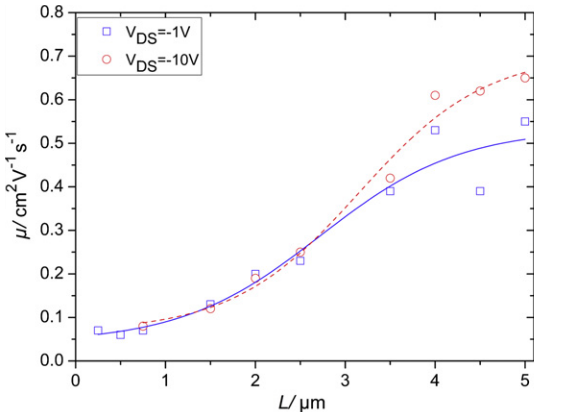


Fig. 4. Mobility μ at $V_{DS} = -1$ V (blue) and -10 V (red) as a function of the channel length L for the fully UV NIL-patterned TFTs on Si. The solid ($V_{DS} = -1$ V) and dashed ($V_{DS} = -10$ V) lines are a guide to the eye to indicate the mobility trend. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

far as the channels, it directly influences the electrical performance.

Next, we used the here engineered process with imprint planarization (Scheme 2) to demonstrate TFTs on PEN foil. The transfer, output characteristics and the corresponding square root of I_{DS} are shown in (Fig. 5a and b).

The mobilities as function of the channel length from 5 μm down to 500 nm are given in Fig. 6. From the semi-logarithmic plot (I_{DS} vs. V_G), an on/off ratio of 7×10^6, a sub-threshold swing of 0.9 V/dec and a switch-on voltage of $V_{SO} = 7.4 \pm 0.7$ V for the TFTs on flexible foil have been calculated. From the plot of the square root of I_{DS} (Fig. 5a), a gate-dependent mobility of $\mu = 0.20$ cm^2 V^{-1} s^{-1} at $V_G = -0.50$ V (average over four TFTs: $\mu = 0.27 \pm 0.05$ cm^2 V^{-1} s^{-1}) has been determined. The on-current at V_G = - −10 V is comparable to the data obtained for the TFT on Si (Fig. 3a), but significant differences are visible in the switch-on voltage, hysteresis and mobility. The TFTs on Si and PEN foil have an identical device architecture and are fabricated with the same process, except for the additional imprinting of the planarization layer and oxide etch stop deposition in case of the TFTs on foil. The positive shift of the switch-on (and off) voltage and the observed hysteresis in the transfer characteristics of the TFT on foil (Fig. 5a), are a result of charge trapping at the oxide – semiconductor interface [39,40]. A slightly different spreading of the semiconductor during inkjet printing was observed, which indicates a differently packed silane (TCPS) layer on the dielectric (SiO_2) for both substrates. The quality of the monolayers directly influences the crystal orientation of the semiconductor and potentially even the phase separation of PS out of the blend. The difference in monolayer packing might originate from an increased roughness of the dielectric and source–drain contacts, caused by the initial roughness of the foil and its dynamic response to temperature cycling during material deposition steps and RIE processing. The shoulder-like behavior seen in the I/V curve for the flexible TFTs might be explained by a back-channel effect [30,41]. The electrical characteristics of our TFTs are comparable to earlier reported values in literature with photolithographically patterned bottom-contact, bottom-gate TFTs on PET foil with an average saturation mobility of $\mu = 0.22 \pm 0.05$ cm^2 V^{-1} s^{-1} [42]. TFTs with a small channel length down to 500 nm have also been fabricated on foil. Plotting the mobility at $V_{DS} = -1$ V and -10 V vs. the channel length shows a transition point at $L = 1.5$ μm (Fig. 6). The drop in the mobility below L <1.5 μm indicates a limited charge injection, which is supported by the non-linear plot of the square root of I_{DS} vs. V_G (Fig. 5a). Furthermore, charge injection is limited due to the ink blend properties, as discussed for Si previously. Above $L = 1.5$ μm the data in Fig. 6 could indicate a plateau (with large data scatter) as now indicated by the trend-lines, or point to a decrease of the mobility at higher channel lengths. A decreasing mobility at larger channel length is possible [43]. More measurements are needed, however, to investigate this in more detail. Transfer characteristics for $L = 2.0$ μm, 1.0 μm, 0.75 μm, and 0.5 μm and output

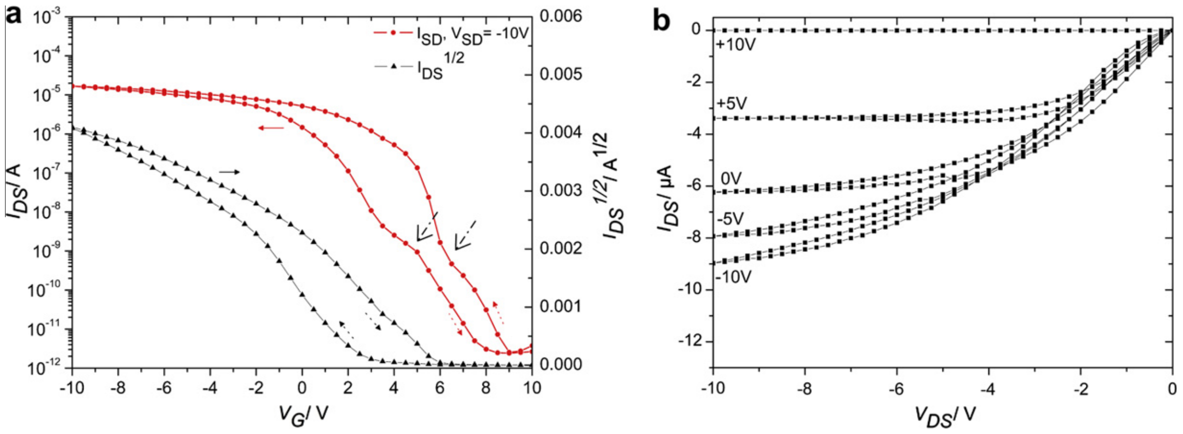


Fig. 5. (a) Transfer characteristics and the corresponding plot of the square root of I_{DS} of one fully UV NIL patterned bottom-contact, bottom-gate TFT on PEN. Channel length and width are 5 and 1000 μm respectively. A 150 nm thick SiO_2 layer served as the gate dielectric, and a blend of TIPS pentacene/PS as the semiconductor. The shoulders in the *I*/*V* characteristics are indicated by the dash-dotted arrows (b) The output characteristics of a TFT on PEN with a gate voltage between +10 V and −10 V at a step of 5 V.

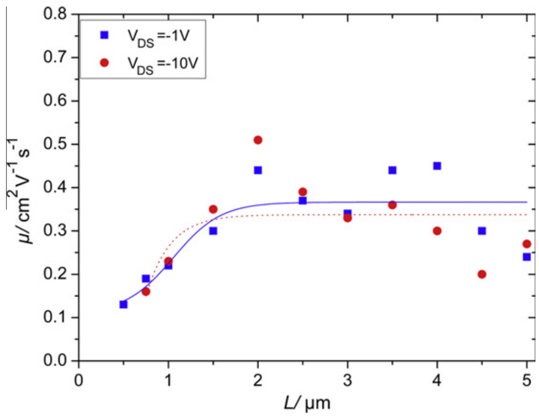


Fig. 6. Mobility μ at $V_{DS} = -1$ V (blue) and −10 V (red) as a function of the channel length *L* for the fully UV NIL-patterned TFTs on PEN foil. The solid ($V_{DS} = -1$ V) and dashed ($V_{DS} = -10$ V) lines are a guide to the eye to indicate the mobility trend. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

characteristics for $L = 2.0$ μm and 0.75 μm are shown in Fig. S4, showing also the positive shift of the threshold- and switch-on voltage for a decreasing channel length.

Our results confirm that high-quality bottom-contact, bottom-gate TFTs have been made by patterning the entire MIM stack with UV NIL on PEN foil with channel lengths as small as 500 nm on foil, holding promise for facile R2R production.

3. Conclusions

In this paper, the feasibility of UV NIL as a patterning technique for the fabrication of multilayered, electronic devices on Si and PEN foil has been shown. Bottom-contact, bottom-gate TFTs have been fabricated as demonstrators by patterning the entire MIM stack of the TFT by UV NIL, forming the gate, source–drain and contact hole with an alignment precision of 25–200 nm on Si and 50–300 nm on foil. We could only successfully and reproducibly pattern all three layers of the TFT on foil by introduction of imprint planarization, allowing a controlled and homogeneous residual layer thickness. A further conclusion of this work is, that the dielectric should match the coefficients of thermal expansion of the foil-on-carrier system (excluding SU8) and should withstand or at least show a high etch selectivity to the imprint resist upon reactive ion etching and resist strip-off (excluding Parylene C). The performance of the TFTs on Si and PEN foil with the largest channel length ($L = 5$ μm) is comparable with state-of-the-art devices fabricated by photolithographic patterning [30,42]. By downscaling the channel length, TFTs with a minimal channel length of 250 nm on Si and 500 nm on PEN foil have been demonstrated.

The final TFT fabrication process on foil is envisioned to be R2R imprinting. The critical overlay of the source–drain and gate cannot be accurately enough controlled in a R2R process. Therefore, efforts are undertaken to develop a self-aligned imprinting process, implementing the fabrication lessons learned here with the room temperature, low pressure and high precision technique SFIL.

4. Experimental

4.1. Materials and methods

Imprint resist MonoMat and anti-sticking layer RELMAT™ were purchased from Molecular Imprints, Inc. An experimental poly(ethylenenaphthalate) foil (PEN, 25 μm thick) was provided by Holst Centre. 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS pentacene) was synthesized according to literature [44]. Polystyrene (PS) (Mw ≈ 9.58 kDa, PDI = 1.03) was purchased from Fluka. 1,2,3,4-Tetrahydro-naphthalene (tetraline) was purchased from Merck.

4.2. Foil-on-carriers (FOCs)

FOCs have been made by reversibly laminating the PEN foil with a glue to a double-side polished Si wafer at a temperature < 95 °C. The foil was cut according to the size of the carrier (4 in Si wafer) and thermally cured by heating for 1 h at 170 °C in a convection oven.

4.3. Step-and-flash imprint lithography (SFIL)

The UV-transparent quartz templates used for the experiments were fabricated by standard e-beam lithography and RIE techniques. The templates contained, on an active area of 11×11 mm^2, test features in the dimensional range of 100 nm up to 750 μm and the TFT features with channel lengths from 5 μm down to 250 nm with a depth of 300 nm. SFIL was performed with an Imprio 55 tool from Molecular Imprints, Inc. The imprints were carried out at room temperature and under a force of 3 N. For improved adhesion of the drop-dispensed imprint resist (MonoMat™), a BARC layer of DUV30 J was spincoated on the surfaces at 3000 rpm for 1 min and baked for 2 min at 120 °C. MonoMat™, after field by field drop dispensing on the substrate, filled the template within 60 s and was cured through the backside of the template for 3 s with broadband UV light (exposure dose of 80 m J/cm^2 and λ = 230–360 nm).

4.4. Dry etching

Anisotropic O_2 plasma-based reactive ion etching was performed in a home-built tool (Tetske) at a chamber pressure of 10 mTorr and 20 sccm O_2 at 20 W to remove the thin residual layer within 1 min and to strip-off the resist after processing within 2 min. Unprotected metal (Cr and Au) and dielectric of the MIM stack were removed by Ar ion beam etching with an Oxford Ionfab 300, removing the metal layer within 5 min and the 150 nm SiO_2 within 10 min, controlled by an endpoint detection system.

4.5. Dielectric deposition

Parylene C was deposited with a dedicated Parylene coater (SCS Labcoter 2 Parylene Deposition System 2010). SU8–5 (MicroChem) has been deposited by spincoating for 10 s at 500 rpm and 30 s at 4000 rpm followed by a soft bake program starting at 25 °C, holding the temperature 1 min at 50 °C, 1 min at 65 °C and 3 min at 95 °C after which the temperature was slowly decreased to 25 °C. An SU8 layer thickness of 4.1 μm has been obtained. SiO_2 and Al_2O_3 were evaporated in a Balzers evaporator (BAK600) using an 8 kV e-gun beam at a pressure of 9×10^{-7} bar resulting in a deposition rate of 3–5 Å/s.

4.6. Self-assembled monolayers (SAMs)

PFBT was deposited by 15 min dipping of the sample into a PFBT (10 mM) solution in ethanol, followed by rinsing with ethanol and N_2 blow drying. N_2 was utilized as carrier gas bubbling through TCPS in a closed chamber at atmospheric pressure for 15 min to deposit TCPS from the gas phase on all oxide areas. The substrates were baked 2 min at 100 °C on a hot plate after flushing the chamber with N_2 to remove the side product (hydrochloric acid) of the condensation reaction.

4.7. Semiconductor deposition

An ink-jet printing setup with a high-precision vertical translation stage and a Microfab glass nozzle (type MJ-ATP-01–50-DLC, 50 μm orifice diameter) was used to print the blend of TIPS pentacene (20 mg/ml):PS (10 mg/ml) in a blending ratio of 2:1. Droplets with a volume of 50 pL were jetted on demand, onto transistor substrates kept at a temperature of 70 °C. All printing experiments were performed in ambient cleanroom conditions [30].

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Appendix A. Supplementary material

A schematic representation of the layout of the bottom-gate TFT with and without etch barrier, optical microscopy images of the inkjet-printed TIPS pentacene/PS blend on the fully patterned TFT, and photographs of the final flexible TFTs are given.

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.orgel.2012.09.001.

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