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AMERICAN SCIENTIFIC PUBLISHERS

Science of Advanced Materials
Vol. 6, pp. 1–9, 2014
(www.aspbs.com/sam)

A Fast Room-Temperature Poling Process of Piezoelectric $Pb(Zr_{0.45}Ti_{0.55})O_3$ Thin Films

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ABSTRACT

The effect of two poling processes on the ferroelectric and piezoelectric properties of sol–gel and pulsed-laser-deposited $Pb(Zr_{0.45}Ti_{0.55})O_3$ (PZT) thin films has been investigated as a function of the poling field, poling temperature and poling time. In the case of *dc*-electric field poling at an elevated temperature (200 °C), the remnant polarization and effective piezoelectric coefficient are found to increase with and saturate at high *dc*-poling field (400 kV/cm) and long poling time (30 minutes). The room-temperature poling process using *ac*-electric field poling, shows the same trend with poling field but much shorter poling times (100 seconds), with only a slightly lower saturation value of polarization. It is suggested that in room-temperature poling screening charges are merely rearranged, whereas in high temperature poling these charges are largely removed. A much larger improvement in the properties of sol–gel PZT thin films is found, as compared to those deposited using pulsed laser deposition (*PLD*), indicating that a poling process is required for sol–gel films.

KEYWORDS: Piezoelectric Film, Poling Process, Poling Conditions, Screening Charge, Grain Boundary.

1. INTRODUCTION

Piezoelectric micro-electromechanical systems (piezoMEMS) have received a great deal of attention in recent years. Sensing and actuation capabilities in most of the MEMS devices utilize the piezoelectric effect, such as in bio-sensors,[1–3] micro-machined ultrasonic transducers (MUTs),[4,5] accelerometers[6] resonators,[7] and micro-pumps.[8,9] Among piezoelectric thin-film materials, $Pb(Zr_x, Ti_{1-x})O_3$ (PZT) films can offer an attractive option for piezoMEMS technology due to their superior ferroelectric and piezoelectric properties, and moreover, ease of integration into microsystems.[10]

In ferroelectric materials, domains of continuous crystallographic orientation and polarization form spontaneously upon cooling from above the Curie temperature. When cooling a ferroelectric sintered ceramic or (epitaxial) thin film in the absence of an electric field, these ferroelectric domains form in a manner that is elastically and electrically self-compensated. In ceramics the net polarization can be very small, whereas in thin films one may observe already a significant net polarization, induced by the substrate induced strain. However the net polarization is generally much less than can be reached by a process known as poling.[11,12] During poling, when a sufficiently high *dc*-electric field is applied to the ferroelectric materials, the domains become oriented in the allowable directions closest to the direction of applied field. Secondly the internal screening, due to localized charges, can be reduced significantly by the poling process. When the field is removed, the orientation of domains is largely retained because of the reduced internal screening; poling is therefore an important process to enhance the ferroelectric and piezoelectric properties in ferroelectric materials.[12–14]

In general, the alignment of ferroelectric domains is dependent on the poling conditions: the-poling field strength, poling temperature and poling time.[14,15] In the poling process, a higher poling field generally results into more complete domain polarization. A longer poling duration and a higher poling temperature will derive better domain alignment as well as make the domain motion easy.

Kohli et al.[16] showed that the domain fraction of out-of-plane oriented polarization domains in highly tetragonal, sol–gel deposited $Pb(Zr_{0.15}Ti_{0.85})O_3$ thin films can be significantly increased by applying a large number of high-voltage bipolar pulses or by high *dc*-field poling at 160 °C, enhancing the ferroelectric and piezoelectric properties

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Received: XX xxxx xxxx
Accepted: XX xxxx xxxx

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significantly. In the case of hot poling the improvement is larger and much more stable than for room temperature pulse poling. This was attributed to a stabilization of defect-dipole complexes in the case of hot poling.

The effects of repetitive slow bipolar pulse poling at 80 °C and *dc*-field poling at 80 °C on the properties of a range of soft and hard $0.05(PbSn_{0.5}Sb_{0.5}O_3)$–0.95 $(PbZr_xTi_{1-x}O_3)$ sintered powder ceramics were compared by Ogawa and Nakamura.[17] With increasing pulse time and maximum voltage the planar coupling coefficient increases and saturated with increasing ac pulse number. The (relative) improvement was significantly more for the hard ceramics. *ac*-poling on *dc*-poled samples degraded the properties on the first poling pulse, and the properties were only partly recovered on further pulsing.

Nakajima et al.[18] showed that on increasing the maximum applied field E_{max}, when cycling at room temperature through the hysteresis loop of $PbZr_{0.39}Ti_{0.61}O_3$ thin film devices, deposited by metal organic chemical vapor deposition on a platinized Si wafer, the remnant polarization increases from approximately zero, going through two threshold maximum field values and saturates at high E_{max} (above 250 kV/cm). The volume fraction of out-of-plane oriented tetragonal domains was shown to have increased significantly and permanently using *in-situ* Raman Spectroscopy.

Kobayashi et al.[19] used high voltage *ac*-pulsing (during an unspecified time) to pole $PbZr_{0.3}Ti_{0.7}O_3$ sol–gel deposited thin films on platinized silicon-on-insulator wafers, before and after structuring the films into cantilevers by deep reactive ion etching (DRIE). It was found that *ac*-pulsing can strongly improve the film properties when it is applied after structuring, but if poling was applied before structuring, its properties can not fully be restored by a second poling after structuring. It was suggested that out-of-plane oriented domains are more susceptible to damage by DRIE than in-plane oriented domains, but no explanation was given for this one.

In this paper we study the effect of room temperature of poling by a single unipolar *ac*-pulse and of high temperature *dc*-poling on the ferroelectric and piezoelectric properties of $Pb(Zr_{0.45}Ti_{0.55})O_3$ thin films made along various processing routes using different deposition techniques (pulsed laser deposition and sol–gel), resulting in different crystalline qualities. We studied in detail the influence of poling method, field strength and poling time for the different quality films, which allows us to distinguish the effects of method parameters on the one hand and film quality on the other hand. It is shown that the room-temperature *ac*-poling method results in a much faster poling process, although with somewhat less perfect poling. Further it is shown that the time constants involved in the poling process do not depend on the film quality, for the films investigated, but do depend on the poling field strength and poling temperature. It is suggested that with the room-temperature unipolar *ac*-poling procedure the screening charges are rearranged such as to give less screening, whereas with the high-temperature *dc*-poling procedure they are largely removed from the film.

2. EXPERIMENTAL DETAILS

2.1. Thin-Film Capacitor Fabrication

Three types of ferroelectric devices on a Si substrate were fabricated along different routes, resulting in different crystalline structures, but all with (001) orientation of the PZT film. The different materials and processes used for the $Pb(Zr_{0.45}Ti_{0.55})O_3$ (PZT) thin films on the different substrates, $Pt/Ti/SiO_2/Si$ and $SrRuO_3/SrTiO_3/Si$, are given in Table I.

For two devices (Text(001) and Epi(001)) pulsed laser deposition (*PLD*) was used for the deposition of the PZT layer. The laser ablation was carried out at laser fluencies of 2–3 J/cm^2 with repetition rates of 5–10 Hz, using a KrF excimer laser with a wavelength of 248 nm. The target-to-substrate distance was fixed at 60 mm and the PZT thin films were fabricated in an oxygen atmosphere of 75 mTorr at 600 °C. Details of the *PLD* deposition parameters of $SrRuO_3$ (SRO) electrodes are given in Ref. [20]. The 30-nm $SrTiO_3$ (STO) buffer-layer on the Si-substrate of the Epi(001) device was deposited by molecular beam evaporation (*MBE*).[21]

The textured PZT films in the SG(001) devices were prepared by a sol–gel technique, where a PZT precursor solution was prepared from lead acetate ($Pb[OAc]_2 \cdot 3H_2O$), titanium *iso*-propoxide ($Ti[i\text{-}OPr]_4$) and zirconium *n*-propoxide ($Zr[n\text{-}OPr]_4$) in 2-methoxyethanol solvent. The 0.4 M PZT precursor with 10 mol.% excess lead content in solutions was prepared and spin coated on $Pt/Ti/SiO_2/Si$ wafers at 4000 rpm for 30 seconds, followed by pyrolysis at 400 °C for 10 min. The process was repeated until the PZT thin films with the required layer thickness were obtained. Finally, thermal annealing at 650 °C during 60 min was carried out to obtain the ferroelectric phase PZT thin films. More details on the fabrication and morphology of sol–gel PZT thin films have been described in a previous publication.[22]

The thickness of all PZT thin films is 500 nm. The crystallinity of the films was determined with X-ray diffraction (XRD). θ–2θ scans show that the *PLD* films all are (001) oriented, while the SG(001) film shows a fraction with (111) orientation.[23] The Epi(001) is fully aligned in the in-plane direction as well, as was shown by the fourfold symmetry of the phi-scans, whereas the SG(001) and Text(001) are textured (no preferential in-plane orientation). From the rocking curves the average tilt angle α_{av} of the grains in the films was determined,[23] which is a few degrees for the textured films and only 0.3° for the Epi(001) film. We expect that a larger α_{av} value implies a poorer crystallographic lattice fit at the grain boundaries between adjacent grains, thus larger effect of grain boundaries on for example the poling process. In Ref. [23] we

Table I. Fabrication processes and layer stacking of PZT thin film capacitors.

Device	Piezoelectric stack	Top-electrode	PZT film	Bottom-electrode	Buffer-layer	Substrate	α_{av} (°)
SG(001)	Textured (100)-oriented PZT on (111)Pt/Ti/SiO_2/Si	100 nm Pt *sputtering*	500 nm sol–gel	Pt/Ti = 100/15 nm *sputtering*	500 nm SiO_2 *thermal oxidization*	(001)Si	4.9
Text(001)	Textured (100)-oriented PZT/LNO on (111)Pt/Ti/SiO_2/Si	100 nm Pt *sputtering*	500 nm 10 nm LNO PLD	Pt/Ti = 100/15 nm *sputtering*	500 nm SiO_2 *thermal oxidization*	(001)Si	3.6
Epi(001)	Epitaxial (001)-oriented PZT on (001)SRO/STO/Si	100 nm SRO *PLD*	500 nm *PLD*	100 nm SRO *PLD*	30 nm STO *MBE*	(001)Si	0.3

have shown that the ferroelectric and piezoelectric properties of poled films are strongly correlated to α_{av}. This was ascribed to the dielectric properties of the tilted grain boundaries. Relations have been established between α_{av} and these properties.

For the electrical measurements, the 200×200 μm^2 capacitors are patterned by lithography process and structured by argon etching of the top electrode and wet etching (HF–HCl solution) of the PZT layer.

2.2. The Poling Process

Before poling, a ferroelectric ceramic material consists of small grains (crystallites), each containing polarization domains in which the polar direction of the unit cells are aligned. In a polycrystalline ceramic material the grains and therefore the polarization domains are randomly oriented and hence, the net polarization of the material is strongly reduced or even zero, i.e., the ceramic does show little exhibit ferroelectric properties. In the poling process, a sufficiently high *dc* electric field is applied, usually at a temperature slightly below the Curie temperature of the ferroelectric material (see Fig. 1(a)), which will orient the domains as much as the crystallographic structure allows in the field direction. After cooling of the sample and removal of the poling electric field, most of the dipoles are locked into a configuration of near alignment) known as the remnant polarization.[24] The remnant polarization is generally less than the maximum (saturation) polarization, due to the random orientation of the grains, residual charged defects in the grain boundaries (GBs) and (polarized) defects in the grain interior, partially screening the polarization in the grains.

In (001) oriented thin films the situation is in so far different that the crystallographic lattice of the grains has a preferential direction, although with a spread α_{av}, around the film normal direction. (With the notation (001) we refer here to the pseudocubic lattice: the film plane corresponds to the (001) plane. For the PZT composition used here, which has a tetragonal unit cell, the unit cell and hence the polarization vector can be oriented perpendicular to as well as parallel to the film plane. This is in literature also referred to as (001)/(100) oriented films.) The in-plane orientation of the unit cell depends on the substrate and intermediate layers.[23] The largest defects in the film are the GBs, which are predominantly approximately perpendicular to the film plane, extending from the bottom to the top electrode. It is generally assumed that during the poling process the charges in the GBs are removed or compensated, removing the low resistance current path along the GBs, so that also the leakage current of the device is strongly reduced after poling. This is clearly seen in Figure 2(b) for the SG(001) device after the high temperature poling process. On the other hand the SG(001) device poled with the room temperature process hardly shows any leakage current reduction. We have also observed large reductions of leakage currents in *PLD* PZT thin-film devices.[25] The clearest effect of the poling is the permanent increase of the remnant polarization P_r, because of reduced polarization screening. We will use P_r as the parameter to quantify the effect of different poling conditions. To quantify the effect on piezoelectric properties we measured the effective piezoelectric coefficient ($d_{33,f}$).

Figure 2(a) shows the remnant polarization of different types of devices before and after the two poling procedures used in this study, and after prolonged cycling. The large effect of the poling on the less epitaxial devices is evident. The topic of this paper is the change of P_r in the shaded area of Figure 2(a). The differences in the final P_r level reached after poling for the different devices is discussed in Ref. [23]. Further we note the large stability of the *PLD* devices, which show no deterioration of P_r on cycling in contrast to the SG devices, which already degrade after 10^6 cycles. This is ascribed to the usage of the LNO seed layer on top of the Pt base electrode, which is expected to improve the aging properties, in the case of the Text(001) film, as has also been shown for sol–gel PZT films,[26] as well as earlier for other oxide electrodes.

Two poling procedures are investigated. In the more conventional the sample is heated up to 200 °C. Then a *dc* poling field E_{pol} is applied during the poling time t_{pol}, after which the sample is cooled down in the applied field (Fig. 1(a)). We will call this the HT-DC (high temperature, *dc* field) poling process.

Before and after poling the P_r is determined from the polarization hysteresis (P–E) loop measurement, using the ferroelectric mode of the aixACCT TF-2000 Analyzer. In this study, the P–E loop was performed using a triangular applied electric field of $E_{max} = \pm 200$ kV/cm at 1 kHz cycling frequency and room temperature (RT). The effective piezoelectric coefficient ($d_{33,f}$) is determined from the out-of-plane piezoelectric displacement of the top electrode of the thin-film capacitor, measured with

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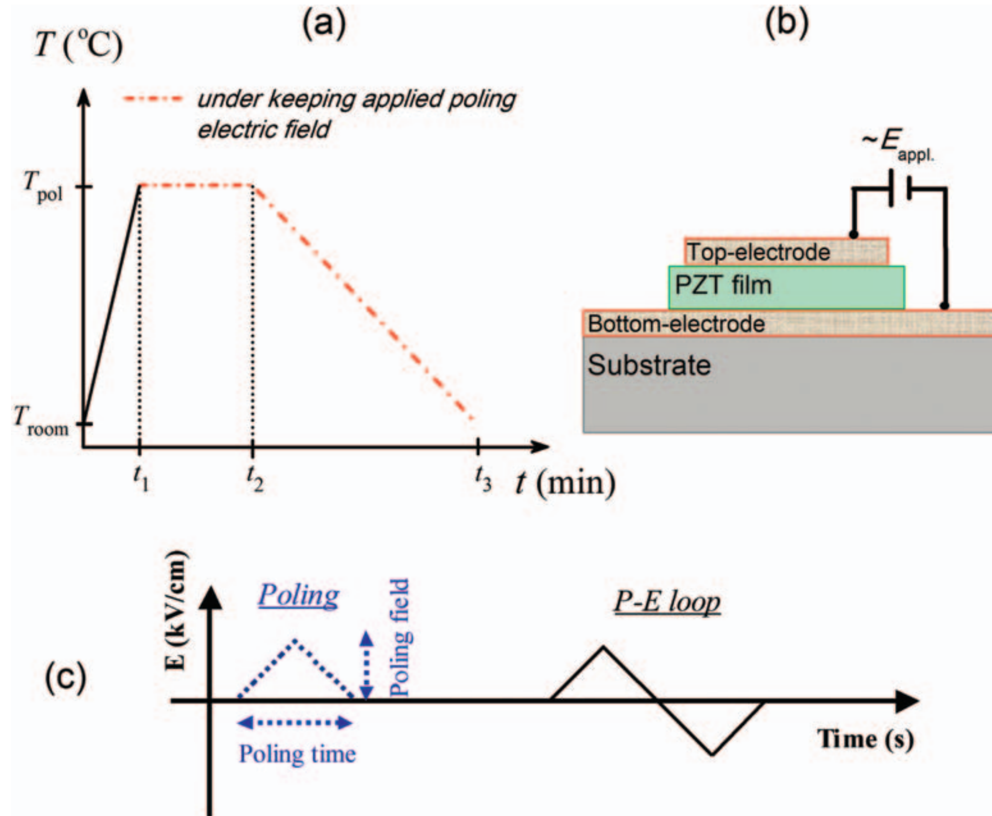

Fig. 1. (a) Time-temperature scheme of the high-temperature *dc*-electric field (HT-DC) poling process. (b) Structure of a PZT thin-film based capacitor with top and bottom electrodes. (c) Time-bias voltage scheme of the room-temperature *ac*-electric field (RT-AC) poling scheme and the bias voltage ramping during hysteresis loop measurement using the aixACCT TF-2000 ferroelectric analyzer.

a Polytech MSA-400 scanning laser Doppler vibrometer (LDV). According to the measurement principle, the $d_{33,f}$ value is defined as: $d_{33,f} = \delta/V_{ac}$, with δ the piezoelectric displacement of the thin-film capacitor and measured at an *ac* driving voltage (V_{ac}) (here a sinusoidal *ac*-voltage of 3 V or 6 $V_{peak-peak}$ was used) and at 8 kHz frequency.

It was found that P_r, measured from the P–E loop on an device that had not previously been subjected to a poling field, increases with increasing maximum applied field P_{max} and with decreasing cycling frequency (as shown in Fig. 3), indicating that already at room temperature significant poling takes place during the cycling. This was investigated further by an alternative room temperature poling process

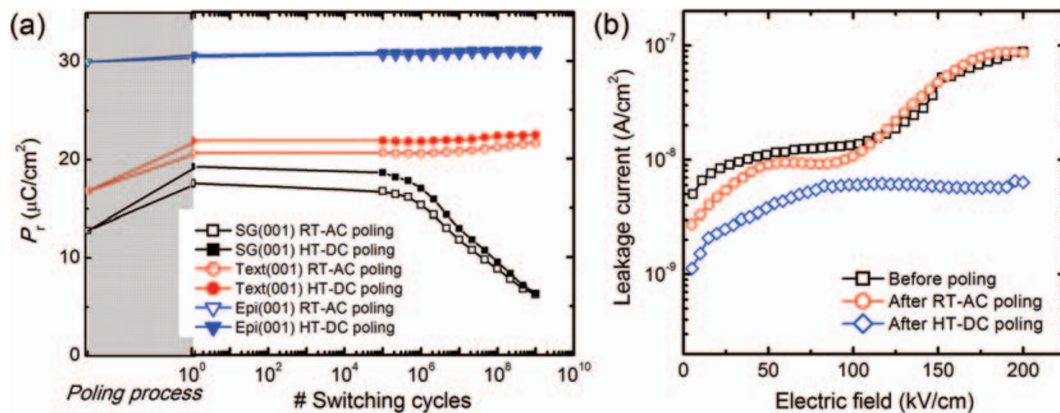

Fig. 2. (a) Remnant polarization (P_r) before and after RT-AC (400 kV/cm, 100 sec) poling (open symbols) and HT-DC (400 kV/cm, 30 min) poling (filled symbols) and after prolonged cycling. The switching cycles were performed with bipolar switching pulse of 200 kV/cm pulse height and 5 μs pulse width, and the P_r data were obtained using an *ac*-amplitude $E_{max} = \pm 200$ kV/cm and 1 kHz frequency. (b) Leakage current of SG(001) PZT device before, after RT-AC (400 kV/cm, 100 sec), and after HT-DC (400 kV/cm, 30 min) poling, respectively.

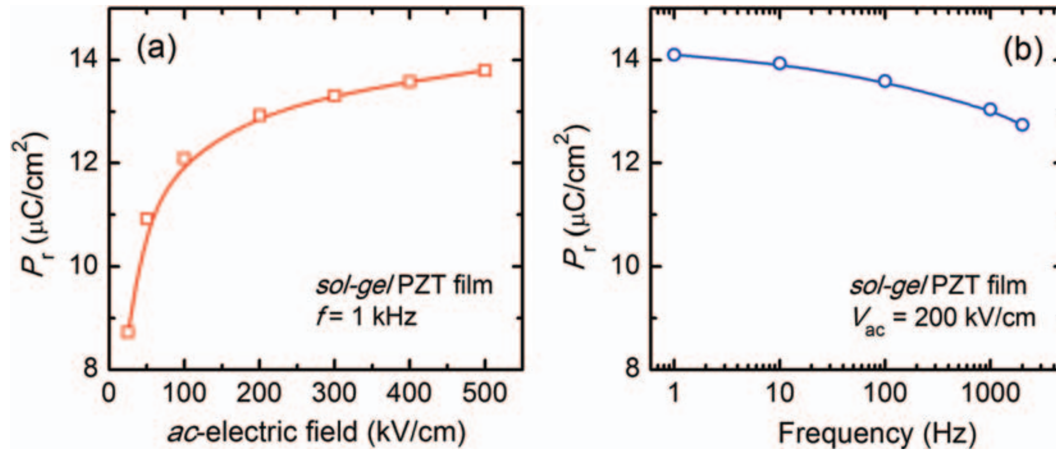

Fig. 3. Remnant polarization (P_r) of unpoled SG(001) films as a function of the measuring parameters: (a) applied maximum *ac*-electric field E_{max} and (b) cycling frequency.

(named RT-AC process) using a slow half triangular field cycle, varying the poling time (equal to a half pulse length $\tau_{pol}/2$) and pulse height E_{pol} (Fig. 1(c)). The large advantage of this process is that it can be done quickly before further characterizations of devices, without the need of a heated sample stage using the standard ferroelectric components of the aixACCT TF-2000 ferroelectric analyzer.

From the change in P_r with different poling conditions, we will deduce time constants for the poling process, which we expect to give information on the underlaying processes.

3. RESULTS AND DISCUSSION

3.1. Thermal (HT-DC) Poling Process

Figure 4 shows the effect of poling time duration (t_{pol}) and poling field (E_{pol}) on the P_r and $d_{33,f}$ values of the SG(001) and Text(001) films, where both *dc*-poling field (400 kV/cm) and poling temperature (200 °C) are kept constant. It is observed that both P_r and $d_{33,f}$ show an approximately exponentially saturating trend, with a time constant (t_{s400}) of about 30 min. We fitted P_r (Fig. 4(a)) with an exponential function of the form

$$P_r(t_{pol}, HT) = P_{r0} + \Delta P_r(1 - \exp[-t_{pol}/t_{s400}]) \quad (1)$$

Here P_{r0} is the remnant polarization value before poling, ΔP_r the maximum achievable change in remnant polarization by the polarization process, and t_{s400} the time constant for poling with a *dc* poling field of 400 kV/cm. We obtain the fitting parameters as given in Table II for the SG(001) and the Text(001) films. The time constants t_{s400} for both the SG(001) and the Text(001) films are in good approximation the same, whereas the initial polarization P_{r0} and the absolute change ΔP_r, differ significantly. The properties of the Epi(001) film do hardly change on poling (see Fig. 2(a)) and we will therefore not analyze the poling process of this film further in this paper. (Elsewhere we have discussed that the high initial quality of the Epi(001)

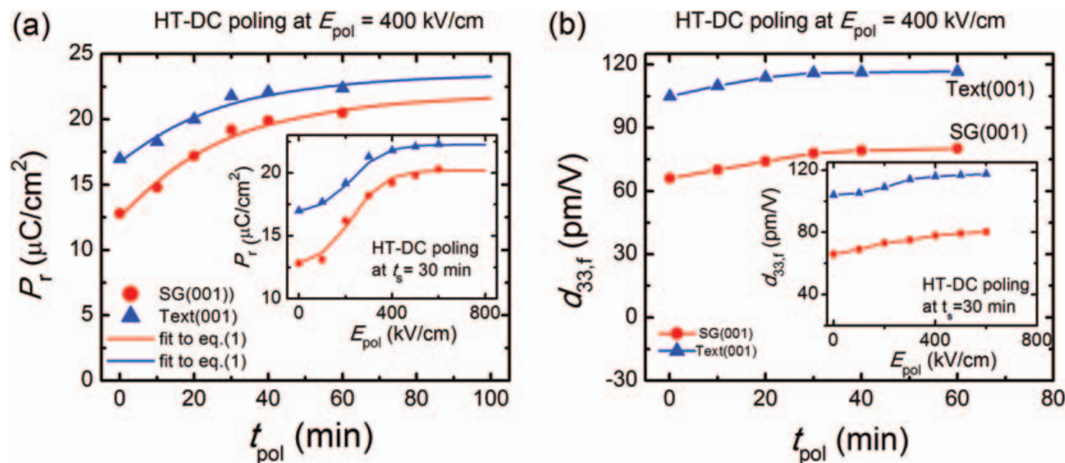

Fig. 4. (a) Remnant polarization (P_r) and (b) effective piezoelectric coefficient ($d_{33,f}$) of the SG(001) and Text(001) piezoelectric capacitors after HT-DC poling as function of poling time t_{pol} at $E_{pol} = 400$ kV/cm. The inset of Figure 4(a) gives P_r as function of polarization field E_{pol}, during $t_{pol} = 30$ min. The lines in (a) are fits according to Eq. (1); in the inset the curves are according to Eq. (1) but with time constants $t_s(E_{pol})$ determined from Eq. (3). The lines in (b) are guides to the eye.

Table II. Fit parameters describing the change of the remnant polarization and the time constants of the RT-AC and HT-DC poling processes.

	RT-AC poling			HT-DC poling		
	P_{r0} (μC/cm^2)	ΔP_r (μC/cm^2)	t_{s400} (sec) [min]	P_{r0} (μC/cm^2)	ΔP_r (μC/cm^2)	t_{s400} (sec) [min]
Fit to $P_r(t_{pol}, E_{pol} = 400$ kV/cm)						
SG(001)	12.8	5.6	59 [1.0]	12.5	9.4	1657 [27.6]
Text(001)	16.7	5.8	111 [1.8]	16.7	6.7	1627 [27.1]
Epi(001)	30.0	0.4	–	30.0	0.7	–

Fit to $t_s(E_{pol})$

E_{s01} (kV/cm)	t_{s01} (sec) [min]	E_{s02} (kV/cm)	t_{s02} (sec) [min]	$t_{s\infty}$ (sec) [min]	E_{s0} (kV/cm)	t_{s0} (sec) [min]	$t_{s\infty}$ (sec) [min]
17.6	12719 [212.0]	88.3	1190 [19.8]	44.3 [0.7]	73.5	50510 [841.8]	1037 [17.3]

films is ascribed to the high crystalline quality, especially the much reduced number of defect charges in the grain boundaries as compared to the SG(001) and Text(001) films[23]).

The influence of poling time and poling field on the $d_{33,f}$ values are shown in Figure 4(b). Similar trends as for P_r are observed although the relative change in $d_{33,f}$ on poling is much less: both P_r and $d_{33,f}$ values increase with increasing poling field and saturate for $E_{pol} > 400$ kV/cm. $d_{33,f}$ is measured at a fairly large *dc* bias field of $E_b = 60$ kV/cm, hence more towards saturation, where domain wall motion hardly contributes to its value. In that case, $d_{33,f}$ can be estimated as $d_{33,f}(E_b) = 2Q_{11,\mathrm{eff}}\varepsilon_0\varepsilon_{33}(E_b)P_3(E_b)$, where $Q_{11,\mathrm{eff}}$, ε_0, ε_{33} and P_3 are the effective electrostrictive constant, dielectric constant of vacuum, relative dielectric constant of film and out-of-plane polarization, respectively.[27] With improving P_r on poling, also $P_3(E_b)$ increases, but simultaneously $\varepsilon_{33}(E_b) = (\partial P/\varepsilon_0\partial E)_{E_b}$ decreases. The net effect is that $d_{33,f}$ improves relatively less on poling than P_r.

3.2. Room Temperature (RT-AC) Poling Process

Figure 5 shows the same quantities P_r and $d_{33,f}$ for samples poled by the RT-AC process. The fitting parameters are given in Table II. There are two obvious and significant differences with the results from the HT-DC poling process: (i) P_r saturates at a somewhat lower value than using the HT-DC poling process, hence $\Delta P_r(RT) < \Delta P_r(HT)$ and (ii) the timescales of the RT-AC process ($t_{s400} = 1$ min) are much shorter than of the HT-DC process ($t_{s400} = 28$ min). The latter is quite surprising, since one would expect that poling at elevated temperatures is more efficient, since diffusion processes are faster.

3.3. Time Constants of the Poling Processes

To investigate the surprising difference in timescales between the two poling processes we extract the time constants from the field dependent measurements by rewriting Eq. (1) as:

$$t_s(E_{pol}) = \frac{-t_{pol}}{\ln[1-((P_r(t_{pol}, E_{pol}) - P_{r0})/\Delta P_r)]} \quad (2)$$

Thus one obtains the poling field dependence of the poling time constant t_s, as depicted in Figure 6 for both the SG(001) and Text(001) films, subjected to the HT-DC and RT-AC poling processes. The following observations are made:

(i) the time constants for the SG(001) and Text(001) films are the same;
(ii) the time constants of the HT-DC process are 4–23 times larger than in the RT-AC poling process, increasing with applied field;
(iii) t_s decreases rapidly with increasing E_{pol}, and saturates above approximately 400 kV/cm;
(iv) the curve of $t_s(E_{pol})$ of the RT-AC process shows two kinks, whereas that of the HT-DC process shows only one.

The dependence $t_s(E_{pol})$ is fitted with a simple series of exponential functions:

$$t_s(E_{pol}, T) = \tau_{s\infty}(T) + \sum_{i=1,2} \tau_{s0,i}(T)\exp(-E_{pol}/E_{s0,i}) \quad (3)$$

For the HT-DC process, a single exponential term is sufficient to describe the data, whereas two terms are needed for the RT-AC process. The fit parameters are given in Table II.

The physical picture behind this mathematical description is that there are one or more electrical field activated processes, giving rise to the field dependent exponential terms, in series with a fast field independent process (with temperature dependent time constant $\tau_{s\infty}(T)$), as schematically shown in Figure 7.

3.4. Final Remnant Polarization

A second observation is that the HT-DC process results in a larger final remnant polarization, hence $\Delta P_r(HT\text{-}DC) > \Delta P_r(RT\text{-}AC)$, after prolonged poling time than the RT-AC process (see Table II). Thus, although the RT-AC poling process is faster in increasing the remnant polarization it appears to be less effective than the HT-DC process. As the final polarization obtained depends on the reduction of the screening either by removing screening charges or by rearranging their configuration in such a way that their

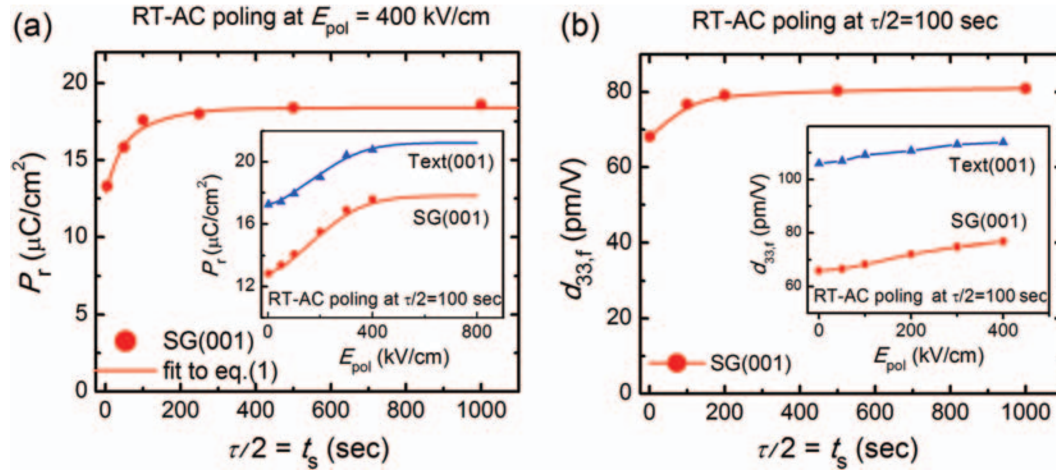

Fig. 5. (a) Remnant polarization (P_r) and (b) effective piezoelectric coefficient ($d_{33,f}$) of the SG(001) and Text(001) piezoelectric capacitors after RT-AC poling as function of poling time t_{pol} at $E_{pol} = 400$ kV/cm. The inset of (a) gives P_r as function of polarization field E_{pol}, during $t_{pol} = \tau/2 = 100$ sec. The lines in (a) are fits according to Eq. (1); in the inset the curves are according to Eq. (1) but with time constants $t_s(E_{pol})$ determined from Eq. (3). The lines in (b) are guides to the eye.

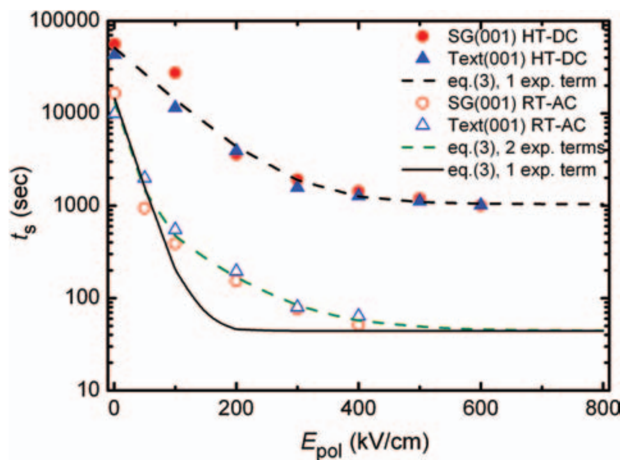

Fig. 6. Time constant $t_s(E_{pol})$ of the HT-DC and RT-AC poling process as function of the applied poling field. The lines are fits with Eq. (3). The fit parameters are given in Table II.

screening effect is reduced, one must conclude that the RT-AC process only removes part of the screening. This is supported by the observation that the leakage current of the SG(001) device after the RT-AC poling is only slightly reduced as compared to before the poling process. This in contrast to the HT-DC poling process that reduces the leakage current significantly. The fact that the time constants are also very different between both processes, suggests that in the case of the RT-AC poling process mainly screening charge rearrangement takes place, which does not require long charge diffusion times. In the case of HT-DC poling the screening charges are most likely removed in the poling process, accounting for the long (diffusion) poling times involved.

3.5. Discussion

We have assumed that the change in remnant polarization due to the poling process is caused by

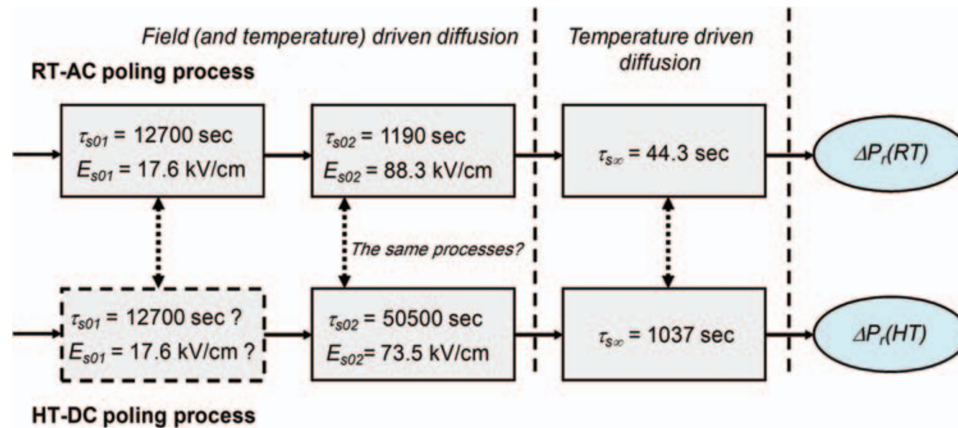

Fig. 7. Time constants and energy barriers of different terms in the expansion of the poling time constant t_s, for the RT-AC and the HT-DC poling process. The different blocks indicate possibly different processes. The dashed block may be present in the HT-DC poling process.

rearrangement and/or removal of screening charges that are predominantly present in the GBs of the PZT films. It seems obvious that with increasing field strength these charges can be removed more quickly, causing the decrease of the poling time with increasing field.

The limiting process for $E_{pol} > 400$ kV/cm is field independent, but is clearly temperature dependent. Surprisingly the HT-DC process shows a larger high field time constant than the RT-AC process. For a one-dimensional diffusion process the average distance x a diffusing particle travels in time t is given by $\langle x^2 \rangle = 2Dt$, where D is the diffusion constant, given by $D = A(T)\exp[-E_a(T)/kT]$; E_a is the (temperature dependent) potential barrier for migration, k the Boltzmann constant and $A(T)$ a prefactor that may be temperature dependent. We may assume that the characteristic poling time t_s can be estimated by $t_s \approx L^2/2D$, where L is the film thickness. It then follows from the ratio of time constants at HT and RT that $E_{a,HT} = (473/300)E_{a,RT} + 473kb'$, where $b' = b - \ln(A(RT)/A(HT))$ and $t_{s\infty}(HT)/t_{s\infty}(RT) = a = \exp(b)$, with $b = 3.15$. Assuming that the prefactors are approximately equal it is found that the barrier height at elevated temperature is higher than at room temperature by the term $473kb' = 0.13$ eV and increasing proportionally to $E_{a,RT}$. This is somewhat surprising, since one would expect that the barrier for defect diffusion is lower at higher temperatures, due to lattice expansion.[28] We speculate that the opposite finding is due to the fact that the film is clamped to the Si substrate. Due to the difference in thermal expansion, the film becomes increasingly in plane tensile strained with decreasing temperature, 'opening' up the grain boundaries and hence facilitating defect diffusion along the interfaces formed by the GBs.

Although it is not immediately obvious that one can assume that the under laying diffusion process described by (t_{s02}, E_{s02}) of the HT-DC and the RT-AC poling procedures are the same, this seems probable since the energy constants E_{s02} involved are approximately equal. The difference between the coefficients t_{s0i} is attributed to the same effect that explains the temperature dependence of $t_{s\infty}$. It appears that at the elevated temperature of the HT-DC poling process the charge transport process (t_{s01}, E_{s01}), is not present or is dominated by the process (t_{s02}, E_{s02}). The latter would imply that the coefficient τ_{s01} not scales, at least not to the same degree, with temperature as $\tau_{s\infty}$.

The final P_r value obtained by the RT-AC process is less than that reached by the HT-DC poling process. This implies that the screening is also different. One can decrease the screening arising from charges in GBs by removing the charges, but also by aligning the charges in such a way that the polarization in the adjacent grains can rotate more towards the film normal. However, in the latter case the defect sites, associated with these charges are still present and are likely to constitute leakage conduction paths between the top and bottom electrodes. This is then expected to show up in differences in the leakage current, being strongly reduced if the charges are removed. This is indeed what is observed: in the case of RT-AC poling the leakage current is only slightly affected by the relatively short poling process (reduction with factor 2–3, see Fig. 2(b)), but for the HT-DC poling process the leakage current is much stronger reduced. For (110) oriented PZT films on Si a reduction in the leakage current by a factor of 50 after prolonged P–E loop cycling (which is comparable to prolonged RT-AC poling) was reported.[25] It appears that this charge redistribution in the GBs is very stable on continuous cycling, considering the observation that P_r does not decrease up to 10^9 cycles. The decrease in P_r for the case of the SG(001) devices is ascribed to the presence of the Pt electrodes. It is well known that devices with metallic electrodes easily degrade.

The present study allowed us to draw a more detailed picture of the physical mechanisms and changes in the material due to poling. The picture drawn also qualitatively explains the results given in literatures.[16–19] In these cases, regardless of the quality of the film or deposition technique the high(er) temperature poling gives a better result. Longer room temperature *ac*-poling, *ac*-pulses,[16,17] and increased *ac*-field[18] also improves the results. In our case we find that devices with a pure metal base electrode show fatigue, regardless of the poling procedure, whereas Kohli et al.[16] appear to find this only for the room-temperature *ac*-poled devices. The difference might be that in their study the high-temperature *dc*-poled samples show a large build-in field bias after poling, which in some way may protect the device from fatigue.

An important difference between what we named RT-AC poling and room temperature *ac*-poling in literature, is that in our case we use a single, unipolar *ac* pulse, whereas in literature bipolar pulses are used. It would be interesting to be able to distinguish the effect of temperature difference from that of the unipolar/bipolar character of the poling process, by also systematically studying also the effect of room-temperature *dc*-poling (although our unipolar, single pulse RT-AC poling process is very close to such a process) and room-temperature and high temperature bipolar *ac*-poling on the same series devices. The effect on the time constants involved may shed more light on the charge displacement processes involved. Further we note that here as well as in in the literature discussed above, all thin films are made on Si substrates, which excludes possible differences due to different substrate expansion. Finally we note the importance of the processing techniques used to structure devices, on the properties of the film and their sensitivity to poling, as is clearly shown by Kobayashi et al.[19] This sensitivity seems to be related to the processes used to structure the underlying SiO_2, Si, and buried Si oxide layers, since these processes are added to the usual wet etching steps for defining the capacitor devices used in this paper.

4. CONCLUSIONS

The ferroelectric and piezoelectric properties of textured sol–gel, textured *PLD* and epitaxial *PLD* PZT thin-films, deposited on Pt/Ti/SiO_2/Si and SRO/STO/Si substrates respectively, were investigated after poling under high-temperature *dc*-electric field (HT-DC) and room-temperature *ac*-electric field (RT-AC) conditions. The increase of the remnant polarization P_r and effective piezoelectric coefficient $d_{33,f}$ was determined as function of the poling conditions, specifically the poling time and the poling field. The polarization and piezoelectric coefficient changes are interpreted as being due to changes in the screening of the polarization by rearrangement and/or removal of the screening charges from the grain boundaries. The time constants associated with these processes have been obtained.

We arrived at the following conclusions:

(i) Poling at room temperature is obtained at a much faster rate than at higher temperature.

(ii) For poling fields less than 400 kV/cm the poling process is strongly driven by the applied field and time constants involved in the poling process depend exponentially on the applied field.

(iii) The effect of the poling is less strong in the case of room temperature poling, resulting in a lower final remnant polarization.

(iv) The leakage current is hardly reduced in the case of RT-AC poling.

(v) The points (iii) and (iv) are interpreted as indications that in the case of RT-AC poling, there is mainly rearrangement of the charges in the GBs, such as to reduce their screening effect, whereas in the case of HT-DC poling also a large fraction of the screening charges is removed from the GBs.

(vi) Practical working values for the high temperature poling process are a *dc*-electric field of 400 kV/cm, during 30 min and a poling temperature of 200 °C, irrespective of the type of device used.

(vii) In combination with the ferroelectric components in the aixACCT TF-2000 ferroelectric analyzer, a room-temperature poling process under *ac*-electric field was introduced, that produces only slightly reduced remnant polarization values as compared to the high-temperature poling process. However, this process allows a rapid poling procedure that can be used in the ferroelectric analyzer before device characterization. It may especially be useful in the improvement of the properties of practical ferroelectric film devices, like membranes and cantilevers, where a high-temperature treatment may not always be possible

Acknowledgments: This work has been financially supported by the Vietnam's National Foundation for Science and Technology Development (NAFOSTED) under Grant number 103.02-2011.43, by the Dutch GO EFRO-funded "I2I" program (Innovation 2 Industrialization for advanced micro- and nanosystems), and by NanoNextNL, a micro and nanotechnology consortium of the Government of the Netherlands and 130 partners.

References and Notes

1. D. Maraldo, K. Rijal, G. Campbell, and R. Mutharasan, *Anal. Chem.* 79, 2762 (**2007**).
2. Q. Cui, C. Liu, and X. F. Zha, *Microfluid. Nanofluid.* 3, 377 (**2007**).
3. T. Alava, F. Mathieu, L. Mazenq, C. Soyer, D. Remiens, and L. Nicu, *J. Micromech. Microeng.* 20, 075014 (**2010**).
4. F. Akasheh, T. Myers, J. D. Fraser, S. Bose, and A. Bandyopadhyay, *Sens. Act. A* 111, 275 (**2004**).
5. H. S. Choi, J. L. Ding, A. Bandyopadhyay, M. J. Anderson, and S. Bose, *J. Micromech. Microeng.* 18, 025037 (**2008**).
6. J. Baborowski, S. Hediger, P. Muralt, and C. Wuetrich, *Ferroelectrics* 224, 283 (**1999**).
7. H. Yagubizade, M. Darvishi, Y.-Y. Chen, M. D. Nguyen, J. M. Dekkers, R. J. Wiegerink, M. C. Elwenspoek, and N. R. Tas, *Appl. Phys. Lett.* 102, 063509 (**2013**).
8. D. J. Laser and J. G. Santiago, *J. Micromech. Microeng.* 14, R35 (**2004**).
9. K. S. Yun and E. Yoon, MEMS/NEMS Handbook Techniques and Applications, edited by T. L. Cornelius, Springer-Verlag, New York (**2006**), p. 121.
10. P. Muralt, *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* 47, 903 (**2000**).
11. A. D. Prewitt and J. L. Jones, *Ferroelectrics* 419, 39 (**2011**).
12. D. Damjanovic, *Rep. Prog. Phys.* 61, 1267 (**1998**).
13. H. Thomann, *Adv. Mater.* 2, 458 (**1990**).
14. D. L. Polla and L. F. Francis, *Annu. Rev. Mater. Sci.* 28, 563 (**1998**).
15. N. Izyumskaya, A.-I. Alivov, S.-J. Cho, H. Morkoç, H. Lee, and Y.-S. Kang, *Crit. Rev. Solid State Mater. Sci.* 32, 111 (**2007**).
16. M. Kohli, P. Muralt, and N. Setter, *Appl. Phys. Lett.* 72, 3217 (**1998**).
17. T. Ogawa and K. Nakamura, *J. European Ceram. Soc.* 21, 1391 (**2001**).
18. M. Nakajima, H. Nakaki, Y. Ehara, T. Yamada, K. Nishida, T. Yamamoto, M. Osada, and H. Funakubo, *Appl. Phys. Lett.* 97, 181907 (**2010**).
19. T. Kobayashi, N. Makimoto, T. Oikawa, A. Wada, H. Funakubo, and R. Maeda, *IEEE 26th International Conference on Micro Electro Mechanical Systems* (*MEMS*), Taipei, Taiwan (**2013**), p. 413
20. M. D. Nguyen, Ferroelectric and piezoelectric properties of epitaxial PZT films and devices on silicon, [dissertation], University of Twente, The Netherlands (**2010**).
21. $SrTiO_3$ buffered Si substrates are provided by Professor Schlom DG, Cornell University, USA.
22. M. D. Nguyen, C. T. Q. Nguyen, T. Q. Trinh, T. Nguyen, T. N. Pham, G. Rijnders, and H. N. Vu, *Mater. Chem. Phys.* 138, 862 (**2013**).
23. E. P. Houwman, M. D. Nguyen, M. Dekkers, and G. Rijnders, *Sci. Technol. Adv. Mater.* 14, 045006 (**2013**).
24. A. J. Moulson and J. Herbert (eds.), Electroceramics, Chapman and Hall, New York (**1990**).
25. M. Dekkers, M. D. Nguyen, R. Steenwelle, P. M. te Riele, D. H. A. Blank, and G. Rijnders, *Appl. Phys. Lett.* 95, 012902 (**2009**).
26. M.-S. Chen, T.-B. Wu, and J.-M. Wu, *Appl. Phys. Lett.* 68, 1430 (**1996**).
27. M. D. Nguyen, M. Dekkers, E. Houwman, R. Steenwelle, X. Wan, A. Roelofs, T. Schmitz-Kempen, and G. Rijnders, *Appl. Phys. Lett.* 99, 252904 (**2011**).
28. R. J. D. Tilley (ed.), Defects in Solids, John Wiley & Sons Inc., New Jersey (**2008**).