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Zapping thin film transistors

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Abstract

It was expected that hydrogenated amorphous silicon thin film transistors (α-Si:H TFTs) behave similarly to crystalline silicon transistors under electrostatic discharge (ESD) stress. It will be disproved in this paper. This knowledge is necessary in the design of the transistors used in a ESD protection circuit. The goal of this paper was to identify and to model failure under ESD zap. The drain of grounded gate TFTs has been stressed applying repeated square voltage pulses of different duration (100 ns to 10 s). The evolution and the mechanisms of the pre-breakdown degradation will be presented and discussed. Finally, the temperature distribution across an α-Si:H TFT under applied stress will be simulated by means of coupled electro-thermal simulations.

1. Introduction

Thin film transistors (TFTs) are indispensable in large area electronics. Hydrogenated amorphous silicon (α-Si:H) TFTs, or polysilicon TFTs on large glass substrates are equivalent to the crystalline MOS transistors in the integrated circuits. They are used in processes where crystalline silicon could not be of any use, such as for low temperature processes (~100 °C), or for deposition over a large area (1 m^2). In active-matrix liquid crystal displays (AM LCDs), amorphous silicon TFTs are most often used like switching devices inside each pixel in the display. The use of a TFT in this way was introduced more then 20 years ago [1]. The α-Si:H TFTs are often built on glass substrate. That is a necessity in display industry, or the light could not pass through the display. As glass has relatively low melting point (~600 °C), it means that all technology processes of TFT deposition are temperature limited.

The channel material of TFTs is amorphous silicon. Amorphous silicon thin films are commonly produced using a glow discharge technique, also known as plasma enhanced chemical vapour deposition (PECVD). A silicon rich gas (usually SiH_4) is admitted to a vacuum reactor chamber. Then discharge is initiated and maintained by an electric field between two parallel plates [2]. The hydrogen was recognised as being essential for tightening up the unpaired valence electrons that would otherwise lead to electronic defect states. The main advantages of α-Si:H are that it can be deposited over a large area and at the low temperature [3]. The disadvantage is that electron mobility is poor, which is due to the disorder in an amorphous structure. Therefore the conductivity, which is related to the electron mobility μ and the density of states (DOS) in the band gap $N(E)$ is very poor as well. The problem is up to some level lessened introducing the proper amount of hydrogen into amorphous silicon. Hydrogen atoms are small and can move easily through the network of amorphous silicon. In that way some of the dangling silicon bonds are compensated [4], making the density of gap states lower and the electron mobility higher. The conductivity of α-Si:H is determined from transport in the extended states at the band edge. The normal (dark) conductivity of α-Si:H is strongly n-type.

Working of α-Si:H TFTs is basically similar to crystalline MOS metal-oxide-semiconductor (MOS) devices. The only difference is that instead of oxide, mainly

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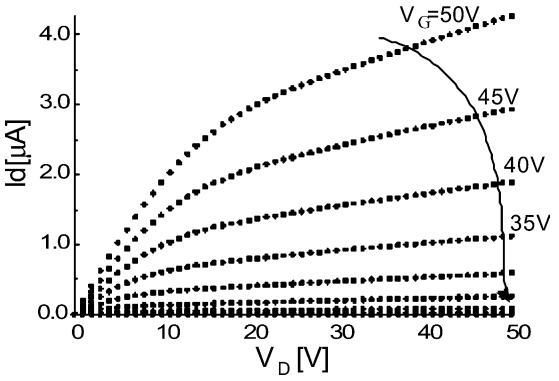

Fig. 1. A typical set of measured $I_D(V_D)$ characteristics of an α-Si:HTFT.

silicon nitride is used as the gate dielectric, and instead of crystalline, amorphous silicon is used as the channel material. The principle of operation is still the same as in crystalline MOS transistors. Therefore they can be well described by standard MOS equations.

To give an example of TFTs working, a typical set of measured $I_D(V_D)$ characteristics for a top-gate TFT with the channel dimensions $L = 6$ μm and $W = 100$ μm, under different voltages applied on the gate $V_G = 20$–50 V, is shown in Fig. 1.

It can be seen in Fig. 1 that there are two distinguished regions of working: liner and saturation. It also can be noticed that current in the saturation regime is not flat. That is particularly expressed for short-channel TFTs (in this investigation all TFTs with $L < 9$ μm are considered as short-channel TFTs) and is not included in the described model.

2. TLM experiments

In order to study breakdown behaviour under electrical bias the following measurements have been carried out. Unfortunately the transmission line model (TLM) system as it is could not be used properly in the classic way for α-Si:H TFTs, as their on-resistance is much higher than 50 Ω. The value of the on-resistance varies, but it is in order of MΩ. Another problem is that the current level is very low. Even the current under high electrostatic discharge (ESD) stress (few hundreds of Volts) is too low to be measured by the current transformer of the oscilloscope (sensitivity of which is 5 mA). Only the peak of the drain current can be measured. Also, the drain current during the breakdown can be read out. That is shown in Fig. 2. It also should be noted that the gate and the source current during the breakdown are not known, so the path of the breakdown current can not be established by this measurement. The voltage data on the drain could be easily measured by the oscilloscope.

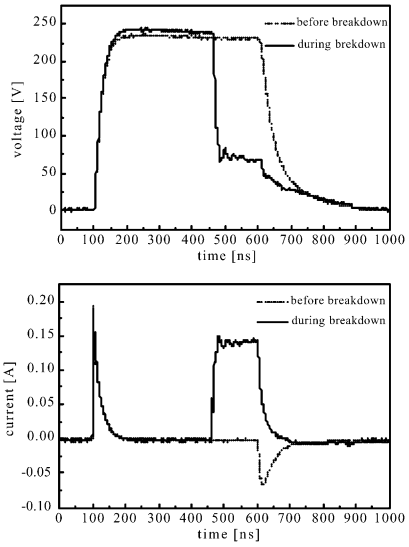

Fig. 2. Shape of current and voltage TLM pulses monitored on the oscilloscope before and during breakdown.

Therefore the standard TLM measurement system had to be changed in order to make up for the lost of the data (current measurements) in the following way. Between each two TLM stress pulses, the transfer characteristic $I_D(V_D)$ of the TFT was monitored by the parameter analyser. From the transfer characteristics important electrical parameters like threshold voltage, subthreshold slope were extracted. From the behaviour of the transfer characteristic the degradation flow was estimated. Another important parameter that was measured by the TLM is the breakdown voltage. The measurement of the TLM voltage showed that TFTs give different response to the TLM stress then crystalline MOS devices. The TLM voltage was increased up to the breakdown and it did not go into the snapback. After the breakdown the TFTs were already thermally damaged (this point is equivalent to the second breakdown when reading classic TLM curve for crystalline MOS devices).

In the experiments, the TLM voltage pulse generator was typically set up with a pulse width of 100, 300, 500 ns and 1 μs. These are pulse durations that in comparison with the typical pulse length used in standard ESD investigations on ICs must look rather long. The reason for choosing such long pulses is that in the case of α-Si:H TFTs the RC time of the device is rather long (∼100 ns), as shown in Fig. 2, due to large resistance of amorphous silicon. Therefore short pulse measurements would not always give complete results. The reason for choosing to experiment with different pulse durations is to investigate if power dissipation given by $P(t) = i(t)v(t)$ is a parameter in breakdown or it is only stress voltage level. A number of experiments repeated for different pulse widths are investigated in [5].

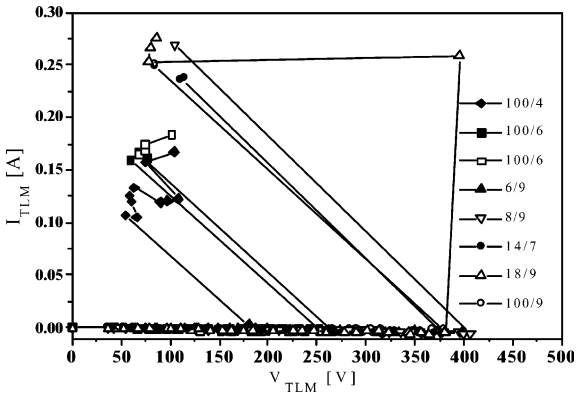

Fig. 3. TLM curves show different breakdown voltages for TFTs with different W/L ratio.

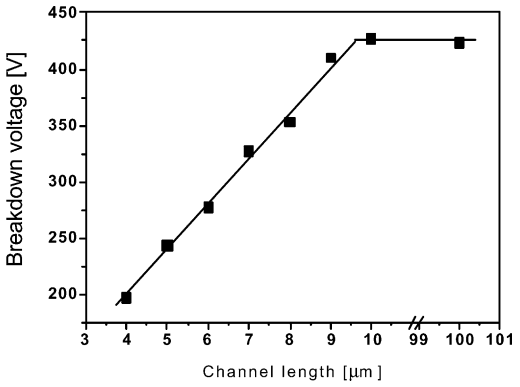

Fig. 4. The mean value of the breakdown voltage versus the channel length.

2.1. Breakdown voltage due to TLM

The breakdown voltage under TLM pulse is defined as the voltage at which the drain current increases sharply and accompanied with a decrease in the drain voltage. In Fig. 3 are shown some typical TLM curves measured for the TFTs with different dimensions.

The results presented in this section concern two important subjects related to TLM stress induced breakdown:

- breakdown voltage versus channel width and channel length
- breakdown voltage versus pulse length.

An overview of the TFTs with a variety of the channel length and width tested by the TLM measurement system is given in Table 1.

Table 1
Breakdown voltages in samples with different channel lengths

W/L	Sample A1	Sample B1	Sample C1	Mean value
100/10	420	450	410	427
100/100	430	440	400	423
8/9	430	430	400	420
4/9	430	430	400	420
10/9	420	420	400	413
18/9	410	410	400	407
6/9	420	420	390	410
100/9	410	400	370	393
100/8	370	370	320	353
14/7	350	330	300	327
100/6	280	280	260	277
10/5	260	240	230	243
100/4	210	190	190	197

From the data shown in Table 1 it can be quickly concluded that the breakdown voltage depends on the channel length and does not depend on the channel width (from the fact that the TFTs with the constant channel length $L = 9$ μm and with different channel widths did not show remarkable variations of the breakdown voltage). The dependence of the breakdown voltage versus the channel length, which is extracted from the data shown in Table 1, is separately plotted in Fig. 4.

Fig. 4 shows that the breakdown voltage depends almost linearly on the channel length for the short channel TFTs. That stands for the channel lengths of $L < 10$ μm. For long channel TFTs ($L \geqslant 10$ μm) the breakdown voltage stays constant with an approximate value of $V_{BR} = 425$ V.

Beside the breakdown voltage measurements in the sample consisting of the TFTs with W and L variations, another experiment is carried out in order to get a better insight in the breakdown physics. The breakdown voltage was measured for different duration of the TLM stress pulse. Differences in breakdown voltage due to difference in channel lengths/batches, mask possible difference in breakdown voltages due to different pulse lengths. Therefore for the following experiments only TFTs were used with constant W/L ratio (18/9). In Table 2 the breakdown voltages of tested TFTs are listed. These TFTs were stressed with TLM pulses with pulse lengths of 100, 300, 500 ns and 1 μs. It should be noted that the large (~100 ns) rise/fall time of the TFT has to be taken into account.

The data from Table 2 are graphically presented in Fig. 5. The experimental data show that the breakdown voltage lowers when the TLM stress time increases. Unfortunately the number of data points in the Fig. 5 is not enough for a reliable extrapolation.

The conclusion that we can draw from the experiments is that the breakdown voltage apparently depends

Table 2
Breakdown voltages of the TFTs with $W/L = 18/9$ under the TLM with different pulse lengths

	100 ns	300 ns	500 ns	1 μs
Sample T1	430	420	400	380
Sample T2	430	430	400	380
Sample T3	470	*x*	380	360
Sample T4	470	*x*	370	360
Sample T5	*x*	*x*	380	360
Mean value	450	425	386	368

x = no data.

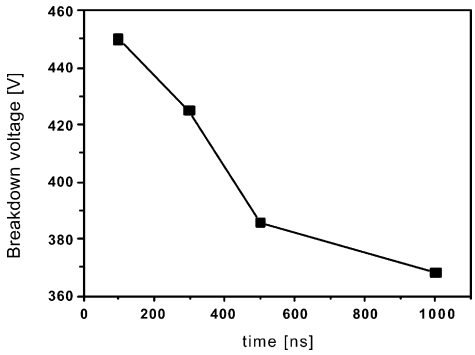

Fig. 5. The mean value of the breakdown voltage versus the TLM stress.

on the channel length and does not on the channel width. In the TFTs with the channel length $L < 10$ μm, so called short-channel effects, similar as in the standard crystalline devices, occur and the breakdown voltage is considerably lower. The current flow is dependant on the W/L ratio, but also on the channel length itself, due to punch through effect, which will be discussed later on. It is also shown that the breakdown voltage depends on the stress time. As the stress time is increased, the breakdown voltage is decreased. These results suggest that electrical breakdown is in the end a thermal process. The heat generation is due to the current flow and it depends on the thermal properties of the materials used, amorphous silicon, SixNy and glass. The time dependence suggests also that a high power dissipation develops (Wunch and Bell model [6]).

2.2. Pre-breakdown degradation due to TLMs

If a TLM stress is higher than the "threshold of degradation" ($V_{\mathrm{THDEG}} \cong 180$ V), the transfer characteristic, monitored between two TLM stress pulses, starts to change. The transfer characteristic shifts to the negative side and the slope of the characteristic increases. A set of $I_{\mathrm{D}}(V_{\mathrm{G}})$ curves monitored in this way is shown in Fig. 6.

In literature, two mechanisms have been found to contribute to degradation effects in α-Si:H TFTs: trapping of charge in the gate dielectric and change in the DOS of the amorphous silicon itself. Which of this two set in during ESD stress will be investigated further in this section.

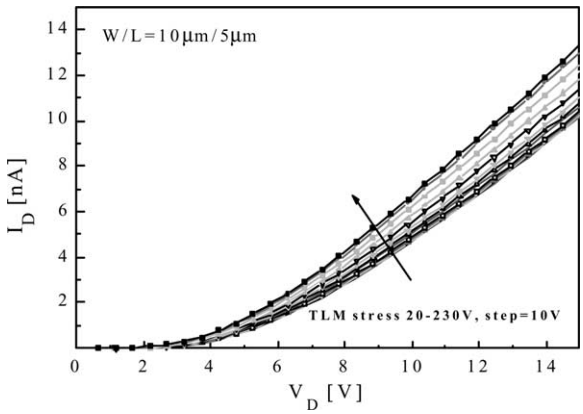

Fig. 6. Transfer characteristics monitored during the TLM series.

It is clear that change in the drain current might be due to:

- the change in the threshold voltage, which can be due to the charge accumulation in the dielectric or at the interface dielectric/amorphous silicon,
- due to the change in the electron mobility. The electron mobility μ_n is thermally activated with an energy given by the width of the tail state distribution, not by $E_{\mathrm{C}} - E_{\mathrm{F}}$ [7]:

$$\mu_n = \mu_0 N_{\mathrm{c}} \frac{kT}{n} \mathrm{e}^{-(E_{\mathrm{a}}/T)} \tag{1}$$

where μ_0 is the extended state electron mobility, N_{C} is the DOS at the mobility edge, n is the total electron density and E_{a} is the activation energy which reflects the tail state distribution of the α-Si:H. Therefore the electron mobility might change if the temperature of the TFT is changed.

The presence of the interface states can be read from the subthreshold slope. The sub-threshold slope is defined by:

$$S = \frac{\mathrm{d}V_{\mathrm{D}}}{\mathrm{d}(\log I_{\mathrm{D}})} \tag{2}$$

The change in the subthreshold slope will help us to distinguish whether the charges that are able to change the threshold voltage are located in the gate dielectric (which produce no change in the subthreshold slope) or at the gate dielectric/amorphous silicon interface (which will produce change in the subthreshold slope).

Threshold voltage (V_T) is derived from the intersection of the slope of linear characteristic with x-axis. It is found that once the TLM voltage exceeds the threshold of degradation, V_T decreases linearly with applied voltage. The peak decrease in the threshold voltage is just before breakdown. The breakdown voltage and TLM stress that a TFT can stand depends on the channel dimensions, as explained in 2.1. On another hand, if the same amount of TLM stress is applied to TFTs with different channel dimensions, the threshold voltage shift shows the same dependence with the channel dimensions like the breakdown voltage. An overview of the V_T shift for TLM stress of 500 ns and transistors with different channel dimensions is shown in Fig. 7 [8]. Appearance of the negative shift of V_T can be connected with both mechanisms, the creation of positive states in the amorphous silicon layer, or near the interface and due to the charge trapping in the gate dielectric.

Besides V_T, the transconductance is also derived from the slope of the linear transfer characteristic. An increase of electron mobility is assumed and will be further explained by the analysis that follows. In α-Si TFTs, the main carriers are electrons whose room-temperature mobility is typically 0.3–0.6 cm^2/Vs. The dependence of the mobility with temperature is given by Eq. (1). We suppose that shift of V_T and shift of μ are independent processes, although they can be correlated, as a shift in μ will almost certainly change V_T. We assume that these positive interface states help to move the current flow closer to the interface α-Si/SiN and further from the bottom interface of α-Si/SiO_2, where it is more confined in higher mobility part of the band- gap. There is also another possible mechanism which can help to explain observed change in the transfer characteristics slope, assuming that electron mobility is constant and that created positive interface states attract an inversion layer that extends the drain, resulting in a shortening of the effective length of the transistor [9]. To avoid this uncertainty, the slope change will be presented through a relative change of transconductance:

$$g_m = \frac{dI_D}{dV_G} = \frac{W}{L}\mu C V_{DS} \tag{3}$$

Stepped lowering of V_T implies stepped accumulation of positive charges. Irreversibility of this degradation is observed and confirmed by means of repeated TLM experiment under the same conditions. To investigate whether the ESD induced degradation is permanent, repeated TLM stresses were applied in the following way. In the first TLM series, TLM stress (V_{TLM}) is stepped from 20 V up to 250 V, when the series is stopped. After 100 min of pause (with all electrodes grounded) the second TLM series is repeated (V_{TLM} = 20–250 V). This time both V_T and g_m stay constant during TLM stress. After pause of 1000 min the third TLM series is applied (V_{TLM} was increased from 20 V up to dielectric breakdown). Same as in the previous case, no degradation is found for voltages up to 250 V. Finally, when $V_{TLM} > 250$ V, then degradation of V_T and g_m continues with the same rate (1/100 V) as in the first TLM series (Fig. 8).

It should be noted that after the first TLM stress the "turnaround phenomenon" of the threshold voltage

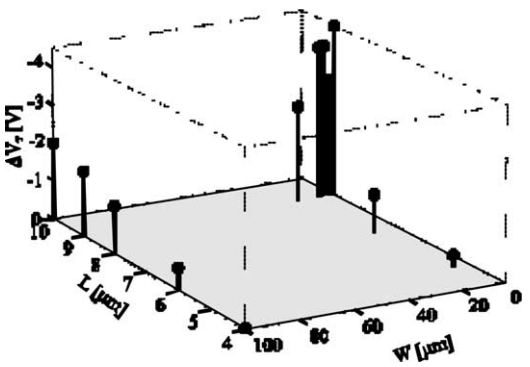

Fig. 7. Threshold voltage shift after TLM series (from 20 V up to 250 V) as function of W, L.

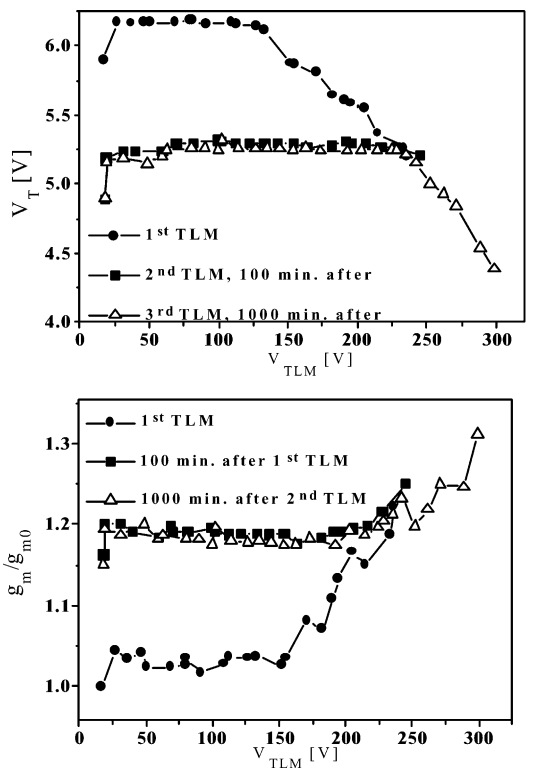

Fig. 8. Threshold voltage and transconductance behaviour during the first and the repeated TLM series.

shift is noticed. This phenomena for the low negative gate bias is already known in the literature [10] and it appears when the negative threshold voltage shift caused by the hole trapping in the SiN gate dielectric are positively compensated by the states created near the conduction band in the α-Si film. This process of state creation should be distinguished from the creation of states under high electric field.

In order to distinguish whether these charges are located in the gate dielectric or at the gate dielectric/amorphous silicon interface, the sub-threshold slope of the transfer characteristics is analysed. It appears that sub-threshold slope increases during TLM stressing, which can be result of interface state creation. Assuming that created defects in amorphous silicon are located at the gate dielectric/amorphous silicon interface, the effective defect density Dit can be related to the subthreshold slope [11] as:

$$S = \ln 10 \frac{kT}{q}\left(1 + \frac{q^2 D_{\mathrm{it}}}{C_{\mathrm{i}}}\right) \tag{4}$$

where q is the electron charge, k is the Boltzmann constant, C_{i} is gate capacitance per unit area and T is absolute temperature. The calculated values of the density of interface states vary between TFTs. For example, after a TLM series up to 250 V they are estimated to be in the order of 10^{12} $\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$. The behaviour of the subthreshold slope under TLM stress is shown in Fig. 9.

2.3. Where are the defects?

The sub-threshold slope increase during TLM stressing implies defect state creation. In order to determine where these defect states are located within volume of a TFT a repeated symmetrical experiment is performed as follows. After the first TLM series ($V_{\mathrm{TLM}} = 50$–250 V, step $= 10$ V) is applied on the source of the TFT, the second TLM series is applied on TFTs drain. In the second TLM series the V_{T} decrease and g_{m} increase

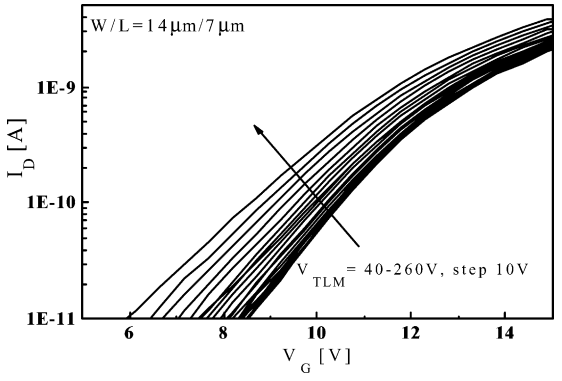

Fig. 9. Subthreshold slope change during TLM stress series.

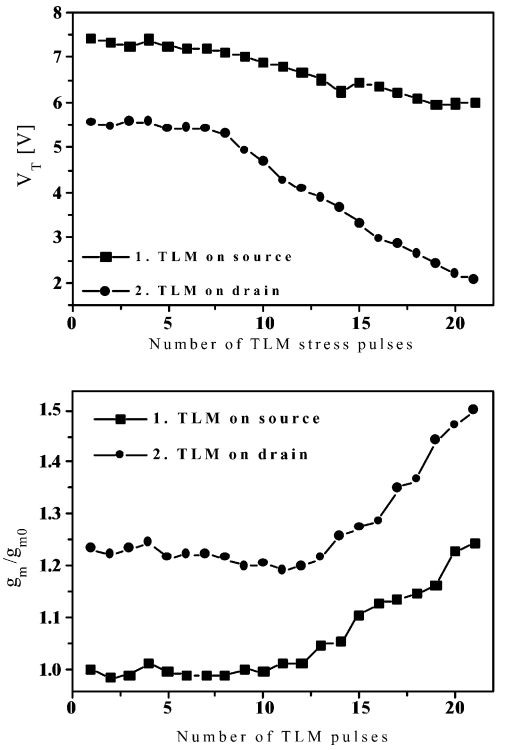

Fig. 10. Threshold voltage and transconductance variation under two repeated symmetrical TLM series (first series on the source, second on the drain).

continuously from the same threshold of degradation voltage, when compared to the first series (Fig. 10). Apparently, repetitive TLM stresses on one side of the transistor up to the highest previous level do not create additional damage, whereas an additional TLM series with the same low voltage on the other terminal does create additional damage. It means that if TLM stress is applied on the drain, the defect states are non-equally distributed along the channel. They are located close to the drain of TFT.

2.4. CV measurements showing interface states creation

An additional proof that TLM stress induces creation of fast interface states is obtained from high frequency $C(V)$ measurements [12]. Parasitic capacitance's of the drain and the source are measured before and after a TLM series up to 200 V applied on drain. The position of the Fermi level in an undoped α-Si, as used in this investigation, is shifted closer to the bottom of the conduction band. Therefore, tested TFTs are undoped and n-type. It should be noted that during the TLM testing the TFTs threshold voltage is decreased by 0.5 V, and the transconductance is slightly increased. As it is shown in Fig. 11, the high frequency $C(V)$ curves of the

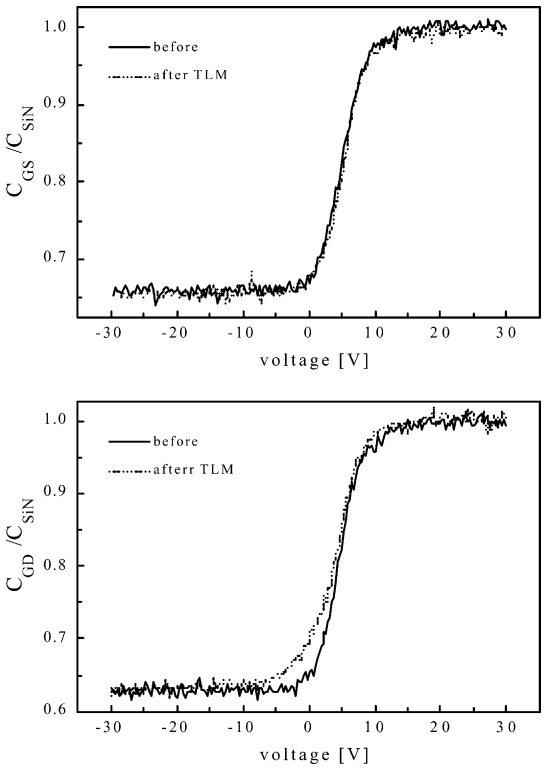

Fig. 11. Normalised high frequency capacitance versus voltage curves measured for the gate/source overlapping and gate/drain overlapping capacitance's before and after TLM stress applied on the drain.

parasitic capacitances of the source before and after TLM stress are the same, meaning that TLM stress did not induce any damage at the source side. In contrast, the high frequency $C(V)$ curve of the parasitic capacitance at the drain side (Fig. 11) after TLM stress is stretched-out to the negative side and degraded as compared with the curve monitored before the TLM stress.

2.5. Modelling of TLM stress induced degradation

Firstly, the gradually distributed electric field across the gate dielectric is simulated. The simulation shows that if the threshold voltage of degradation is applied on the drain, the electric field close to drain has value ~5 MV/cm. This electric field peak is located close to the drain, but it expands from drain to source during each next TLM stress pulse, since the TLM stress is stepped.

The assumption that a TLM stress creates positive interface charges, giving rise to sub-threshold slope and lowering V_T, is interpreted by means of electrical simulations. The assumed model says that the new created interface charge, induced by the electric field, widens

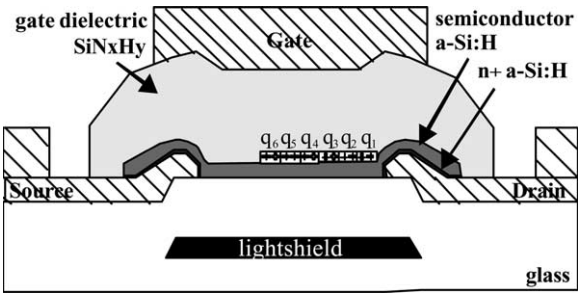

Fig. 12. Model of stepped accumulation of the interface charges.

with every step along the interface from the drain to the source (Fig. 12). The transfer characteristic of the top gate amorphous silicon transistor is simulated by Silvaco simulation tools [13], taking into account created interface charge. Initially, the transfer characteristic is simulated without any interface charge. At each simulation step a constant quantum of interface charge is added along the length from drain to source (Fig. 12). Charge parameters have been optimised, leading to: length of the cube $x = 0.2$ μm and fixed charge density quantum of 10^{12} cm^{-2}. The result of the simulations is presented in Fig. 13. It can be seen that it describes the experimentally measured characteristics, which are shown in Fig. 6.

2.6. Thermal annealing of degradation

In order to remove created interface traps, TFTs are thermally annealed. The procedure of annealing for both variations that will be presented is as follows: first thermal annealing, then the first TLM series (when V_T and g_m were monitored), a second thermal annealing (with repeated conditions of first annealing), the second TLM series (V_T and g_m monitored). Two experiments of annealing are carried out: dry annealing in the ambient

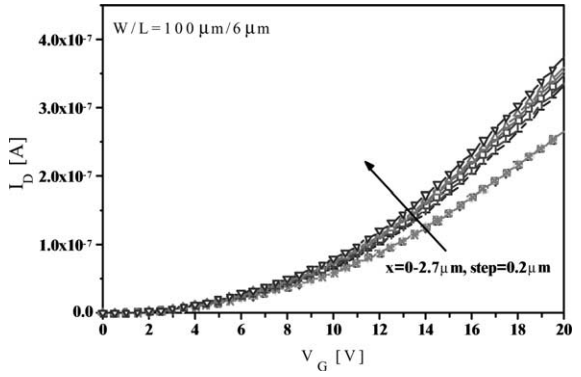

Fig. 13. Simulated transfer characteristics.

of vacuum, and wet annealing in the ambient of N_2, with the presence of hydrogen.

2.6.1. Dry annealing

After initial annealing and the first TLM series, the TFT is annealed at 200 °C for 1 h in vacuum, with all electrodes open. Analysing the behaviour of V_T and g_m under second TLM series, it can be seen that they are not constant under TLM stress. It means that the annealing is sufficient to de-trap, at least partly, the created traps. During the second TLM series after thermal annealing, transonductance is completely recovered. It returns to the starting value, and behaves similarly (same threshold of degradation and rate) as during the first TLM series (Fig. 14). It proves that created interface states, responsible for increasing of the transconductance, are removed by thermal annealing at the 200 °C. The threshold voltage value did not recover to the starting value (Fig. 14). This leads to the conclusion that processes of change in g_m and V_T have different activation energies. The process of recovering of transconductance has lower activation energy than the process of recovering of the threshold voltage. A possible explanation is that heat treatment removes only created fast states from the interface, but that the energy/time is not enough to remove deep states in the gate dielectric.

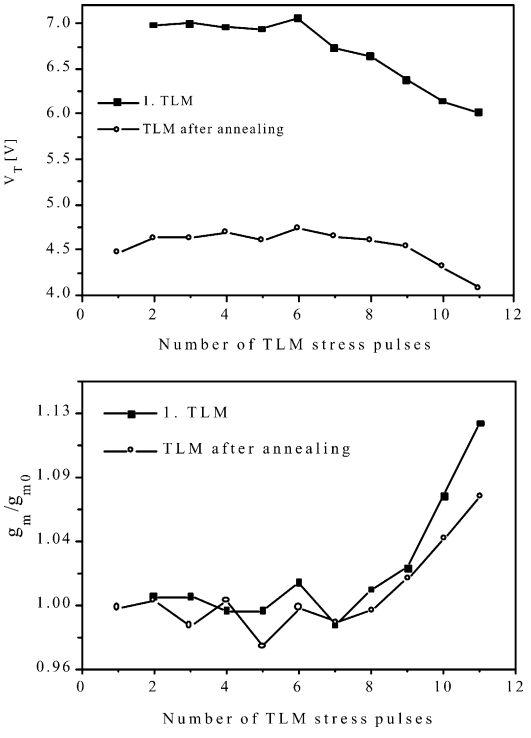

Fig. 14. Effects of dry thermal annealing on threshold voltage and transconductance.

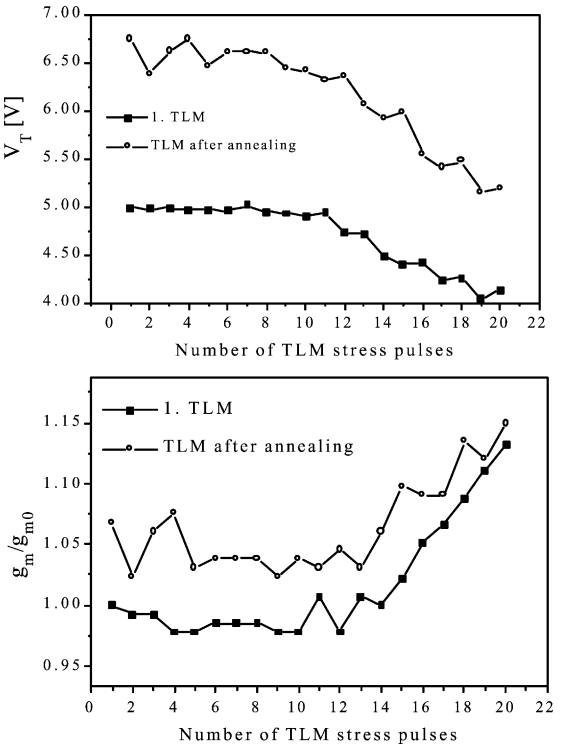

Fig. 15. Effects of wet thermal annealing on threshold voltage and transconductance.

2.6.2. Wet annealing

A completely different result is obtained by wet open-circuit thermal annealing in the atmosphere of N_2 with the presence of H_2 at 250 °C for 30 min. The results are shown in Fig. 15. As shown in Fig. 15, the threshold voltage after thermal annealing is increased (in contrast to the dry annealing), while transconductance is almost completely recovered, although it does not return exactly to the starting value. Both V_T and g_m under the second TLM series are active, they degrade in the same way as under the first TLM series, which implies that created states are removed from the α-Si:H/SiN interface. The difference in V_T shift during wet and dry annealing comes from the presence of hydrogen. Annealing without the presence of hydrogen gives negative, while annealing in the presence of hydrogen gives positive shift, as hydrogen plays important role in the process of de-trapping holes.

3. Long time experiments

A square voltage pulse in the range of seconds is applied to the drain of a TFT using a parameter analyser HP4142B and a voltage generator expander. The stress pulses are increased in steps up to 200 V, the highest

voltage that can be generated by the parameter analyser equipped with a voltage expander. During each stress pulse the drain current is measured and after each stress pulse the transfer characteristics are measured, both with the same parameter analyser.

3.1. Current during stress

Both, the voltage and the current during stressing were measured. As the voltage during stress is supplied by the voltage generator, the voltage is constant. The information of the current during stress is important, bearing in mind that that information was lost during TLM measurements. The current during stress measured on both the drain and the source of the TFT with $W/L = 18/9$ is shown in Fig. 16 for stress voltage on the drain $V_D = 200$ V, with the source and the drain grounded. It can be concluded from the plot that the current during stress is drain to source current, as two curves shown in Fig. 16 overlap, except for the first point. It should be noted that the drain current during stress is in the beginning (low drain voltages) only a subthreshold (leakage) current, as the gate is grounded. Expected level of the leakage current is in the order of several pA. After the drain stress voltage is increased, the real conduction current (order of μA) sets in. Due to the high voltage applied on the drain, the DIBL effect is initiated, as it will be explained further in Section 5.

Another important remark about the drain current during stress is that although the drain current level measured with each stepped voltage stress increases, during a stress pulse the current I_D shows an exponential decay (Fig. 16). This decay is due to the process of creation/removal states across the amorphous silicon layer. This process is confirmed from the measured transfer characteristic after stress, as it will be explained later in this section. The current during stressing reflects the creation/removal of states at the interface, but also in the bulk of α-Si. Reaching equilibrium in this process takes some time—if it is reached at all [14].

3.2. Breakdown voltage due to long pulse stress

Due to the limitations of the measurement set-up (stress voltage only up to 200 V), the breakdown voltage under long pulse stress could be measured only for the TFTs that have a breakdown voltage lower than 200 V. Therefore the breakdown voltage measurements were limited on the short channel TFTs. Two TFTs were measured: $W/L = 100/6$ and $W/L = 100/4$. For these TFTs the breakdown voltages of 150 V and 110 V are measured, respectively, under the stepped stress of 1 s. Also TFT with $W/L = 18/9$ was tested, but it did not breakdown up to 200 V stress of 1 s. The current measured on the drain one step before and during the breakdown is shown in Fig. 17.

3.3. Pre-breakdown degradation due to long pulse stress

Pre-breakdown degradation is monitored in the same way as it was under the TLM stress. From the measured transfer characteristics, values of threshold voltage, subthreshold slope and transconductance are extracted. All these parameters show the similar behaviour as under the TLM stress.

Threshold voltage, sub-threshold slope and transconductance show similar behaviour as under TLM stress. Therefore the experimental results will not be discussed in details, but only in general. An overview of the pre-breakdown degradation measured on the TFT with $W/L = 18/9$ under long pulse stress of different lengths is given in Table 3.

There are three distinguished regions in the behaviour of monitored parameters. While stress voltage is low ($V_D < 50$ V) there is a slight increase in the V_T followed with also very small decrease of S. This is an initial change that is known in the literature and it is called the

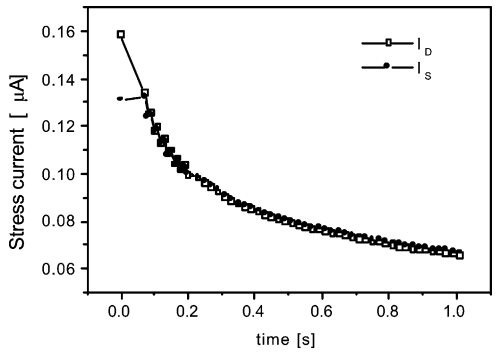

Fig. 16. Current during long pulse stress measured on the drain and the source (the source current is actually measured with the negative sign, plotted as positive for convenience).

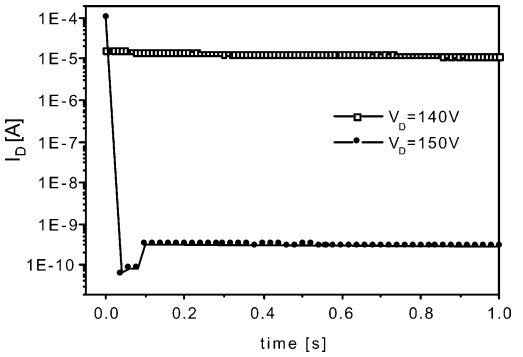

Fig. 17. Pre-breakdown and breakdown current during long pulse stress.

Table 3
Pre-breakdown degradation of the TFTs with $W/L = 18/9$ tested by the long pulse with different pulse lengths

Stress (V)	0–50	50–125	125–200
V_T	↗/0	↘	↘↘
g_m	0	↗	↘↘
S	0/↘	0/↘	↗↗

turnaround phenomena and it was already mentioned in Section 2.2. After the stress voltage is increased further ($50 < V_D < 125$ V), another region could be recognised when V_T decreases moderately ($\Delta V_T < 1$ V), g_m increases and S stays the same as in the previous region. In this region there is no significant creation/removal of interface states and the process of charge trapping in the gate dielectric dominates. After the stress voltage is higher then 125 V, V_T degrades severely ($\Delta V_T \sim 3$ V), while g_m decreases severely and S increases sharply. In this region creation/removal of interface states in the amorphous silicon layer dominates in the process of degradation.

4. Time–voltage trade-off

In this section the time–voltage trade-off is presented in order to give an in-depth analysis of the ESD effects in α-Si:H TFTs. The data presented in this section are actually drawn from the experimental results shown previously in Sections 2 and 3.

4.1. Breakdown voltage over time

The question we want to have an answer to is if the breakdown depends on the stress time or it is only related to the stress level. That is important information to determine the mechanism of breakdown. The dependence of the power of the square pulse and the time to failure is due to the energy consumed at TFT, as explained by Wunch and Bell model [6]:

$$E = \int_0^T I(t)V(t)\,\mathrm{d}t \tag{5}$$

It is an early model of thermal breakdown in Si devices. In this model the pulse power and time to failure are related by $P \sim t^{-1/2}$. This model covers only the middle part (typically for Si that is in the region (10 ns $< t <$ 100 μs) of the $P(t)$ curve. For very short failure time ($t <$ 10 ns), the little heat is developed so that the process is adiabatic $P \sim t^{-1}$. For very large failure times, typically above 100 μs and after thermal equilibrium has been established, the constant or steady state term dominates.

Unfortunately, there are not enough (accurate) breakdown voltages measured for different pulse lengths using TFTs with the same W/L. The data measured under TLM stress are shown in Fig. 5, and the same TFT ($W/L = 18/9$) could not be measured by long pulse stress. Only the small number of data for TFTs $W/L = 100/6$ and 100/4 are available. In these two TFTs the breakdown voltage change from 240 V under TLM stress to 150 V under long pulse stress and from 180 to 110 V, respectively. Still, from this limited data source it is possible to draw the conclusion that breakdown voltage depends on the pulse duration, e.g. it lowers if the pulse length of applied stepped voltage stress increases, but a unique function of this dependence is not known. Though the current in TFT under square voltage pulse proves not to be constant in time (it exponentially decreases with time), we could assume from Eq. (5) that V_{BR} lowers if the pulse length of applied stepped voltage stress increases. This conclusion implies that the breakdown due to ESD stress in TFTs is a thermal breakdown. The power-density-dependant failure of amorphous silicon TFT was previously investigated in [15] in the range 1–10 ms. From the power of the square stress and the volume of the melted area, the melting point of the breakdown will be calculated in Section 6.

4.2. Pre-breakdown damage threshold over time

The pre-breakdown degradation dependency on time is explained through the damage threshold. The damage threshold, a stress voltage under which the pre-breakdown degradation sets in, was extracted as a voltage for which threshold voltage V_T starts to decrease. Measurements of the damage threshold shown in Fig. 18 involve both TLM and long pulse measurements. The data are collected from Sections 2.2 and 3.3. The extrapolated function of the threshold of degradation over stress pulse length is shown in Fig. 18.

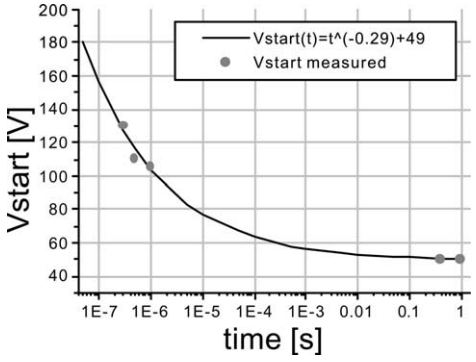

Fig. 18. The time dependence of the degradation presented with points (measurements) and line (descriptive power law curve).

The measured data are approximately described (as the number of data is low for a reliable fitting) by an analytical function, which is based on the formula that describes time dependence of the threshold voltage V_T shift at voltages where states creation dominates, described by a power law, $\Delta V_T = a \cdot t^{\beta}$, with β about 0.3–0.5 [16]. It concurs very well with the measurements, which supports our earlier statement that the secondary degradation of the threshold voltage is due to state creation.

It is also important to note that there are two regions in the dependence between the damage threshold and time. In the first region the damage threshold decreases with time. In the later part of the curve ($t > 100$ μs) the equilibrium process is established, the temperature in the system becomes constant and the further increase in stress time does not speed up degradation process anymore.

5. Device simulations

5.1. Theoretical introduction

The breakdown of amorphous silicon devices was earlier investigated in diodes [17], or in an antifuse structure [18], where evidence was found of impact ionisation in a-Si. In the thin film transistors itself a huge amount of work and research was focused on metastable effects in amorphous silicon, but very little was published on the subject on electrical breakdown. The items that have to be clarified about electrical breakdown in α-Si:H TFTs are:

- Is there punch-through?
- Is there impact ionisation and avalanche breakdown?

Before the results of simulations regarding these questions will be shown, a few basic definitions will be introduced. Punch-through effect occurs when the neutral substrate width is reduced to zero at a sufficient drain voltage and the source depletion region is in direct contact with the drain depletion region. At this point, the source is effectively short circuited to the drain, and a large current can flow. What actually happens is that under high drain bias the channel depletion width is no longer constant along the length of the device, but varies from the source to the drain. This effect is called drain induced barrier lowering (DIBL) effect and it occurs when higher drain voltage is applied to the device. It is very well known in MOS devices [19]. The surface potential (bend bending) along the channel between source and drain for long channel devices is normally constant. In short devices, or in long devices under very high drain biasing, it happens that the peak of the surface potential is reduced and is constant only over a small part of the channel, if at all. Since the peak surface potential is reduced, which means that the barrier is lowered, the current will increase.

Avalanche multiplication that may occur by means of impact ionisation is very well explained in standard crystalline Si devices [20]. Electrons/holes gain so much energy in a high electric field that they can generate extra electron-hole pairs by exciting electrons from the valence band into the conduction band. In this way an avalanche of free carriers may arise. Could we expect an avalanche multiplication due to impact ionisation in amorphous silicon in our TFTs?

5.2. Simulation results

The electrical simulations of TFTs are preformed by SILVACO process and design simulation software. The effect of DIBL is shown through the simulations of:

- surface potential of an a-Si:H TFT under high drain bias;
- surface potential of a long- and a short-channel TFT under the same biasing conditions.

In Fig. 19 is shown how the surface potential is distributed along the channel for three different drain biases ($V_D = 10$, 20, and 50 V). In all cases the gate voltage was kept constant. It should be noted that the simulated TFT was scaled in lateral direction, which means that channel length and the drain biasing are divided with the factor 10. So the channel length of simulated device was $L = 0.6$ μm, under drain bias ($V_D = 1$, 2, and 5 V). That is done for the simplicity. It slightly influences the accuracy of the simulation results, but does not influence the conclusion extracted from the results at all. This

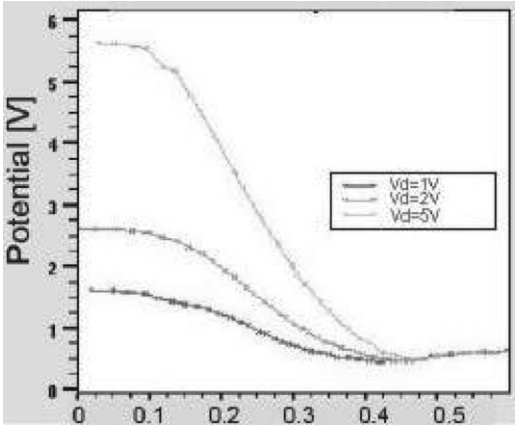

Fig. 19. An example of DIBL effect in amorphous thin-film transistors simulated for various drain voltages (scaled down from $V_D = 10$, 20, and 50 V).

figure shows that by increasing the drain bias, we decrease the barrier. It proves that the DIBL effect is present in α-Si:H TFT devices. It also helps us to understand the results obtained from the experiments. In the experiments the drain was stressed. The gate was grounded, so that the device was not active in the conductive mode. Initially, under very low drain voltage a low leakage current was flowing through the channel. As the drain voltage was increased, the DIBL effect was more and more pronounced. When the drain voltage is large enough, the real current flows through the device.

In another example it is shown that the same effect of barrier lowering can happen if the channel length is varied. Therefore a TFT with two different channel lengths is simulated. The results of these simulations are presented in Fig. 20. The simulations show that with shortening of the channel, the barrier between source and drain is lowered. It also agrees.with our experimental observations. Namely, it was noticed that both the threshold of degradation and the breakdown voltage depend on the channel length. The shorter TFTs degrade and fail earlier than the longer ones.

The previous simulation results proves the presence of the punch-through in α-Si:H TFTs. It shows that the punch-though occurs when drain voltage is high enough to suppress the barrier in surface potential between source and drain. It happens earlier in shorter devices from the reason that in the short channel devices the barrier is already initially lowered. What we want to know further is if the depletion width at the drain extends far enough in real device to have punch-through.

The question of the impact ionisation and the avalanche breakdown is analysed through the simulation of the recombination/generation rate under stepped drain bias. The results of the simulations performed for a constant gate voltage ($V_G = 25$ V) and different drain biasing are shown in Fig. 21. Fig. 21 shows (please note

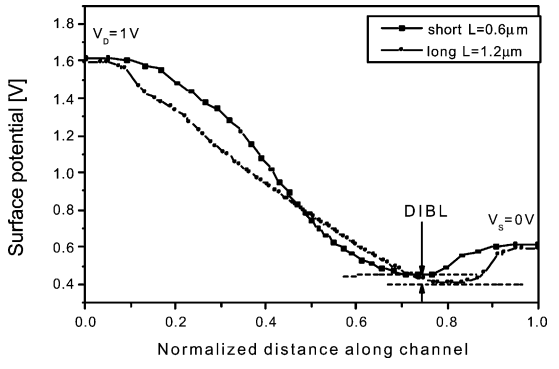

Fig. 20. Surface potential distribution for TFTs along the channel obtained for examples with different channel lengths.

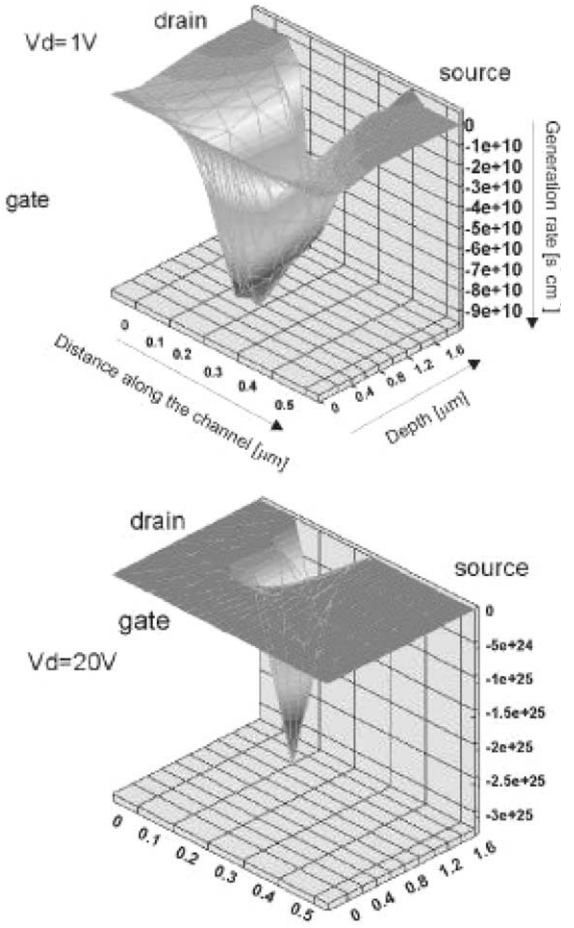

Fig. 21. Generation rate simulated under constant gate $V_G = 25$ V and varying drain biasing $V_D = 1$, 20 V.

that the drain voltage and the channel length are scaled with factor 10) that the peak generation rate is located at the drain, in case when stress is applied to the drain. The generation peak value in the TFT with the channel length $L = 0.6$ μm changes from $G = 9 \times 10^{10}$ 1/s cm^3 $V_D = 1$ V to $G = 3 \times 10^{25}$ 1/s cm^3 for $V_D = 20$ V. As the results are scaled by factor 10, it allows us to compare this result with the TFT with $L = 6$ μm and $V_D = 10$ and 200 V, although we must be aware that linear scaling of both voltage and size is not the same as scaling the problem, as depletion layer width goes with $V^{1/2...1/3}$. The experiment shows that the breakdown in the TFT with $L = 6$ μm that occurs at 280 V could really be initiated by avalanche breakdown at the drain side. In this case we can expect an generation rate $G > 3 \times 10^{25}$ 1/s cm^3. This level of generation is enough to start an avalanche breakdown. Simulation results prove that an avalanche breakdown is possible in amorphous silicon TFTs under ESD stress conditions.

6. Post-breakdown observation

Post-breakdown observations have been carried out using optical microscopy and scanning electron microscopy (SEM). The observation confirms the location of the breakdown spot close to the drain in case when the ESD stress is applied to the drain. This further support our conclusion that avalanche creates onset of breakdown in short devices. In long-channel devices, where breakdown voltage is higher than in the short-channel devices, the electric field close to drain at the moment of breakdown is very high and very close to the value of the critical electric field for silicon nitride (5–6 MV/cm). This electrical field was simulated and the value at the drain for applied drain voltage of 350 V is already at the level of the critical electric field. This could indicate that not only avalanche is cause of breakdown.

The most often found failure mode is gate dielectric breakdown. It appears as a rupture localised close to the drain, with a centre at the edge between drain and channel. Exceptions are short channel devices, where the rupture completely covers the channel length. In this case, because of punch-trough, the avalanche generation rate is no longer confined to the drain side. The size of the rupture indicates that the breakdown is a high temperature event. The temperature of the breakdown was calculated on basis of the rupture size, assuming a spherical volume of the whole rupture, and the temperature of over 1400 °C is estimated. The location of the rupture indicates the position of the highest temperature peak. After inspection of failed devices the assumption is made that the highest peak of the temperature should be located at the edge between the drain and the channel, as it is shown in Fig. 22. Fig. 22 shows example of gate dielectric breakdown in a TFT with $L = 6$ μm, after etching of the top gate electrode. The size of the breakdown spot is large so that it covers almost the whole channel length. The centre of the breakdown spot is located exactly on the drain/gate edge.

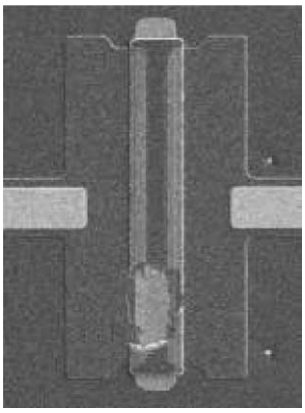

Fig. 22. SEM photograph showing the breakdown location in the TFT.

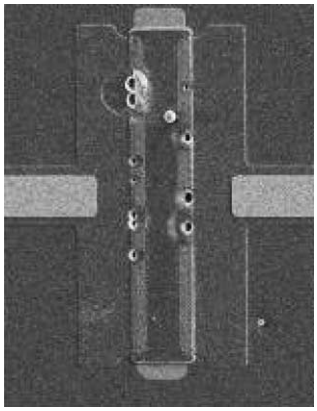

Fig. 23. SEM photograph showing the breakdown location in the TFT.

Another failure mode, found in about 10% of all analysed failures, is breakdown of the glass substrate, when the current path is created from drain to source via a light-shield. The SEM picture of the de-processed device (gate dielectric removed) discovering this breakdown mode is shown in Fig. 23. Current path is created through the glass substrate. A number of melt filaments are found at both drain/gate and source/gate edges.

7. Non-isothermal device simulation

Although industrial interest in TFTs in the last years is increased as display industry is developing, this is the first attempt that self-heating in TFTs in amorphous silicon TFTs is still not investigated in depth. This method for simulation of self-heating effects uses an electrical circuit where currents represent heat flow and voltages represent temperatures. The power dissipation of a transistor in the electrical circuit is modelled with a current source in the thermal circuit. Current in the thermal circuit represents the heat dissipation across device. The principle of this method is shown in Fig. 24.

The thermal resistance and thermal capacitance of the amorphous silicon are modelled in the thermal circuit with an electrical resistor and an electrical capacitor respectively. The thermal circuit is coupled with the electrical circuit by means of the temperature and power dissipation. The voltage at thermal circuit is equivalent of temperature in electrical circuit. The temperature in electrical circuit is involved by change in carrier mobility. The carrier mobility change is approximated by equation:

$$\mu = \mu_0 e^{-(E_a/kT)} \quad (6)$$

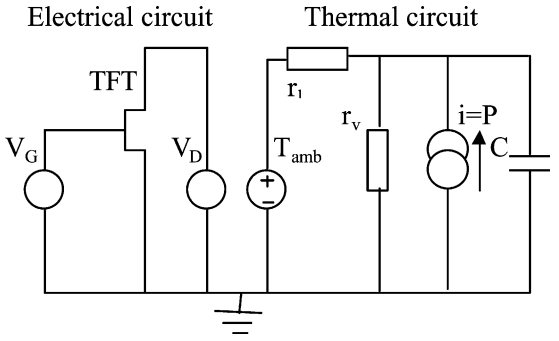

Fig. 24. Principle of the thermal–electrical circuit simulation method.

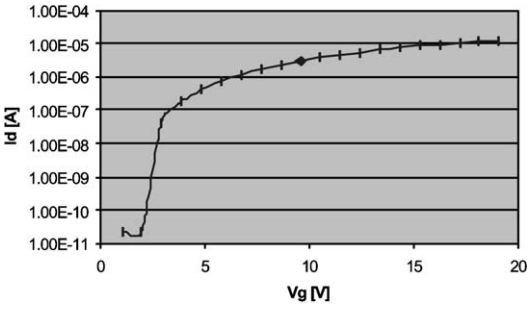

Fig. 25. Transfer characteristic of TFT simulated by PSTAR MOS model.

where activation energy $E_a = 0.1$ eV, Boltzmann constant $k = 8.6 \times 10^{-5}$, T is absolute temperature and μ_0 is set at 15 so that carrier mobility at 300 K is $\mu = 0.3147$ cm^2/Vs. The circuit simulator PSTAR is used to determine steady state and transient solutions of these coupled circuits. The circuits can be solved in two ways: simultaneously (coupled) and sequentially (uncoupled), as circuit simulator PSTAR allows control of electrical mobility by electrical variables. In simultaneous simulations all voltages and temperatures are solved in the same time. In the sequential simulations the electrical circuit is solved first, than the results are used as input parameters for the thermal circuit. The result of thermal simulations is again used as input (temperature) for electrical circuit etc. In this work simultaneous approach is used. Sequential approach is used only during programming process to verify obtained results. The problem with non-isothermal device simulations is that the thermal and the electrical geometric domain are different. The thermally active area is much larger. In three-dimensional simulations it can produce very large number of elements and a long execution time. Often compromise must be made between accuracy of the simulation and computer time, although in this simple TFTs structure should not be a limitation.

7.1. TFT modelling using PSTAR

Before electrothermal simulations have been performed, it is first checked if a TFT can be simulated with PSTAR. The model used in these simulations is PSTAR MOS model, level 301, which allows change of transistors parameters, such as mobility and threshold voltage. To compare simulated characteristics with the measured ones, parameters are set at $\mu = 0.3$ cm^2/Vs, $V_T = 2$ V, $L = 100$ μm and $W = 1000$ μm. The simulated characteristic, shown in Fig. 25, shows that level of the output drain current is similar to the measured current. It was also checked if carrier mobility behaves according to the given equation. It should also be noted that switching characteristics of crystalline MOS transistors are much better than once of the TFTs, but it is assumed that it would not influence the quality of the simulations, so this model has been accepted.

7.2. Electrothermal model

In electro-thermal simulations, current and voltage distributions over a TFT active area are calculated. In that order, the TFT is split up into a number of sections. Depending on the mesh, 2D and 3D simulations are distinguished. In 2D simulations, a TFT is split into number of sections along the TFTs length. In 2D simulations all these sections have the same width, which is equal to the width of TFT itself. In 3D simulations each of these sections is split into number of sections along the TFTs width, allowing calculation of the temperature distribution in both directions of channel length and channel width of the TFT.

In the first stage two-dimensional simulations are performed. Geometrical representation of the simulated structure is shown in Fig. 26. The electrically active area of the TFT is split into ten sections (by dashed lines A–K in Fig. 26), each with its own current, voltage and temperature. The thermal circuit is created within a thermally active area, which is inevitably larger than the electrically active area, with its own mesh that only

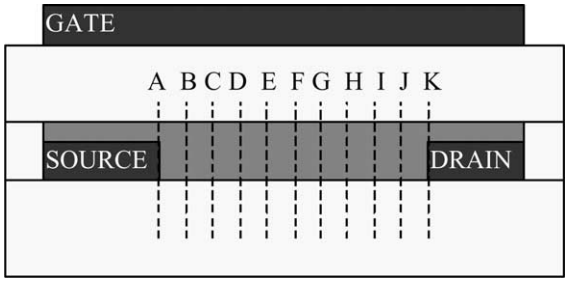

Fig. 26. Geometrical representation of top gate TFT.

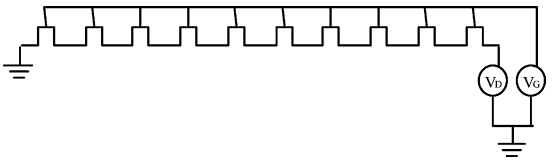

Fig. 27. 2D electrical model of a TFT.

coincides with the mesh for electrical circuit in the areas where heat is generated.

Electrical circuit of the model is shown in Fig. 27. For the electrical network, a TFT with dimensions $W = 20$ μm and $L = 10$ μm is modelled with a serial connection of ten TFTs with $W = 20$ μm and $L = 1$ μm.

The concept of modelling of a TFT with serial connection of TFTs is verified in the following way. The same example used in Fig. 25 is simulated to compare previous results of simulations of a TFT with the simulation of this model. As shown in Fig. 28 (left axis) the simulated output drain current is the same as the current shown in Fig. 25. In addition to this model verification, in the same plot it is also shown how the lateral effects are automatically incorporated using this model. Thanks to the fact that voltage on each of TFTs is not equal, current naturally must be equal in a serial connection, then the power dissipation and consequently the temperature are not equally distributed between TFTs in the serial connection. Distribution of voltages at each of ten TFTs in serial connection is shown in Fig. 28 (right axis). Biasing conditions are $V_D = 10$ V, $V_G = 0$–20 V. At the first moment, total drain bias stays on the last TFT in the row, as the last TFT is at the drain side. As soon as it starts to conduct, the other TFTs start too. After all of TFTs are in the saturation region ($V_G > 15$ V), voltage among them is still non-equally distributed.

As the electrical circuit is verified as satisfying, the thermal circuit is to be built. Although the mesh that is used in this simulation is extremely simple, as it is made manually, the thermal circuit is already more complicated. It comes from the reason that the active area for thermal circuit is larger than the active area for the

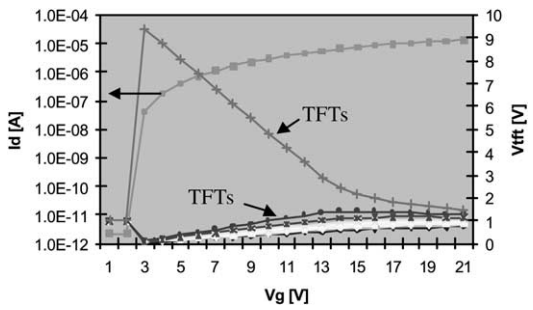

Fig. 28. Current and voltage distribution among 10 TFTs in serial connection.

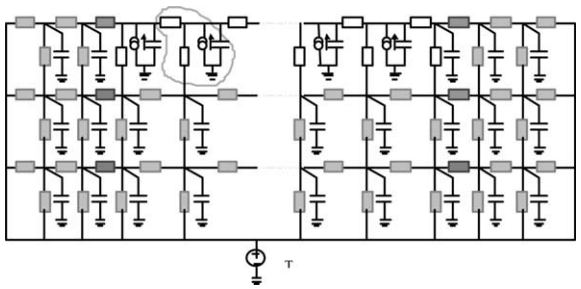

Fig. 29. Thermal circuit used in 2D simulations.

electrical circuit, as temperature is dissipated into the glass substrate. In this case, only two extra layers surrounding electrically active area are taken into account. Scheme of the thermal circuit is given in Fig. 29. Part of the circuit that is circled represents one section in the electrically active area of TFT. Thermal resistances are coloured in different shades of grey in order to distinguish their different meanings. Resistances at the top central part represent thermal behaviour in electrically active area (white). They are surrounded by a number of lateral resistances that represent the junction between amorphous Si and glass (dark grey). Rest of the circuit belongs to glass area (light grey). It should be noted that temperature is taken into account only in the bottom part of device (amorphous silicon layer and under it) and thermal dissipation through nitride and metal connections has been neglected.

For each of the circuit elements used in the thermal network a model has to be defined with spatial dimensions as parameters. The dependence of a thermal resistance and capacitance on the spatial co-ordinates is determined by the heat flow equation:

$$C_T \frac{\partial T}{\partial t} = H + \kappa \cdot \nabla T \tag{7}$$

where C_T is the thermal capacitance per unit of volume in $J\,K^{-1}\,cm^{-3}$, T is the temperature in K, H is the heat generation per unit of volume in $W\,cm^{-3}$, κ is the thermal conductance in $W\,K^{-1}\,cm^{-1}$. If we introduce an analogy between the thermal capacitance per unit of volume with electrical capacitance per unit of volume, the thermal conductivity with electrical conductivity, the temperature with voltage and the heat generation with electrical current, than heat equation is analogue to the following partial differential equation:

$$C \frac{\partial V}{\partial t} = i + R \cdot \nabla V \tag{8}$$

Necessary condition or solving this differential equation is that system must be discrete. In three- dimensional discrete system current flow is allowed in direction of x, y and z axis. To solve equation the boundary conditions must be given. Boundary conditions are determined by

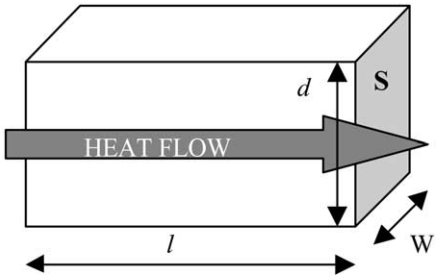

Fig. 30. Definition of elementary dimensions in a section.

means of ambient temperature and input power dissipation. Finally, we can represent temperature distribution by a network of electrical resistances and capacitance's. An elementary volume is represented in Fig. 30. As current through the capacitance is $i = C \cdot \mathrm{d}V/\mathrm{d}t$, follows that all thermal capacitance's must be connected to the ground. As current through resistance is $i = \Delta V/R$, then resistances are connected into a network. For the three-dimensional rectangular mesh, the solution for the thermal resistance is:

$$R_{\mathrm{TH}} = \frac{l}{\kappa \cdot S} \tag{9}$$

where l and S are dimensions shown in Fig. 30. The heat capacitance is given by:

$$C_{\mathrm{TH}} = C_{\mathrm{p}} \cdot S \cdot d \tag{10}$$

where C_{p} is specific heat per volume in $\mathrm{J\,K^{-1}\,cm^{-3}}$. Thermal resistance at the junction of two materials is calculated direction as a parallel connection of two thermal resistors:

$$R_{\mathrm{TH}} = R_{\mathrm{TH1}} \| R_{\mathrm{TH2}} \tag{11}$$

The mesh is generated using the simplest concept of classical rectangular meshing. A rectangular domain is divided into smaller rectangles by classical mesh. Dimensions used in building of the thermal mesh are up to free choice of the researcher. His choice is of course limited with the computer speed. Physical quantities are calculated within the volume of mesh cubes. One possible choice of mesh dimensions used in this simulation is given in Fig. 31. Top layer thickness is set at 360 nm which is in reality representing thickness of both amorphous silicon and silicon nitride layer. Thickness of glass layers is set at 1 μm, although in reality thickness of the glass substrate is usually much thicker.

The materials involved are amorphous silicon, glass (Corning), metal (Molybdenum or Aluminium) and silicon nitride. Their thermal conductance and specific heat at room temperature are given in Table 4. In this simulation it is assumed that both thermal conductance and specific heat are temperature independent, for simplicity

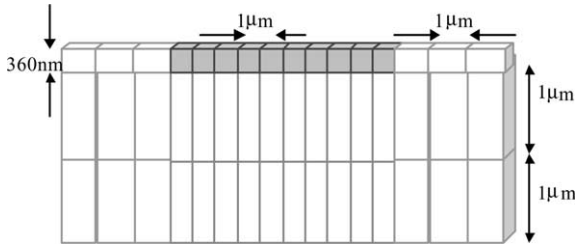

Fig. 31. Meshing dimensions.

Table 4
Characteristics of materials

Material	Thermal conductance ($\mathrm{W\,K^{-1}\,cm^{-1}}$)	Specific heat per unit volume ($\mathrm{J\,K\,cm^{-3}}$)
Amorphous silicon	0.018724	2.3405
Glass	0.01	0.66988
Silicon nitride	0.0187	2.2737
Aluminium		0.921096

reasons. It is apparent that these materials have similar value of thermal conductance, which is very low in comparison with thermal conductance of crystalline silicon. That is the reason why problem of heating exists in amorphous silicon TFTs, despite the fact that power dissipation is never high (because of low carrier mobility).

Steady state solution of this simple 2D structure is given in Fig. 32. It represents temperature distribution along the channel. Simulated structure is n-type TFT, with electron mobility $\mu = 0.3$ $\mathrm{cm^2/Vs}$, $V_{\mathrm{T}} = 6$ V and bias conditions are $V_{\mathrm{D}} = 350$ V and $V_{\mathrm{G}} = 50$ V. As voltage is applied on drain and source is grounded, the temperature has the highest peak at the drain side. Moving closer to the source side, the temperature decays. Temperature at the source side has value that is very close to the room temperature.

Extension of 2D simulation to 3D simulation is obtained by splitting TFT in the channel width direction.

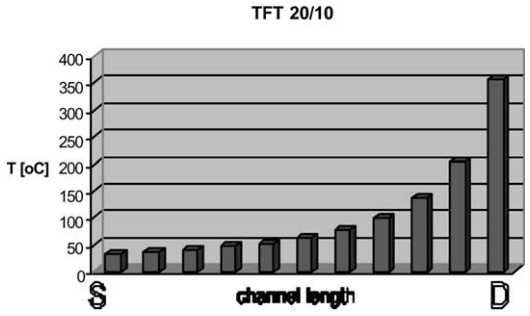

Fig. 32. Steady state solution for 2D simulation.

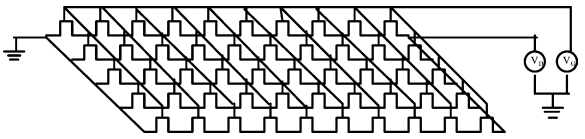

Fig. 33. Electrical circuit as used in 3D simulation.

The scheme of the electrical circuit used in 3D simulations is shown in Fig. 33. The total channel width is split in 5 rows, which do not interact in electrical, but only in thermal circuit. It is possible that electrical current exists in lateral direction. Simulation of this current would be possible if a TFT would be added between two neighbour nodes in two consequent rows. In this case this lateral current is neglected for the simplicity reason. In our case, a TFT with dimensions $L = 10$ μm, $W = 100$ μm is modelled with a network of 50 TFTs with dimensions $L = 1$ μm and $W = 20$ μm.

For building of the thermal circuit for 3D simulation, the same method is applied as in 2D simulations. Only difference is that part of the circuit is added to represent temperature dissipation into direction of new added dimensions. The new part of the circuit has the same mesh used for lateral dissipation in 2D dimensions. The results of 3D simulations obtained under steady state conditions are presented in Fig. 34. Transistor dimensions are $L = 10$ μm, $W = 100$ μm. Transistor model is n-type TFT. Biasing conditions for both simulations are: $V_D = 350$ V, $V_G = 50$ V.

The result of transient analysis is given in Fig. 35. Firstly, as ESD event is simulated, voltage pulse of length 100 ns, with rise and fall time of 10 ns is applied on drain. Gate voltage is $V_G = 50$ V, source is grounded. In this time scale self-heating process is not completed, in other words, the temperature is still not come to the value calculated in DC simulation (at the hottest point 325 °C). Length of applied drain pulse is increased in steps (100 ns, 1 and 100 μs) in order to determine when the self-heating process is completed. For stress pulse lengths of 100, 200, 500 ns and 1 μs the hottest point temperature is increasing with time and yet is not

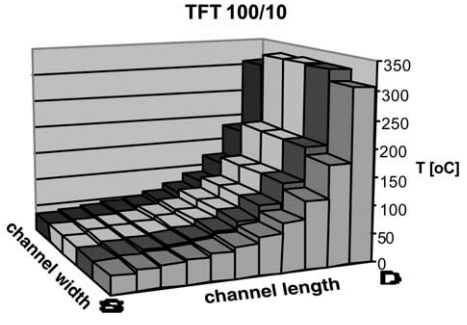

Fig. 34. Steady state 3D simulation.

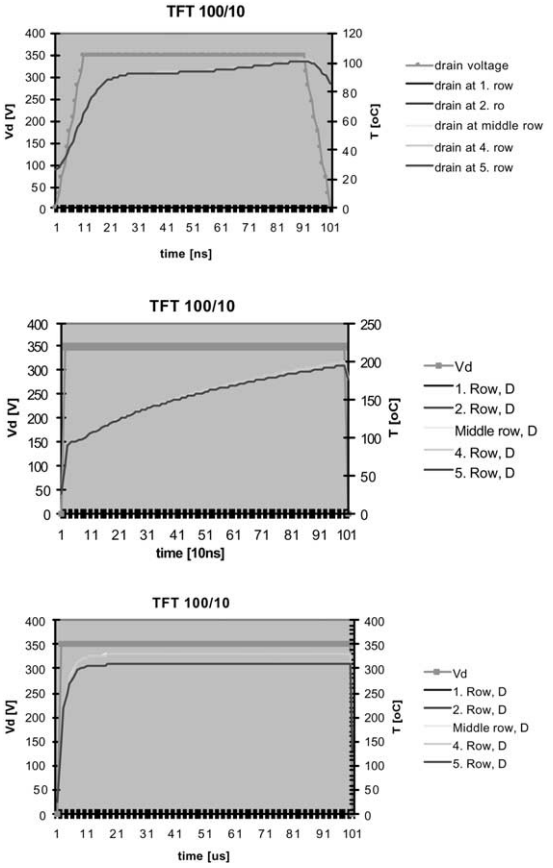

Fig. 35. Transient 3D simulation calculated at the five points at the drain side for different pulse duration (a) 100 ns, (b) 1 μs and (c) 100 μs.

reached equilibrium. Also, there is not much difference in temperature between rows. Temperature is homogeneously distributed over device. The temperature comes to saturation after 15 μs (Fig. 35). Finally, for the length longer than that the temperature is constant.

Thermal simulations of TFTs include many approximations, which are not present in reality, so it would be difficult to give a reliable answer to the question what is the temperature level under certain current and voltages. Nevertheless, the distribution of temperature is determined. Process of self-heating can be described as:

- if a voltage is applied on drain, than the drain becomes hot region,
- if a voltage is applied on drain, then the temperature develops with time and reaches its maximum after 15 μs.

Simulated distribution of temperature approves experimentally measured results. As TFTs are very simple devices from the point of view of their geometrical

design, they are rather easy to simulate. For given example, the execution time of transient 3D simulation is about 30 seconds. It is due to the fact that only rectangular mesh is used.

8. Intrinsic thermal–electrical effects in a -Si:H TFTs

As is was previously explained, a simulator [21] has been used which translates a thermal model into an electrical equivalent, which in turn can be simulated using an electric circuit simulator. The simulations are performed in order to show the level of the temperature peak under ESD stress conditions, and the location of the peak within the TFT. For the simulations we use simulation package LUMEX, which was developed at the University of Twente and is used for coupled electro-thermal simulations as a pre-processor for the circuit simulator.

Firstly, simulations of the TFTs with W, L variations are performed in order to show the temperature distribution over the TFT area in the short and long TFTs. The biasing conditions are: gate voltage $V_G = 60$ V and drain voltage $V_D = 100$ V. These biasing conditions are chosen to show the heat generation in the most severe case. The simulations were performed under assumption that the heat generation is equally distributed in all four lateral directions over glass area. The area surrounding the devices was the same in all simulations. Only the channel length was varied, while the channel width was constant, as well as the drain and the source metal contacts widths. The simulated structure is designed according to the top-gate device built on a glass substrate and from the top side passivated over all device area, used in the experimental procedure. The temperature distribution shown in Fig. 36 is the temperature of the glass substrate in the first layer under the amorphous silicon layer. In Fig. 36 the channel length area has on the x-axis a finer grid than the surrounding substrate. The temperature distribution over TFTs shown in Fig. 36 is similar in both TFTs. The simulations show that the temperature peak is located always at the drain side. Across the channel length, the temperature decreases from drain to source. In case of short devices the distribution is very much uniform across the channel length. For the channel length of $L = 4$ μm (Fig. 36), the simulation shows that the TFT is overheated. The simulated temperature is impossibly high $\Delta T = 2400$ °C, so it implies that in the reality the TFT would be already broken down. In contrast, the device with the length 100 μm is not heated ($\Delta T < 1$ °C). The simulations confirm that short channel devices suffer from more pronounced thermal heating due to the larger localised power dissipation.

It is shown in the experiments that the breakdown voltage depends on the TLM pulse duration. The question is whether the change of breakdown with the

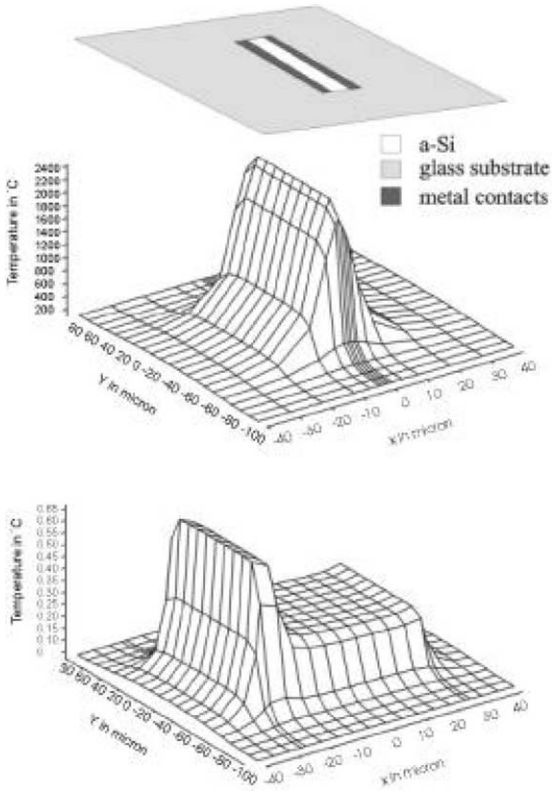

Fig. 36. Thermal simulations showing the temperature distribution in the TFTs with different channel length.

change of the stress time is related to the thermal heating. Therefore, the 3D electro-thermal simulations were performed in transient regime. The stress conditions similar to the one in the experiment ($V_D = 350$ V, $V_G = 10$ V, $V_S = 0$ V, $W/L = 100/20$ μm) were simulated for variations of the pulse length. The results of the transient simulations are presented here by only one point chosen at the end of the stress pulse, when thermal heating is in its peak. The space coordinates of the location for which the results are shown are in the middle of the TFT width, at the drain side, which is chosen as it is shown to be the hottest point in the TFT. Fig. 37 shows the temperature rise for the stress pulses of different duration. It is shown that a certain time, which is in order of an ESD pulse, is needed for establishing a temperature constant in time. After 100 μs the temperature rise in the hottest point becomes constant. It can be assumed that after the TFT enters thermal equilibrium and constant temperature is established, the breakdown voltage becomes constant.

A relation between Fig. 37 and Section 4 has to be mentioned. It was mention earlier in Section 4 that there are two distinguished regions of the damage creation over time. There is a region when the damage threshold decreases with time ($t < 100$ μs) and a region when the

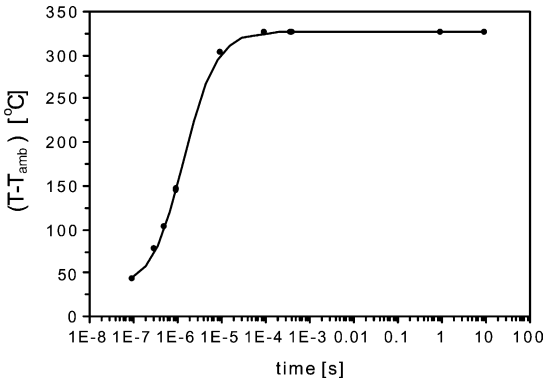

Fig. 37. Transient thermal simulations showing the temperature rise at the hottest point in the TFT for different TLM pulse lengths.

damage threshold stays constant although stress time is increased. That behaviour was extracted from the experimental results and it can be explained with the help of the Fig. 37. Namely, the damage creation is a thermal process. Therefore the amount of the damage depends on the temperature of the system. Therefore the threshold of damage creation depends on the stress time due to the fact that the temperature in the system depends on the stress time as well. For very short stress times ($t <$ 100 μs) the temperature of the system changes with time (Fig. 37). After 100 μs the temperature of the system is constant with increasing the stress time, which provides that if the stress time is longer than that, process of damage creation starts always with the same voltage.

9. Conclusion

In this paper an overview of the research with applying ESD stress on amorphous silicon TFTs is given. The results show that due to their high resistance and low current, TFTs are very difficult to be tested by standard ESD testing systems. The results also show that they response to the ESD stress somewhat different then crystalline MOS devices. For example, the effect of pre-breakdown degradation is much more pronounced. The pre-breakdown degradation of electrical parameters such as threshold voltage is analysed in details as well as electrical breakdown. The process of self heating during stress is very pronounced and it is found to be responsible for the damage.

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