Piezoelectric Strain Modulation in FETs

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***Abstract*— We report on a feature for the transistor, a piezoelectric layer to modulate the strain in the channel. The strain is proportional to the gate-source voltage, and thus increases as the device is turned on. As a result, the device has the leakage current of a relaxed device and the lower threshold voltage of a strained device. Our results, obtained by combining electrical and mechanical simulations, demonstrate that strain modulation can result in a 9 mV/decade smaller subthreshold swing for a FinFET.**

***Index Terms*— CMOS, FinFET, piezoelectric effect, power, strain, subthreshold swing.**

I. Introduction

POWER consumption of electronic circuits is becoming a major issue, for example, both the battery life of portable devices, and the cost of providing cooling, are relevant considerations [1]. A part of the power consumption originates from transistor off-state leakage. This can be reduced using transistors with a smaller subthreshold swing (SS) [1]. Currently, many device concepts aiming at a smaller SS are investigated. Examples are: 1) the impact ionization FET [2] where the current is formed by avalanche of charge carriers; 2) the band-to-band tunneling (B2BT) FET [3]–[5] where the current originates from a strongly field dependent B2BT process; 3) the suspended gate transistor [6], in which the gate is physically close to the Si in on-state, however, further away in off-state; and 4) the incorporation of ferroelectric materials as a gate dielectric [7], [8], which employs the negative capacitance effect.

For more than a decade, strain has been applied in devices to boost the carrier mobility [9]–[12]. This enhancement is attributed to the offset of the energy bands because of strain. The offset also narrows the bandgap, which in turn increases the subthreshold current [12]. Therefore, it may be favorable to relax the semiconductor in the off-state, resulting in a low off-current, and to strain the semiconductor in the on-state, to obtain a lower threshold voltage Therefore, we propose modulation of the strain with the gate-source voltage (V_{GS}).

Common techniques to induce strain, such as the use of materials with a built-in stress or lattice mismatch, result in a constant strain. They cannot modulate the strain with V_{GS}, however, with a piezoelectric (PE) layer, this becomes possible. In [13], a complete substrate was strain modulated with a PE layer. We proposed [14] to attach the PE layer to an individual transistor and bias the PE layer with the V_{GS} of that transistor. Related to our paper is the PE switch [15], where the strain dependent resistivity of a low-stiffness material is modulated using a PE layer.

A straightforward method to induce strain modulation is to replace the dielectric in a bulk transistor with a PE layer. Unfortunately, for every volt across the PE, the resultant conduction band (CB) deformation is much smaller than 1 eV. Hence, the resultant SS cannot drop below 60 mV/decade.

Here, we use an alternative solution. To induce strain, in a FinFET, by compressing it with a V_{GS}-biased PE layer. This paper extends our previous work by providing a theoretical framework for the modeling, design, and optimization, and as a result, more effective strain modulation.

II. Subthreshold Current

To investigate the relation between strain and subthreshold current, we recall the analytical model of [16], and show the influence of strain on the subthreshold current. The complete model is quite extensive, however, we point out the relevant strain-dependent terms. The model is based on a solution to the Poisson equation with the parameter β, to be evaluated for the potential V at both the drain $\beta(d)$ and source $\beta(s)$ sides as follows:

$$\frac{q\,(V_{\mathrm{GS}}-\Delta\phi-V)}{2k_{\mathrm{B}}T}-\ln\left[\frac{2}{w_{\mathrm{S}}}\sqrt{\frac{2\kappa_{\mathrm{s}}\epsilon_0 k_{\mathrm{B}}T}{q^2 n_{\mathrm{i}}}}\right]=\ln\beta-\ln[\cos\beta]+\frac{2\kappa_{\mathrm{s}}t_{\mathrm{ox}}}{\kappa_{\mathrm{ox}}w_{\mathrm{S}}}\beta\tan\beta \quad (1)$$

where q is the elementary charge, $\Delta\phi$ is the gate metal semiconductor work function difference, k_{B} is the Boltzmann constant, T the temperature, κ_{ox} and κ_{s} are the dielectric and semiconductor dielectric constants, ϵ_0 is the vacuum permittivity, n_{i} is the intrinsic carrier density, w_{S} is the fin width, and t_{ox} is the gate dielectric thickness. For a narrow FinFET, the channel quantum well in the low-field subthreshold condition results in a constant offset of the band edges, which has no effect on the SS and therefore is not considered. For a given V_{GS}, the parameters $\beta(d)$ and $\beta(s)$ can be evaluated, from which the drain current can be calculated as follows:

$$I_{\mathrm{DS}}=\mu\frac{t_{\mathrm{S}}}{L}\frac{4\kappa_{\mathrm{s}}\epsilon_0}{w_{\mathrm{S}}}\left(\frac{2k_{\mathrm{B}}T}{q}\right)^2\times\left[\beta\tan\beta-\frac{\beta^2}{2}\frac{\kappa_{\mathrm{s}}t_{\mathrm{ox}}}{w_{\mathrm{S}}\kappa_{\mathrm{ox}}}\beta^2\tan^2\beta\right]_{\beta(d)}^{\beta(s)}. \quad (2)$$

A few percent strain can increase the mobility μ by a factor three [17]–[19], while at the same time, the subthreshold

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current may increase by a factor 100 [12] because of changes in both the bandgap E_G and electron affinity χ_S. Therefore, while investigating the strain effect on the SS, we focus on the band deformation solely. The deformation is present in the model in (1) via the work function difference $\Delta\phi$ and intrinsic carrier density n_i:

$$\Delta\phi = \phi_m - \chi_S - \frac{E_G}{2}$$
$$n_i = \sqrt{N_C N_V \exp\left(\frac{-E_G}{u_t}\right)} \tag{3}$$

where ϕ_m is the metal workfunction, N_C and N_V are the CB, respectively, VB densities of states, and u_t is the thermal voltage.

Strain, indicated by ε, is the relative deformation of a material. The deformation can be along the crystal axes, or a shear type. The latter can be neglected in this paper because the forces are applied in directions along the crystal axes. In general, strain is uni or biaxial, meaning that the material is compressed along one axis and elongated along another. In the case of Si, the energy bands become nondegenerate, the valleys split up into three different band minima. These minima are located in the Δ valleys. The offset of the valleys can be calculated with the band deformation model as follows [20]:

$$\Delta E_{C,k} = \Xi_d(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) + \Xi_u\varepsilon_{kk},$$
$$\Delta E_{V,k} = -a(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) \pm\sqrt{\frac{b^2}{2}\left((\varepsilon_{xx}-\varepsilon_{yy})^2+(\varepsilon_{yy}-\varepsilon_{zz})^2+(\varepsilon_{xx}-\varepsilon_{zz})^2\right)} \tag{4}$$

where Ξ_d, Ξ_u, a, and b are the deformation potentials, given in Table II. The ± sign separates the heavy and light hole bands. In subthreshold, the number of carriers is relatively low, and therefore there is enough place for all carriers at the lowest energy level available. Thus, the effective bandgap is given by $E_G = E_{G0} + \min(\Delta E_C) - \max(\Delta E_V)$, and the electron affinity by $\chi_S = \chi_{S0} - \min(\Delta E_C)$, where E_{G0} and χ_{S0} are the relaxed bandgap and electron affinity.

From (1), it can be observed that a decrease of $\Delta\phi$ has the same effect on the current as an increase of V_{GS}. This can be achieved by a higher χ_S in (3), which in turn can be realized with a strong compressive (negative) strain in (4). In a transistor where the negative strain increases together with V_{GS}, these two effects would sum up, resulting in an extra increase of the current.

To illustrate the effect of strain on the subthreshold current, we modeled the current in a n-type Si FinFET with a V_{GS}-dependent strain along the z-axis (ε_{zz}), the strain along the other axes, (ε_{xx} and ε_{yy}), are negative and proportional to ε_{zz} according to the Poisson ratio. The modeling results are shown in Fig. 1. Negative strain results in an exponential increase, whereas a positive strain results in a very small increase of the subthreshold current. When the strain is, however, V_{GS} dependent, a significant change can be observed. When the transistor turns on, the strain increases, lowering ΔE_C, resulting in an additional increase of the current with V_{GS}.

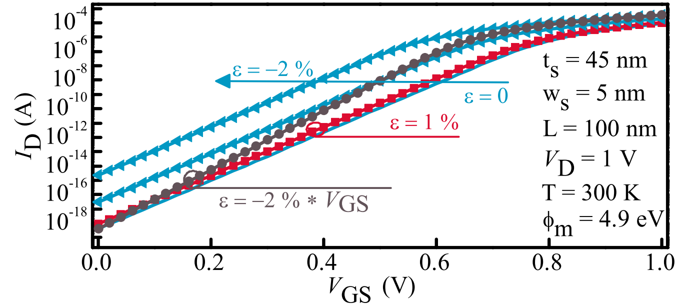

Fig. 1. Modeled transfer characteristics of a FinFET for various conditions of strain ε_{zz}. Blue lines: various static negative strain levels, showing an increase of the subthreshold current with increasing negative strain. Red line: static positive strain results in a very small increase of the current because of the negative strain along the other axes. Black line: V_{GS}-dependent negative strain, resulting in a steeper SS.

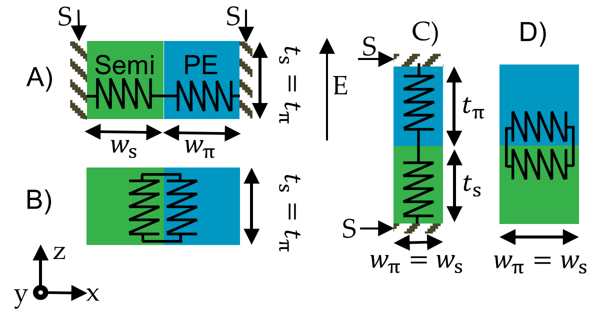

Fig. 2. Four basic configurations to induce strain into a semiconductor using a PE layer. The electric field is shown as E in this figure. The highlighted boundaries of configurations A and C are stiff, hence the displacement perpendicular to the boundary is zero.

III. One-Dimensional Strain Modulation

The previous section showed that in Si, a negative strain is required to effectively modulate the subthreshold current. We propose to induce the stress with a PE material, in these materials, dipoles are present along one of the crystal axes. If the material is subjected to a force, these dipoles displace, and become electrically charged, this is the PE effect. The opposite also holds, when subject to an electric field, the material displaces, which is called the converse PE effect [21].

It has been shown [13] that a PE material can be used to strain a substrate through the converse PE effect and thus modulate the current of transistors on the substrate. To increase the SS of a complete IC, the strain of each transistor has to become a function of its own V_{GS}. To do this effectively a geometry that can induce a large negative strain into the semiconductor layer is required.

In Fig. 2, various geometries are proposed. Two of them use symmetric boundaries on the sides, labeled S in this figure. The material at the boundary can move only along the boundary plane, which lead to a compression of the semiconductor when the PE expands. The relationship between stress and strain is governed by the PE constitutive equation [21]:

$$T = -eE + c\varepsilon \tag{5}$$

where T is the stress, e is the PE charge constant, E is the electric field, c is the stiffness, and ε is the strain. If the PE

TABLE I
MAXIMUM OBTAINABLE STRAIN FOR $V_{DD} = 1$ V AND CORRESPONDING OPTIMIZED DIMENSIONS, Si AND AlN

	ε_{xx} [%]	ε_{zz} [%]	w_S [nm]	w_π [nm]	t_S [nm]	t_π [nm]
A	0.05		5	103		10
B		0.07	5	21		10
C		-0.17			0.2	10
D	-0.025				1	10

layer is free to move, the resultant stress is zero, meaning that all the applied electric forces result in strain. When an additional layer is connected to the PE layer, stress will build up and the resultant strain will depend on the properties and dimensions of both layers.

A 1-D model for the strain can be found in our earlier work [14]. The model assumes both layers to behave like either a series or a parallel connection of springs. The stiffness is taken from the elasticity matrix, the dimensions of the springs are equal to the dimensions of the layers.

In configuration C, the thickness of the semiconductor can be adjusted to tune the resultant strain. A 1-D model for such a device including gate dielectric and gate metal layers is given in (6b). When both the gate metal (w_g) and dielectric thickness (w_{ox}) are set to zero, the result becomes equivalent to configuration C. As long as $w_s/c_s \ll w_\pi/c_\pi$, a close to maximum strain is found, hence we use use $w_s/c_s = 0.1 w_\pi/c_\pi$.

Each of the four configurations has such a scalable dimension, and for each of them, we tailored the dimensions such that maximum strain is obtained. We compare the different configurations with AlN and Si as materials only and assume that the results are qualitatvely comparable with other possible material combinations. This is justified by the fact that the material parameter values, as shown in Table II, are in the same order. The results are shown in Table I. Configuration C is most effective in inducing a large negative strain in the semiconductor.

Two things are required to obtain a large CB deformation. First, a PE layer that is able to exert a large force on the semiconductor, which can be evaluated from (5). Second, a semiconductor with a large band deformation per applied pressure.

To calculate the resultant band deformation per applied pressure, we assume that the resultant strain is uniaxial. This is justified by the high aspect ratio and resultant uniaxial strain of the structures proposed in this paper, as shown in Fig. 5. Furthermore, the shear strain is set to zero.

The CB offset for Si is calculated for the Δ valleys as in (4), likewise the Ge offset is calculated for the L valleys [22], which, in our case, results in $\Delta E_C = (\Xi_u + \Xi_d)(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz})$. In the hetero (III–V) materials the CB minimum is given by the Γ valley, of which the offset is given by $\Delta E_C = a_c(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz})$ [23], where the deformation potential a_c is negative, and hence the III–V materials require positive strain instead to increase the subthreshold current. The VB offset for all semiconductor materials is calculated from (4), the material parameters are shown in Table II.

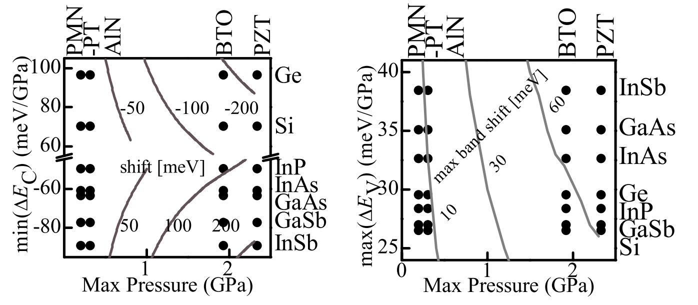

Fig. 3. Horizontal axis shows the maximum pressure in a PE material, calculated from the PE parameters and the maximum field. On the vertical axis, the band–band edge shift per unit of pressure for various semiconductors is shown. Contour lines: the maximum obtainable band deformation using structure C. Dots: the location of various material combinations on the contour plot. Note that the Si and Ge data points coincide on the right.

TABLE II
MATERIAL PROPERTIES OF THE MATERIALS USED IN THIS PAPER. e AND c ARE THE PE CHARGE AND STIFFNESS CONSTANTS. E_{cr} IS THE MAXIMUM ELECTRIC FIELD AT WHICH THE PE STILL SHOWS PROPER BEHAVIOR

	c_{11} [GPa]	c_{12} [GPa]	c_{13} [GPa]	c_{33} [GPa]	e_{33} [C/m^2]	e_{31} [C/m^2]	E_{cr} [MV/m]
AlN [24]	345	125	120	395	1.6	-0.5	200
BTO [21]	150	66	66	146	18	-4.4	110 [25]
PMN-PT [26]	115	103	102	103	20	-3.9	10 [27]
PZT [28]	127	80	85	117	23	-6.6	100 [29]
	c_{11} [GPa]	c_{12} [GPa]	Ξ_u [eV]	Ξ_d [eV]	a [eV]	b [eV]	
Si [30]	166	64	10.5	1.1	2.1	-2.33	
Ge [30]	129	48	16.8	-4.43	2.0	-2.16	
	c_{11} [GPa]	c_{12} [GPa]	a_c [eV]		a [eV]	b [eV]	
GaAs [22]	113	57	-7.17 [23]		1.16 [23]	-2.79	
GaSb [22]	88	40	-6.85 [23]		-.79 [23]	-1.6	
InAs [22]	83	45	-5.08 [23]		1.00 [23]	-1.72	
InSb [22]	69	38	-6.17 [23]		0.36 [23]	-2.3	
InP [22]	101	56	-5.04 [23]		1.27 [23]	-1.6	
	c_{11}	c_{12}					
SiO2 [31]	57	11.4					
HfO2	220 [32]	66 [33]					
TiN [34]	640	160					

In Fig. 3 these two performance parameters are compared for structure C, and contour lines are drawn showing the maximum CB and VB deformation for given material parameters. Note that the pressure in the PE is positive, resulting in a negative pressure in the semiconductor. For effective strain modulation in an n-type transistor a large CB deformation is required, and likewise in a p-type transistor, a large VB deformation is beneficial.

Fig. 3 shows that strain modulation is most effective in an n-type Ge transistor. As a PE material, we choose PZT because it is able to exert a large force.

IV. THREE-DIMENSIONAL STRAIN MODULATION

In the previous section, we have shown that the CB can be modulated well with a PE layer. Here, these results are extended to a 3-D FinFET of Fig. 4. The bias on the PE layer is V_{GS}. The orientation of the layer should be such that it expands along the z-axis and compresses the semiconductor.

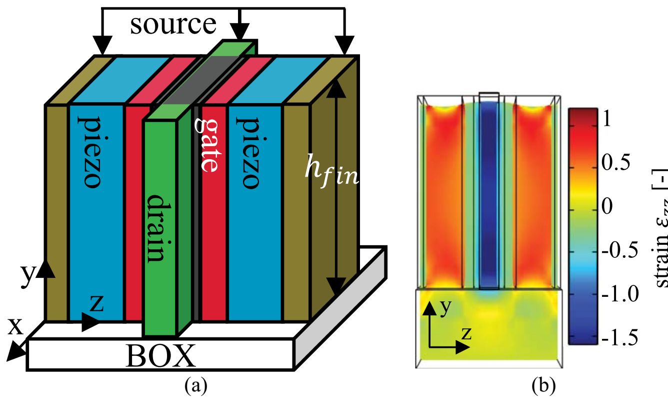

Fig. 4. (a) Proposed strain modulated FinFET, with gate, oxide, and source layers. The current flow is along the one-axis. The extension of the PE along the three-axis compresses the semiconductor. (b) FEM simulation result for the Ge FinFET with PZT PE for strain modulation at $V_{GS} = 1$ V showing three-axis strain ε_{zz} on the yz-plane.

The structure can be made repetitively, therefore the displacement at the xy oriented source metal surfaces has to be zero, resulting in a symmetry boundary condition.

In the previous section, PZT was chosen however, this material is also ferroelectric (FE) [35]. This means that if the electric field changes sign, the polarization changes accordingly, resulting in negative PE constants. When the electric field changes sign again, the polarization follows accordingly. Therefore, we conclude that if the sign of the electric field is constant, then an FE can be approximated as a PE material.

Two layers of PE material are shown in Fig. 4. Subjected to the same V_{GS} bias, both have a different sign in the electric field. One of the layers has a negative electric field, therefore, also the dipole orientation will be negative, resulting in an equal eE product [35], and hence the same strain value.

With a 3-D FEM simulator [36], we simulated the PE effect, Fig. 4 shows the compression of the semiconductor by the PE layers. Compression is negative strain; this reduces the bandgap, which exponentially increases the subthreshold current.

We now continue with the derivation of a 1-D model to estimate and understand the parameter and geometry dependence of the strain. The strain in a material is governed by (5), where for non PE materials $e = 0$. Because of repetitive structure, the displacement at the boundaries is zero. Therefore, the sum of the material displacements has to be zero, this boundary condition is implemented in (6a). Substituting (5) for the strain term, and considering that the force has to be equal everywhere we find (6b):

$$w_S\varepsilon_s + w_{ox}\varepsilon_{ox} + w_g\varepsilon_g + w_\pi\varepsilon_\pi = 0 \tag{6a}$$

$$T = \frac{eV}{c_\pi}\left(\frac{w_S}{c_s} + \frac{w_{ox}}{c_{ox}} + \frac{w_g}{c_g} + \frac{w_\pi}{c_\pi}\right)^{-1}. \tag{6b}$$

From the pressure T and (5), the strain for various layers can be calculated. For the sake of convenience, the source connection to the PE is of the same material as the gate metal and has an equal thickness. A smaller width of the layers relative to the PE layer contributes to an increase in the strain. We use a 1.5-nm-thick HfO2 layer as an insulator, and a 3-nm-thick TiN as a gate metal because both have relatively high stiffness. All the material parameters are shown in Table II. To verify the simple 1-D model, in Fig. 5 we compare the model with results obtained from FEM simulation.

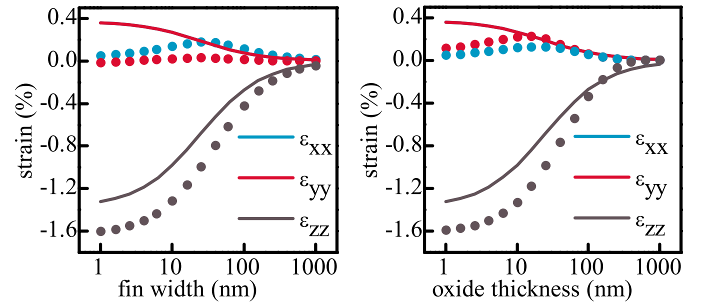

Fig. 5. Modeled (lines) strain ε_s and simulated (symbols) average strain ε_{zz} as a function of w_S and w_{ox}, clearly showing an increase for smaller fin width and oxide thickness. ε_{xx} and ε_{yy} in our model were obtained using the Poisson ratio.

The model is in good agreement, however, underestimates the strain for a very thin dielectric and fin width. The difference is acceptable as the model is 1-D, and the simulations are 3-D and considers all the different boundary conditions, dimensions, and substrate layers. For large fin width, the right-hand term of (6b) goes to zero, and so does the strain ε_{zz}. On the other hand, for a small fin width, the term w_S/c_s becomes zero and the strain is limited by the other layers. A close to maximum strain can be found at a realistic 5-nm fin width. The graph also shows that the x- and y-axes strain is positive, and becomes small for very narrow fins.

V. Results

In most of the semiconductor device simulators, the strain is assumed to be a constant, which is not the case with strain modulation. Therefore, special care was taken to change both V_{GS} and strain for every bias step. The results of the FEM simulator are used as an input for the device simulator [37]. This approach is not self-consistent, which is not required because the electric field is given by V_{GS}/t_π. Fig. 6 shows simulated transfer characteristics as well as the result of the analytical current model of Section II for the Ge strain modulated FinFET. For comparison, equal devices with constant strain are also shown. The strain modulation clearly results in the off-current of a device without strain, and lower threshold voltage of a device with strain. From the graphs, the SS is found to be 59 mV/decade for the devices with constant strain, which is the thermal limit for diffusion current. With strain modulation, the SS, however, reduces to 50 mV/decade. Therefore, strain modulation may lead to novel steep subthreshold slope devices.

VI. Considerations

In this paper, the thickness of the PE is chosen to be equal to the fin height. Simulations [15] showed the possibility of increasing the applied stress by increasing the area of the PE layer.

This paper showed the strain dependence of the FinFET, however, any device with a significant current dependence on the strain is a candidate for strain modulation. For example,

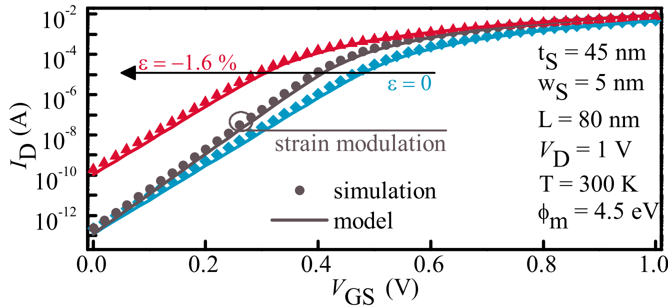

Fig. 6. Simulated and modeled transfer characteristics of a FinFET (Fig. 4) with strain modulation and with constant strain. Clearly, strain modulation results in a steeper subthreshold slope.

the B2BT FET has a strong strain dependence [14] and may be of interest for strain modulation.

In this paper, the focus was on the strain effect on the subthreshold current. However, for devices also the ON-current, and hence the strain-dependent mobility, needs to be considered. The strain is strongly compressive and orthogonal to the transport direction. In the Si FinFET, this results in an enhanced carrier mobility [30], [38]. In Ge, this has a positive effect on the mobility of holes, however, reduces the mobility of electrons slightly [30].

An other issue of concern is reliability, in PZT, this is ofted adressed as fatigue, which is the reduced polarization of the PE layer after about 10^9 switches [39]; however, our device does not switch the polarization, and hence may endure much longer. Furthermore, the presence of lead in the PZT layer, which may diffuse into the semiconductor, and the continuous change of the strain-inducing delamination could become reliability issues.

The speed at which the strain can build up, which we estimate with the acoustic velocity $v_a = \sqrt{c_{33}/\rho}$ [40], where ρ is the mass density [21], sets a limit to the maximum operating speed of a strain modulated transistor. The distance from the edge of the PE layer to the middle of the fin is about 17 nm. Most of this is in the PZT layer, which also has a relatively low acoustic velocity of 2.8 nm/ps. Hence, the limit to the operating speed is in the range of 5 ps.

The goal of a steep subthreshold device is power reduction in ICs. With strain modulation, we are able to reduce the leakage current. This will result in smaller static power. The added PE capacitance will, however, increase the dynamic power. Therefore, one can only benefit from strain modulation if the static power of an IC is significantly larger then the dynamic power.

Altogether strain modulation requires an input capacitance, which increases the dynamic power consumption, additionally the use of PE layer adds limits to both the switching speed and lifetime of a circuit. As a result, strain modulation may find applications in low-power circuits.

VII. Conclusion

By combining a compact model for a FinFET and a band deformation model, we showed that with a negative strain, we are able to increase the subthreshold current significantly. If the negative strain is V_{GS} dependent, than this can result in a smaller SS. To induce this strain, we propose to use a PE layer biased with V_{GS}, and oriented such that it compresses the transistor with increasing bias. With FEM simulation, we derived the resultant strain. Both simulation results, and a 1-D analytical model, showed that very thin layers are favorable to obtain large strain values. By combining 3-D FEM and 2-D device simulations, transfer characteristics of the proposed device were obtained. These showed that with the PE, the lower off-current of a relaxed transistor can be combined with the lower threshold voltage of a strained transistor. In our example, this results in a 50 mV/decade SS. This is below the theoretical limit of 60 mV/decade for normal transistors suggesting that strain modulation can open a new road to steep subthreshold slope devices.

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