Solid-State Electronics 113 (2015) 28–34

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

Physics-based stability analysis of MOS transistors ☆

A. Ferrara [a,*], P.G. Steeneken [b,c], B.K. Boksteen [a], A. Heringa [b], A.J. Scholten [b], J. Schmitz [a], R.J.E. Hueting [a]

[a] MESA+ Institute for Nanotechnology, University of Twente, Enschede, The Netherlands
[b] NXP Semiconductors, The Netherlands
[c] Delft University of Technology, Delft, The Netherlands

ARTICLE INFO

Article history:
Available online 10 June 2015

Keywords:
Power MOSFET
Silicon-on-insulator (SOI)
Safe Operating Area (SOA)
Safe Operating Volume (SOV)
Stability factor
Failure function

ABSTRACT

In this work, a physics-based model is derived based on a linearization procedure for investigating the electrical, thermal and electro-thermal instability of power metal–oxide–semiconductor (MOS) transistors. The proposed model can be easily interfaced with a circuit or device simulator to perform a failure analysis, making it particularly useful for power transistors. Furthermore, it allows mapping the failure points on a three-dimensional (3D) space defined by the gate-width normalized drain current, drain voltage and junction temperature. This leads to the definition of the Safe Operating Volume (SOV), a powerful frame work for making failure predictions and determining the main root of instability (electrical, thermal or electro-thermal) in different bias and operating conditions. A comparison between the modeled and the measured SOV of silicon-on-insulator (SOI) LDMOS transistors is reported to support the validity of the proposed stability analysis.

© 2015 Elsevier Ltd. All rights reserved.

1. Introduction

In power transistors, failure is often associated with instability, which causes one or more device parameters, such as current, voltage or temperature, to runaway [1]. Stability can be experimentally investigated by measuring the device characteristics close to the failure limit [2–6]. This allows calculation of a stability factor that is a measure of the device sensitivity to runaway. However, such a procedure has two drawbacks: (1) it can affect the device performance by changing parameters such as threshold voltage, on-resistance and breakdown voltage and (2) it detects the occurrence of instability but not its physical origin (electrical or thermal).

In order to overcome the first drawback, physics-based models [2,3,5,7,8] or TCAD simulations [9] have been used to predict and quantify instability. However, modeling and simulating runaway effects causes the output parameters to diverge and makes it difficult to identify the physical origin of the numerical instability.

The physics-based stability analysis can be used to identify the boundary between electrical and thermal failure mechanisms in LDMOS transistors (Fig. 1), hence to distinguish the root cause of device failure [10]. In comparison to our earlier work [10], the derivation of the stability factors is elaborated with further mathematical detail, making it generally applicable to any kind of MOS transistor. The electrical and thermal stability factors are defined assuming that self-heating does not play a role in the electrical runaway, while avalanche breakdown and the internal parasitic bipolar transistor of the MOS transistor do not affect thermal stability.

Device failure can be related to an electro-thermal stability factor that includes both the electrical and thermal failure mechanisms (Fig. 2). The individual analysis of runaway mechanisms allows determination of the relative contributions of electrical and thermal phenomena to failure, thus identifying the primary cause of runaway. This knowledge allows one to determine, depending on the operating conditions, whether the electrical or thermal device properties, or both, need to be improved to increase the so-called Safe Operating Area (SOA), *i.e.* the two-dimensional (2D) frame work in the current–voltage plane where it is safe to operate the LDMOS [11,12].

The stability equations need to be combined with models of the different MOS current contributions (intrinsic MOS current I_{dMOS}, bipolar base and collector currents I_b and I_c, and impact ionization current I_{ii}) including their temperature dependencies. For this purpose analytical models for MOS transistors, TCAD simulations, experimental data or combinations can be used [2,3,5,7–9,13]. In this work, physics-based analytical expressions [14,15] with experimental [6] fitting parameters have been used (Appendix A). As shown in [10] for SOI LDMOS transistors, the proposed model

☆ This work is a part of the Dutch Point-One program and is supported financially by Agentschap NL, an agency of the Dutch Ministry of Economic Affairs.

* Corresponding author.
E-mail address: a.ferrara@utwente.nl (A. Ferrara).

http://dx.doi.org/10.1016/j.sse.2015.05.010
0038-1101/© 2015 Elsevier Ltd. All rights reserved.

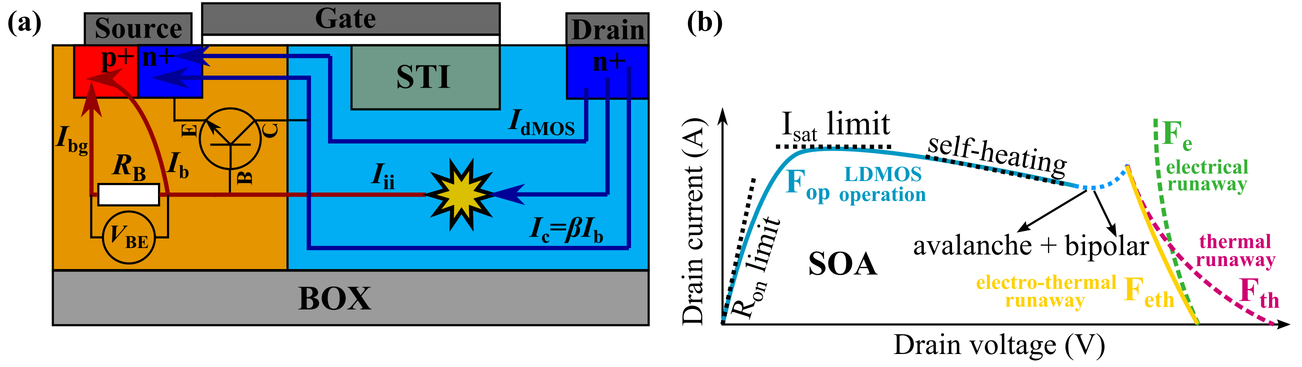

Fig. 1. (a) Parasitic bipolar and avalanche multiplication in the operation of an LDMOS transistor. (b) Schematic of the Safe Operating Area (SOA), showing the failure and operating functions which are analytically investigated in this work.

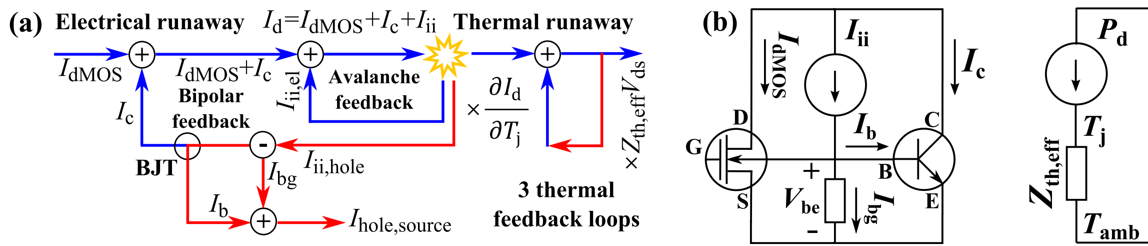

Fig. 2. (a) Schematic representation of the origin of electrical and thermal runaway. (b) Electro-thermal circuit model of the MOS-bipolar system.

allows mapping the failure points onto a 3D space defined by the gate-width normalized drain current, drain voltage and junction temperature. This leads to the definition of the failure functions and the introduction of the Safe Operating Volume (SOV).

2. Origin of electro-thermal runaway

A general overview of the positive electrical and thermal feedback mechanisms leading to instability and runaway is provided in Fig. 2. At high drain voltages V_{ds}, the MOS electron current I_{dMOS} generates electron–hole pairs contributing to an impact ionization current I_{ii} with an electron and a hole component. The electrons flow towards the highly doped n^+ drain contact, the holes flow towards the p^+ body contact inducing a voltage drop V_{be} over the base resistance R_B. This switches on the internal parasitic bipolar with a base current I_b and a corresponding collector current $I_c \approx \beta I_b$, where β is the current gain. This current I_c is in turn multiplied by avalanche when flowing in the drift extension, resulting in a positive feedback behavior. Self-heating [5,8,16] is included in the model by introducing an effective thermal impedance $Z_{th,eff} \approx (T_j - T_{amb})/P_d$ [6], where it is assumed for simplicity that the dissipated power P_d is independent of the pulse time t_{pulse}.

Electrical failure occurs because of the interaction of the parasitic bipolar with the current I_{ii}. Part of this current flows through the base of the bipolar and contributes to $I_c \approx \beta I_b$, which is avalanche multiplied and fed back into the base. Thermal failure can occur because of thermal runaway in each of the current components I_{dMOS}, I_c or I_{ii}. The temperature coefficient of I_{dMOS} depends on V_{gs} [17], I_{ii} has a slightly-negative temperature coefficient [18] (not included in the model), and I_c has a positive temperature coefficient [19]. In most cases, the increase in I_c (also including thermal leakage) induced by self-heating determines thermal instability [2,3,5,8]. However, for V_{gs} below the zero-temperature coefficient point, I_{dMOS} also contributes to instability [5,8,17].

For studying the failure mechanisms the so-called stability factors [1] are required. The complete derivation of the stability factors is carried out in Section 3. Although electrical and thermal failure mechanisms often both play a role in transistor failure, their relative contributions can be identified using the analytical stability analysis described in the same section. The electro-thermal behavior of the MOS transistor is described by combining the electrical and thermal contributions to stability in a coupled equation system. The large signal behavior of the MOS transistor including the parasitic bipolar transistor and self-heating can be described as follows:

$$\begin{cases} I_{dn} = M \cdot \frac{(I_{dMOS}+I_c)}{W_{gate}} = f_e(V_{gs}, V_{ds}, V_{be}, T_j) & \text{(a)} \\ T_j = T_{amb} + Z_{th,eff}(t_{pulse}, A) W_{gate} V_{ds} I_{dn} & \text{(b)}, \end{cases} \quad (1)$$

where I_{dn} is the drain current per unit gate width W_{gate}, I_{dMOS} is the internal MOS drain current, V_{gs} the gate-source voltage, V_{ds} is the drain-source voltage, V_{be} is the base-emitter voltage, T_j is the junction temperature, and T_{amb} is the ambient temperature. The effective thermal impedance $Z_{th,eff}$ depends on the pulse time t_{pulse} and the device area A, and the multiplication factor M is a parameter that is a measure for the increased drain current caused by impact-ionization. The function f_e describes the electrical operation of the MOS-bipolar system depending on the applied biasing and junction temperature T_j. It can be constructed based on compact modeling, TCAD simulations or measurements on special test structures including a temperature sensor and/or a separate body contact. Hence, the electro-thermal behavior of the MOS transistor is described by (1) in case of large signal biasing.

3. Analytical stability analysis

3.1. Derivation of the electrical stability factor

In order to quantify the relative contributions of electrical [20] and thermal [5,8] runaway to coupled electro-thermal [2,9,21] failure mechanisms, analytical stability equations are derived following a linearization procedure. In this section, it is shown how the

electrical stability factor can be derived assuming an isothermal operation of the transistor (*i.e.*, no self-heating). For this purpose, it is useful to refer to the electrical equivalent circuit shown in Fig. 2b. The feedback equation for electrical stability is obtained by solving the node equation at the base of the parasitic bipolar:

$$I_{ii} = I_b + I_{bg}, \quad \text{with} \quad I_{ii} = (M-1)(I_c + I_{dMOS}), \tag{2}$$

where I_{bg} is the (hole) back-gate current and M is the multiplication factor. Further,

$$I_b = \frac{I_c}{\beta} = I_S \exp\left(\frac{V_{be}}{V_T}\right) \quad \text{and} \quad I_{bg} = \frac{V_{be}}{R_B}, \tag{3}$$

where I_S is the saturation current of the reverse-biased base–collector junction of the parasitic bipolar, and V_T is the thermal voltage ($V_T = \frac{kT_j}{q}$, with k being the Boltzmann constant and q the electron charge). The electrical feedback equation can be rewritten as:

$$[1-\beta(M-1)]I_c + \beta\frac{V_{be}(I_c)}{R_B} = \beta(M-1)I_{dMOS}, \tag{4}$$

which is nonlinear because of the dependence $V_{be}(I_c)$. In order to find the electrical instability condition, the problem can be linearized around a fixed bias point.

Generally it can be stated for the current that (neglecting second order terms):

$$I(V,T) \approx I(V_0,T_0) + g(V-V_0) + \phi(T-T_0) = I(V_0,T_0) + gv + \phi t, \tag{5}$$

where V_0 is the fixed (DC) bias point and T_0 is the fixed (ambient) temperature. Hence the small-signal parameters are introduced:

$$i = I - I_0, \quad v = V - V_0 \quad \text{and} \quad t = T - T_0. \tag{6}$$

Further, the transconductance and the temperature coefficient can be respectively written as

$$g = \left.\frac{\partial I}{\partial V}\right|_{T_0} \quad \text{and} \quad \phi = \left.\frac{\partial I}{\partial T}\right|_{V_0}. \tag{7}$$

More specifically, the parameters V_{be}, I_b, I_c and I_{dMOS} are written as the sum of DC bias points and small signal parameters as follows:

$$V_{be} = V_{BE} + v_{be}, \quad I_c = I_C + i_c, \quad I_b = I_B + i_b \quad \text{and} \quad I_{dMOS} = I_{DMOS} + i_{dMOS}. \tag{8}$$

Then, the following small signal parameters of the parasitic bipolar transistor are introduced:

$$r_b = \frac{v_{be}}{i_b}, \quad \beta = \frac{i_c}{i_b} \quad \text{and} \quad g_m = \left.\frac{\partial I_c}{\partial V_{be}}\right|_{T_0} = \frac{i_c}{v_{be}} = \frac{\beta}{r_b}, \tag{9}$$

where r_b is the differential base resistance of the parasitic bipolar (notice that $r_b \neq R_B$), β is the current gain and g_m is the collector transconductance.

Equation (4) can be written in terms of small signal variations at each bias point as:

$$[1-\beta(M-1)]i_c + \frac{r_b}{R_B}i_c = \beta(M-1)i_{dMOS},$$

$$\text{giving} \quad i_c = \frac{\beta(M-1)}{1-\left[\beta(M-1) - \frac{r_b}{R_B}\right]}i_{dMOS}. \tag{10}$$

From (10), the electrical stability factor S_e for the collector current is given by

$$S_e = \beta(M-1) - \frac{r_b}{R_B}. \tag{11}$$

Using the calculated collector current i_c, the total electron drain current i_d including the MOS, bipolar transistor and avalanche contributions can be calculated by introducing the multiplication factor $M = \frac{1}{1-\alpha}$ (α is the avalanche coefficient [22]) as follows:

$$i_d = M(i_{dMOS} + i_c) = \frac{1}{1-\alpha}\cdot\frac{1+\frac{r_b}{R_B}}{1-S_e}i_{dMOS}. \tag{12}$$

Electrical instability occurs when $\left.\frac{\partial I_d}{\partial V_{ds}}\right|_{T_j} \to \infty$. From (12), it can be seen that the drain current diverges when $\alpha = 1$ (avalanche breakdown) or when $S_e = 1$ (electrical runaway of the collector current). In practical cases, avalanche breakdown dominates electrical failure for low gate voltages when the drain current is low and the electric field magnitude is large, while bipolar runaway mainly occurs at high gate voltages and can be significantly enhanced by self-heating, as discussed in the next subsections.

3.2. Derivation of the thermal stability factor

In order to find an expression for the thermal stability factor, small signal temperature variations should also be included in the analysis. The junction temperature T_j is split into a DC and a small signal component according to:

$$T_j = T_J + t_j. \tag{13}$$

Relating the junction temperature T_j to the dissipated power $P_d = I_d V_{ds}$ through the thermal impedance $Z_{th,eff}$ and separating the DC from the small signal components yields:

$$T_j = T_{amb} + Z_{th,eff} I_d V_{ds} = T_{amb} + Z_{th,eff}(I_D + i_d)(V_{DS} + v_{ds}). \tag{14}$$

From (14), the small signal temperature variation can be expressed (neglecting second order terms) as:

$$t_j = Z_{th,eff}(I_D v_{ds} + V_{DS} i_d). \tag{15}$$

The small signal drain current i_d is related to t_j via its temperature coefficient ϕ_d according to (see (5) and (7)):

$$i_d = g_d v_{ds} + \phi_d t_j, \tag{16}$$

where g_d is the drain conductance. In this section, only runaway caused by thermal instability is investigated and electrical effects are neglected. Substituting i_d from (16) into (15) and setting $v_{ds} = 0$ (meaning that the device operates at constant drain voltage V_{DS}) gives

$$t_j = Z_{th,eff} V_{DS} \phi_d t_j, \tag{17}$$

which is a feedback equation for the small signal temperature increase t_j. Thermal instability occurs when $\left.\frac{\partial I_d}{\partial T_j}\right|_{V_{ds}} \to \infty$. From (17) it follows that the junction temperature diverges when the thermal stability factor

$$S_{th} = Z_{th,eff} V_{DS} \phi_d \tag{18}$$

reaches unity. The temperature coefficient ϕ_d includes both the MOS contribution ϕ_{dMOS} and the bipolar contribution ϕ_{cNPN} and can be expressed as the sum of the two in the calculation of S_{th}:

$$\phi_d = \phi_{dMOS} + \phi_{cNPN}. \tag{19}$$

In (19), the temperature dependence of the multiplication factor M has been neglected. More specifically, the total derivative of M with respect to the drain voltage V_{ds} can be expressed as:

$$\frac{dM(T_j, V_{ds})}{dV_{ds}} = \frac{\partial M}{\partial T_j}\cdot\frac{dT_j}{dV_{ds}} + \frac{\partial M}{\partial V_{ds}}. \tag{20}$$

At first order, $\left|\frac{\partial M}{\partial T_j}\right| \ll \left|\frac{\partial M}{\partial V_{ds}}\right|$ since M strongly increases with the drain bias V_{ds}. For this reason, the assumption $M(T_j, V_{ds}) \approx M(V_{ds})$ is taken in this work, which also simplifies the algebra for the calculation of the electro-thermal stability factor derived in the next subsection.

3.3. Derivation of the electro-thermal stability factor

By combining the electrical and thermal contributions to stability, the electro-thermal stability factor S_{eth} is derived in this subsection. For this purpose, (15) and (16) are combined in a coupled small-signal system giving:

$$\begin{cases} i_d = g_d v_{ds} + \phi_d t_j & \text{(a)} \\ t_j = Z_{th,eff}(I_D v_{ds} + V_{DS} i_d) & \text{(b)} \end{cases} \tag{21}$$

The conductance g_d and the temperature coefficient ϕ_d need to be expressed as a function of the MOS (g_{dMOS} and ϕ_{dMOS}) and bipolar (g_c and ϕ_c) contributions by accounting for the electrical feedback equation (10). The small signal electro-thermal equations for the MOS drain current i_{dMOS} and the collector current i_c are:

$$i_{dMOS} = g_{dMOS} v_{ds} + \phi_{dMOS} t_j \tag{22}$$

$$i_c = g_m v_{be} + \phi_{cNPN} t_j \tag{23}$$

Since i_c is a function of v_{be} while i_{dMOS} is a function of v_{ds}, we first look for an expression where i_c is also expressed as a function of v_{ds} in the form:

$$i_c = g_c v_{ds} + \phi_c t_j. \tag{24}$$

For this purpose, (22) and (23) are substituted into (10), yielding, after some algebraic manipulations:

$$g_c = \frac{\beta(M-1) g_{dMOS}}{1 - \left[\beta(M-1) - \frac{r_b}{R_B}\right]} \tag{25}$$

$$\phi_c = \frac{\beta(M-1)\phi_{dMOS} + \frac{r_b}{R_B}\phi_{cNPN}}{1 - \left[\beta(M-1) - \frac{r_b}{R_B}\right]}. \tag{26}$$

The total drain current i_d is calculated as in (12) giving the following expressions for g_d and ϕ_d:

$$g_d = M \frac{1 + \frac{r_b}{R_B}}{1 - S_e} g_{dMOS} \tag{27}$$

$$\phi_d = M \frac{1 + \frac{r_b}{R_B}\left(1 + \frac{\phi_{cNPN}}{\phi_{dMOS}}\right)}{1 - S_e} \phi_{dMOS}. \tag{28}$$

By substituting (21)b into (21)a, the drain current i_d can finally be expressed as:

$$i_d = \frac{g_d\left(1 + Z_{th,eff} I_D \frac{\phi_d}{g_d}\right)}{1 - Z_{th,eff} V_{ds} \phi_d} v_{ds}. \tag{29}$$

Electro-thermal runaway occurs when $\frac{i_d}{v_{ds}} \to \infty$, which can happen in two cases: (1) $g_d \to \infty$; (2) $Z_{th,eff} V_{DS} \phi_d = 1$.

The condition (1) occurs when $M \to \infty$ ($\alpha = 1$) or $S_e = 1$ and corresponds to the electrical runaway discussed in Section 3.1. The condition (2) corresponds to the thermal runaway condition discussed in Section 3.2. However, in this case, the expression for the temperature coefficient ϕ_d is not given by (19), which only accounts for thermal phenomena, but by (28), which also accounts for the electrical feedback occurring at the base node of the bipolar. For this reason, it is natural to define the electro-thermal stability factor as (compare with (18)):

$$S_{eth} = Z_{th,eff} V_{DS} \phi_d = Z_{th,eff} V_{DS} \left[M \frac{1 + \frac{r_b}{R_B}\left(1 + \frac{\phi_{cNPN}}{\phi_{dMOS}}\right)}{1 - S_e} \right] \phi_{dMOS}. \tag{30}$$

In this expression it can be seen how electrical instability can trigger thermal runaway, since S_e appears as a feedback term in S_{eth} (electrically-induced thermal instability [2]).

4. The Safe Operating Volume (SOV)

4.1. The failure functions

The stability factors S_e, S_{th} and S_{eth} derived in the previous section can be associated to the corresponding failure functions F_e, F_{th} and F_{eth} defined such that $F_x(I_{dn}, V_{ds}, T_j) = S_x - 1$, with $x = e, th, eth$. The operating bias points up to which device failure does not occur define a volume described by:

$$V_x = \left\{(I_{dn}, V_{ds}, T_j) \in \mathbb{R}^3 : F_x(I_{dn}, V_{ds}, T_j) < 0\right\}. \tag{31}$$

For safe operation, all failure functions need to obey $F_x < 0$, and failure occurs when $F_{eth} = 0$ in practice since this condition always occurs before $F_e = 0$ and $F_{th} = 0$. The electro-thermal failure function F_{eth} can be determined from (1) a large-signal model by solving the system (1) or (2) a small-signal analysis as in Section 3.

Fig. 3a shows the modeled $I_{dn} - V_{ds}$ and $T_j - V_{ds}$ curves for $V_{gs} = 2V$ at three different ambient temperatures T_{amb} for an LDMOS transistor. The gate-width (W_{gate}) normalized drain current I_{dn} and the junction temperature T_j are found in each bias condition by solving the system (1). The base-emitter voltage V_{be} has to be determined numerically [7] in order to calculate I_c. The expressions used in this work for M, I_{dMOS}, I_c, I_b and their temperature dependencies are provided in Appendix A. The failure points at the edge of the SOA ($F_{eth} = 0$) where the large signal model stops converging are investigated by analyzing the temperature (T_j) behavior of failure functions as indicated by the circles in Fig. 3b. This analysis allows determination of the failure junction temperatures ($T_{j,fail}$) corresponding to electrical (T_{je}), electro-thermal (T_{jeth}) and thermal failure (T_{jth}). In all cases failure is limited by $F_{eth} = 0$ ($T_{j,fail} = T_{jeth}$), but there is a gradual boundary between thermal to electrical runaway as V_{ds}, and hence the multiplication factor M, increases and T_j reduces.

4.2. Influence of the device area and operating conditions

In Fig. 3c, the dependence of $F_{eth} = S_{eth} - 1$ upon the effective thermal impedance $Z_{th,eff}$ is investigated. The failure temperature is affected by $Z_{th,eff}$ mainly for low V_{ds}, where failure is thermally induced, while it tends to become independent of $Z_{th,eff}$ for large V_{ds}, where failure is electrically induced. However, if a safer operating failure criterion is used ($S_{eth} = 0$ rather[1] than $S_{eth} = 1$, red line in Fig. 3c, the failure temperature becomes independent of $Z_{th,eff}$ and therefore of ambient temperature, pulse time and device area. This is a significant result of this work. While in theory the electro-thermal runaway condition is given by $S_{eth} = 1$ [1] ($F_{eth} = 0$), experiments [6] show that the range $0 < S_{eth} < 1$ is often unsafe due to the high value of $\frac{dS_{eth}}{dV_{ds}}$. Therefore, a safer operating condition can be introduced that is given by $S_{eth} = 0$, which leads to a reduction of the estimated safe operating limits (mainly in the thermal runaway regime) but makes the SOV independent of $Z_{th,eff}$ (Fig. 3c). In practice, the condition $S_{eth} = 0$ cannot be achieved for V_{gs} values below the zero temperature coefficient point [17] since the temperature coefficient of the MOS current is positive in this range. For this reason, a practical value of $S_{eth} = 0.2$ was used in [6] for the different operating conditions, yielding a good trade-off between transistor safety and experimental accuracy.

[1] For interpretation of color in Fig. 5, the reader is referred to the web version of this article.

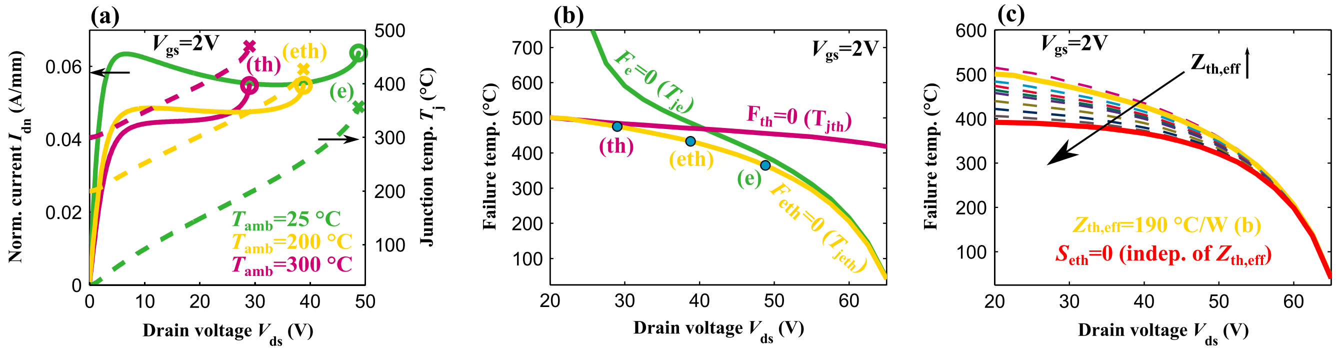

Fig. 3. (a) Modeled $I_{dn} - V_{ds}$ and $T_j - V_{ds}$ curves for $V_{gs} = 2$ V and three ambient temperatures T_{amb} until the edge of the SOA. (b) Failure temperature ($T_{j,fail}$) vs. V_{ds} for $V_{gs} = 2$ V showing the gradual boundary between thermal and electrical failure as V_{ds} increases and $T_{j,fail}$ reduces. (c) Same as (b) for different values of the effective thermal impedance $Z_{th,eff}$. The red line corresponds to a safer operating condition obtained for $S_{th} = 0$ rather than $S_{th} = 1$. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

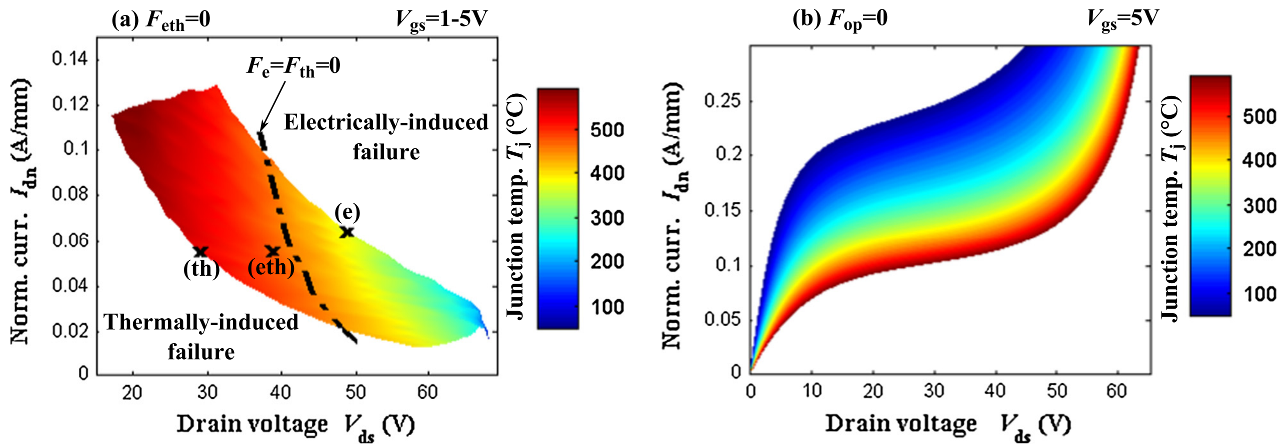

Fig. 4. (a) Color plot of the surface $F_{eth} = 0$ for different V_{gs} values. The black line corresponds to the bias points where $F_e = F_{th} = 0$ and allows separation of the regions of electrically and thermally induced failure. (b) The MOS operating function $F_{op} = 0$ for various junction temperatures defined for $V_{gs,max} = 5$ V and $V_{be} = 0$ V. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

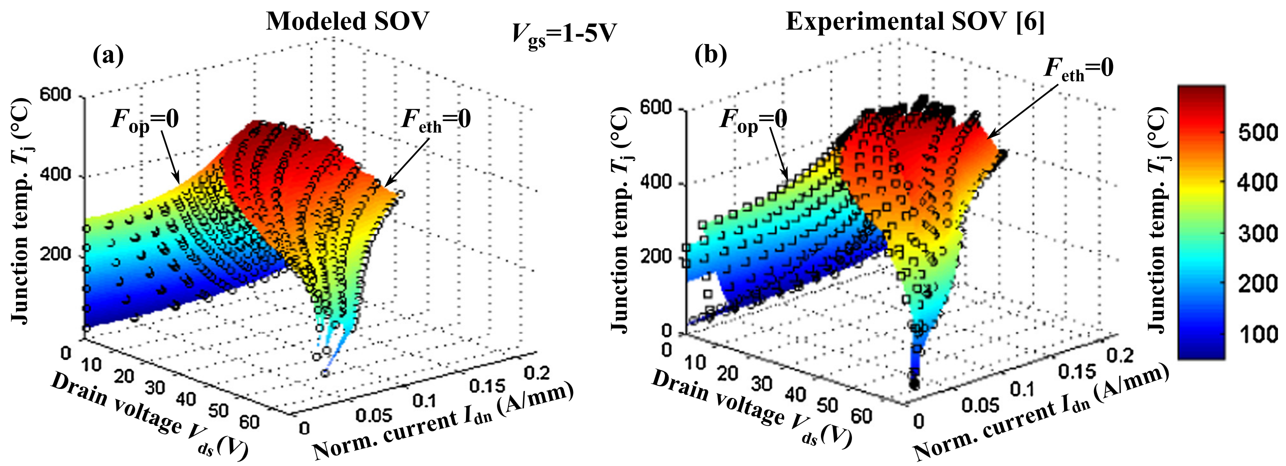

Fig. 5. Comparison between (a) modeled and (b) experimental [6] SOV, showing qualitative agreement across a wide range of bias conditions.

4.3. Mapping electro-thermal failure

In Fig. 4a, it is shown how electrical and thermal failure mechanisms are mapped on the failure function F_{eth}. The black dash-dotted line ($F_e = F_{th} = 0$) indicates the boundary between electrical and thermal failure regions, and the three crosses correspond to the failure points in Fig. 3a. In addition, the operating range is limited by the on-resistance and saturation current that are included using the operating function F_{op}:

$$F_{op} = \{(I_{dn}, V_{ds}, T_j) \in \mathbb{R}^3 : [I_{dn} - f_e(V_{gs,max}, V_{be} = 0)] = 0\}. \quad (32)$$

This is defined for $V_{gs} = V_{gs,max}, V_{be} = 0$ (so excluding the parasitic bipolar transistor) at different temperatures in absence of self-heating. In Fig. 4, the operating and failure functions F_{op} and F_{eth} are mapped onto a 3D space comprising gate-width normalized drain-current I_{dn}, drain voltage V_{ds} and junction temperature T_j. Intersecting the corresponding volumes V_{op} and V_{eth} yields a new frame work describing the operating limits of LDMOS transistors, which was defined as Safe Operating Volume (SOV) in earlier work [6]:

$$V_{SOV} = V_{eth} \cap V_{op}. \quad (33)$$

For comparison with measurement results, the total SOV has been constructed using the equation system (1) and compared with the experimental data from [6] in Fig. 5.

5. Discussion

The presented analysis is useful for the following reasons.

(1) It allows identification of the main failure mechanism (electrical, thermal, electro-thermal) of MOS transistors on a theoretical basis, which is important for device optimization.
(2) It shows that there is a gradual boundary between an electrical failure region at high drain voltage V_{ds} and a thermal failure region at high junction temperature T_j.
(3) It explains why the SOV can be used as a general frame work for the operating range of transistors, which is to a large extent independent of the size and operating conditions.
(4) It suggests that the failure functions can be combined with the model results in Fig. 5a to reduce the number of measurements needed to construct the experimental SOV in Fig. 5b.

6. Conclusions

An analytical procedure for identifying failure mechanisms in MOS transistors has been presented. The electrical, thermal and electro-thermal stability factors derived in this work can be used together with an electro-thermal characterization of the MOS and its parasitic bipolar to perform a failure analysis and determine the main root of instability. The results allow the operating limits to be mapped on the Safe Operating Volume (SOV), an analysis concept which is defined as an extension of the Safe Operating Area (SOA).

Appendix A

Avalanche, MOS and bipolar model equations used in this work. The model parameters have been fitted to experimental data [6].

$$\left\{ M = \frac{1}{1-\left(\frac{V_{ds}}{BV}\right)^m} \right. \quad (\mathbf{A1})$$

BV	70 V
m	4

$$\begin{cases} K(T_j) = K(T_{ref})\left(\frac{T_j}{T_{ref}}\right)^{-m_{ch}} & (\mathbf{M1}) \\ V_{th}(T_j) = V_{th}(T_{ref}) - k_{th}(T_j - T_{ref}) & (\mathbf{M2}) \\ R_{on}(T_j) = R_{on}(T_{ref}) \cdot \left(\frac{T_j}{T_{ref}}\right)^{m_{drift}} & (\mathbf{M3}) \\ I_{dsat}(T_j) = I_{dsat}(T_{ref}) \cdot \exp\left(-\frac{T_j - T_{ref}}{\theta}\right) & (\mathbf{M4}) \\ V_{dsat}(T_j) = R_{on}(T_j) \cdot I_{dsat}(T_j) & (\mathbf{M5}) \\ I_{ch} = \frac{K \cdot (V_{gs} - V_{th})^{\alpha_{ch}}}{1 + \theta_{V_{gs}}(V_{gs} - V_{th})} \cdot \frac{1}{\left[1 + \left(\frac{V_{ch}}{V_{gs} - V_{th}}\right)^{\eta_{ch}}\right]^{1/\eta_{ch}}} & (\mathbf{M6}) \\ I_{drift} = I_{dsat} \cdot \frac{(V_{ds} - V_{ch})}{V_{dsat}} \cdot \frac{1 + g_{ac}(V_{ds} - V_{ch})}{\left[1 + \left(\frac{V_{ds} - V_{ch}}{V_{dsat}}\right)^{\eta_{drift}}\right]^{1/\eta_{drift}}} & (\mathbf{M7}) \\ I_{dMOS}(V_{ds}) = I_{ch}(V_{ch}) = I_{drift}(V_{ds} - V_{ch}) & (\mathbf{M8}) \end{cases}$$

T_{ref}	300 K
$K(T_{ref})$	$0.032\ A/V^2$
m_{ch}	1.5
$V_{th}(T_{ref})$	0.82 V
k_{th}	$1.36 \cdot 10^{-3}$ V/K
$R_{on}(T_{ref})$	27 Ω
m_{drift}	1.5
θ	750 K
$I_{dsat}(T_{ref})$	0.127 A
α_{ch}	2
$\theta_{V_{gs}}$	$0.05\ V^{-1}$
η_{ch}	1.6
g_{ac}	$3 \cdot 10^{-3}\ V^{-1}$
η_{drift}	1.6

$$\begin{cases} I_s(T_j) = I_s(T_{ref}) \cdot \exp\left[-\frac{qE_g}{k}\left(\frac{1}{T_j} - \frac{1}{T_{ref}}\right)\right] & (\mathbf{B1}) \\ I_R(T_j) = I_R(T_{ref}) \cdot \exp\left[-\frac{qE_g}{2k}\left(\frac{1}{T_j} - \frac{1}{T_{ref}}\right)\right] & (\mathbf{B2}) \\ R_B(T_j) = R_B(T_{ref}) \cdot \left(\frac{T_j}{T_{ref}}\right)^{m_{npn}} & (\mathbf{B3}) \\ \beta(T_j) = \beta(T_{ref})\left(\frac{T_j}{T_{ref}}\right)^{m_\beta} & (\mathbf{B4}) \\ I_b(V_{be}, T_j) = \frac{I_S}{\beta}(T_j) \cdot \exp\left(\frac{V_{be}}{V_T}\right) & (\mathbf{B5}) \\ I_c(V_{be}, T_j) = I_S(T_j) \cdot \exp\left(\frac{V_{be}}{V_T}\right) + I_R(T_j) & (\mathbf{B6}) \end{cases}$$

$I_S(T_{ref})$	10^{-15} A
E_g	1.12 eV [12]
$I_R(T_{ref})$	10^{-12} A
$R_B(T_{ref})$	5 Ω
m_{npn}	1.5
$\beta(T_{ref})$	5
m_β	2

References

[1] Hower PL, Govil PK. Comparison of one- and two-dimensional models of transistor thermal instability. IEEE Trans Electron Dev 1974;21(10):617–23.
[2] Hower P, Tsai CY, Merchant S, Efland T, Pendharkar S, Steinhoff R, et al. Avalanche-induced thermal instability in LDMOS transistors. In: Proceedings of ISPSD; 2001. p. 153–6.
[3] Hower PL. Safe operating area – a new frontier in LDMOS design. In: Proceedings of ISPSD; 2002. p. 1–8.
[4] Khemka V, Parthasarathy V, Zhu R, Bose A. A novel technique to decouple electrical and thermal effects in SOA limitation of power LDMOSFET. Electron Dev Lett IEEE 2004;25(10):705–7.
[5] Dibra D, Stecher M, Decker S, Lindemann A, Lutz J, Kadow C. On the origin of thermal runaway in a trench power MOSFET. IEEE Trans Electron Dev 2011;58(10):3477–84.
[6] Ferrara A, Steeneken PG, Heringa A, Boksteen BK, Swanenberg M, Scholten AJ, et al. The safe operating volume as a general measure for the operating limits of LDMOS transistors. In: Proceedings of IEDM; 2013. p. 6.7.1–4.
[7] Radhakrishna U, DasGupta A, DasGupta N, Chakravorty A. Modeling of SOI-LDMOS transistor including impact ionization, snapback, and self-heating. IEEE Trans Electron Dev 2011;58(11):4035–41.
[8] Pfost M, Boianceanu C, Lohmeyer H, Stecher M. Electrothermal simulation of self-heating in DMOS transistors up to thermal runaway. IEEE Trans Electron Dev 2013;60(2):699–707.
[9] Chung YS, Baird B. Power capability limits of power MOSFET devices. Microelectron Reliab 2002;42:211–8.
[10] Ferrara A, Steeneken PG, Boksteen BK, Heringa A, Scholten AJ, Schmitz J, et al. Identifying failure mechanisms in LDMOS transistors by analytical stability analysis. In: Proceedings of ESSDERC; 2014. p. 321–4.
[11] Baliga BJ. Fundamentals of power semiconductor devices. Springer; 2008.
[12] Sze SM. Physics of semiconductor devices. Wiley-Interscience; 1969.
[13] Sque SJ, Scholten AJ, Aarts ACT, Klaassen DBM. Threshold behavior of the drift region: the missing piece in LDMOS modeling. In: Proceedings of IEDM; 2013. p. 12.7.1–4.
[14] Klaassen DBM. A unified mobility model for device simulation – I. Model equations and concentration dependence. Solid-State Electron 1992;35(7):953–9.
[15] Arora N. Mosfet modeling for VLSI simulation: theory and practice. World Scientific; 2007.
[16] Ferrara A, Steeneken PG, Reimann K, Heringa A, Yan L, Boksteen BK, et al. Comparison of electrical techniques for temperature evaluation in power MOS transistors. In: Proceedings of ICMTS; 2013. p. 115–20.
[17] Breglio G, Frisina F, Magri A, Spirito P. Electro-thermal instability in low voltage power MOS: experimental characterization. In: Proceedings of ISPSD; 1999. p. 233–6.
[18] Reggiani S, Gnani E, Rudan M, Baccarani G, Corvasce C, Barlini D, et al. Measurement and modeling of the electron impact-ionization coefficient in silicon up to very high temperatures. IEEE Trans Electron Dev 2005;52(10):2290–9.
[19] Vanhoucke T, Hurkx GAM. Unified electro-thermal stability criterion for bipolar transistors. In: Proceedings of BCTM; 2005. p. 37–40.
[20] Reggiani S, Baccarani G, Gnani E, Gnudi A, Denison M, Pendharkar S, et al. Explanation of the rugged LDMOS behavior by means of numerical analysis. IEEE Trans Electron Dev 2009;56(11):2811–8.
[21] Moens P, Van den Bosch G. Characterization of total safe operating area of lateral DMOS transistors. IEEE Trans Dev Mater Reliab 2006;6(3):349–57.
[22] van Overstraten R, de Man H. Measurement of ionization rates in diffused silicon p-n junctions. Solid-State Electron 1970;13(5):583–608.