



Strain characterization of FinFETs using Raman spectroscopy

B. Kaleli ^{a,*}, T. van Hemert ^a, R.J.E. Huetting ^a, R.A.M. Wolters ^{a,b}

^a MESA + Institute for Nanotechnology, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands

^b NXP Research Eindhoven, High Tech Campus 4, 5656 AE Eindhoven, The Netherlands

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ABSTRACT

Metal induced strain in the channel region of silicon (Si) fin-field effect transistor (FinFET) devices has been characterized using Raman spectroscopy. The strain originates from the difference in thermal expansion coefficient of Si and titanium-nitride. The Raman map of the device region is used to determine strain in the channel after preparing the device with the focused ion beam milling. Using the Raman peak shift relative to that of relaxed Si, compressive strain values up to -0.88% have been obtained for a 5 nm wide silicon fin. The strain is found to increase with reducing fin width though it scales less than previously reported results from holographic interferometry. In addition, finite-element method (FEM) simulations have been utilized to analyze the amount of strain generated after thermal processing. It is shown that obtained FEM simulated strain values are in good agreement with the calculated strain values obtained from Raman spectroscopy.

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1. Introduction

Because of the so-called short-channel effects caused by scaling down conventional field effect transistors (FETs) in complementary metal–oxide–semiconductor technology, multiple gate structures are realized to be a good replacement of those devices [1]. The most important advantage of multigate devices is their better electrostatic control of the channel region which helps to reduce the off-current (I_{off}).

The FinFET as shown in Fig. 1, is in fact such a multiple gate device comprising a narrow Si fin with a self-aligned double gate [2]. Its multigate structure allows realization of smaller devices with improved key properties such as a high on-current/off-current ratio ($I_{\text{on}}/I_{\text{off}}$). Therefore, this is currently one of the most promising structure to achieve better performance. However, the FinFET still needs to reach yet a higher I_{on} to meet the technology requirement. Employing strain to the FinFET channel region is attracting a high interest to achieve this goal [3–5]. The characterization of the generated strain in this relatively small volume of silicon is essential to understand its effects and to keep it under control.

In this work, strain induced by the TiN gate on Si FinFET devices has been physically characterized. The actual strain originates from the thermal expansion coefficient differences between the TiN and the Si channel. This can be illustrated by the simulation example performed using a multiphysics Finite-element-method (FEM) tool (Comsol MultiPhysics 3.5a). In the simulations, we neglected the Si substrate to decrease the computational load and applied fixed boundary conditions below the buried oxide (BOX) layer to mimic the stiff Si

substrate. We simplified our 5-fin device structure by simulating a single fin device. Symmetric boundary conditions were applied to the sides of the fins as well as at the source and drain regions. The rest of the boundaries were kept free to move. Fig. 2(b)–(d) show the simulated vertical strain (ϵ_{zz}) in AA' cross section of a 5 nm wide fin at 900 °C, 500 °C and 25 °C, respectively, after the device structure has been formed. The other strain components, ϵ_{xx} and ϵ_{yy} are much smaller than ϵ_{zz} (up to 20%) and are therefore neglected in this work. A high temperature cycle has been implemented on the built device structure to create strain as would be present in the real case. During the thermal cycle of the stacked structure, strain increases while the temperature increases. At elevated temperatures plastic relaxation occurs and strain becomes zero. Our simulations are referenced to this relaxed state. When the system is cooling down, strain increases again and remains permanently in the Si body or fin. Compressive strain in the range of 0.9% has been observed for a 5 nm fin width (W_{FIN}). The simulation for the 30 nm wide fin at 25 °C is also depicted (Fig. 2(a)) to show that generated strain decreases when W_{FIN} increases and also becomes less uniform in the silicon body. In Fig. 3 the FEM simulated strain values are plotted against W_{FIN} .

In an earlier report the so-called holographic interferometry method was used to physically characterize the strain for two W_{FIN} values [4,6]. This motivated us to perform physical strain characterization of the silicon FinFETs employing an alternative methodology called the Raman spectroscopy. Raman spectroscopy is a non-contact and non-destructive technique that is most widely employed for this purpose [7–10]. It yields valuable information about strain even in aggressively scaled device configurations [11,12].

The paper is outlined as follows. In Section 2 the experimental details will be briefly described. In Section 3 the obtained results will be described and discussed. Finally in Section 4 the conclusions will be drawn.

* Corresponding author. Tel.: +31 534892645.

E-mail address: b.kaleli@utwente.nl (B. Kaleli).

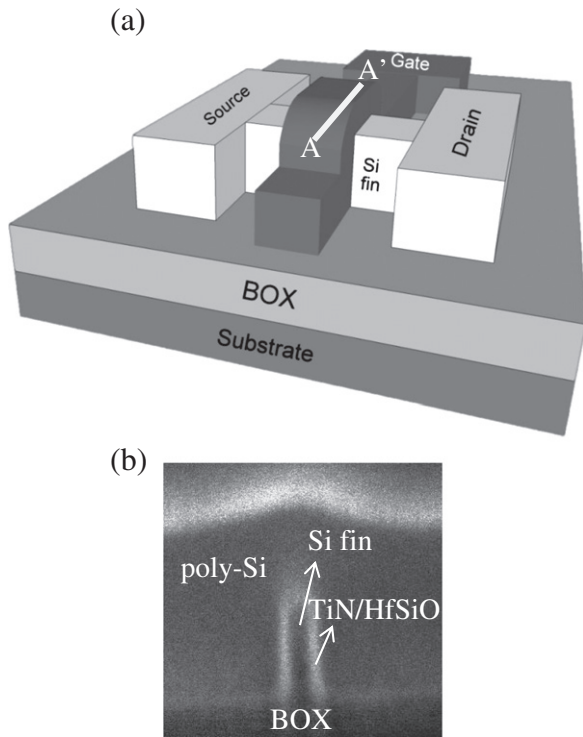


Fig. 1. Schematic FinFET layout: (a) bird's eye view (b) cross-section taken from line AA'.

2. Experimental details

The FinFET devices used in this work were realized at NXP-Research/IMEC [13]. Fig. 1(b) shows the scanning electron microscope (SEM) cross section of a FinFET on a silicon-on insulator (SOI) substrate. The gate stack consists of $\text{SiO}_2 + \text{HfSiO}$ as the gate dielectric layer and TiN as the gate metal with poly-Si capping. A thermal cycle from room temperature to 1340 °C and back to room temperature was

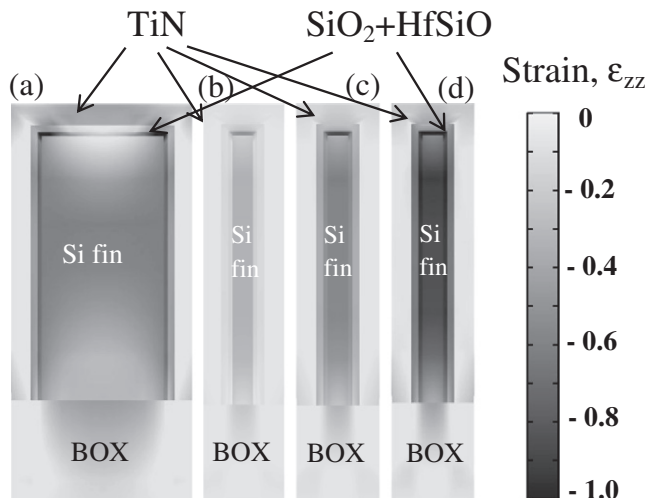


Fig. 2. ϵ_{zz} strain values of the 30 nm and 5 nm wide FinFETs at different temperatures during the temperature cycle obtained with multiphysics FEM simulations at (a) 25 °C after a thermal cycle from $T = 25$ °C to 1100 °C for $W_{\text{FIN}} = 30$ nm, (b) 900 °C, (c) 500 °C and (d) 25 °C for $W_{\text{FIN}} = 5$ nm. The vertical bar indicates the strain values varying from 0 to -1.0 (compressive) strain. The thickness of the TiN film is 5 nm and the height of Si fin is 60 nm.

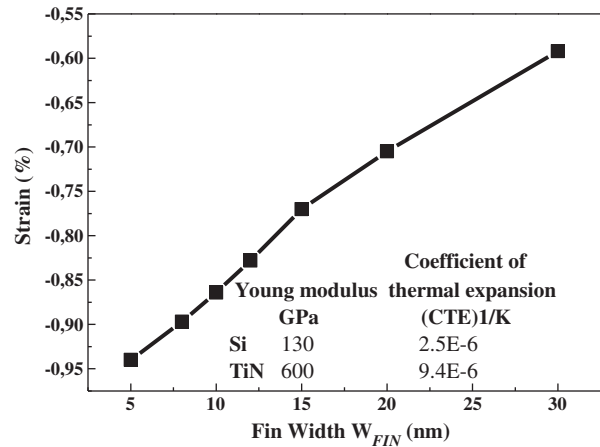


Fig. 3. Calculated maximum strain (ϵ_{zz}) against the fin width obtained with FEM simulations. Inset shows the physical parameters used in the simulations.

implemented after gate deposition which resulted in permanent strain on the channel. All of the devices characterized in this work comprised 5 fins with various fin widths ($5 \text{ nm} \leq W_{\text{FIN}} \leq 1000 \text{ nm}$), 10 μm gate length and 60 nm fin height (H_{FIN}) or SOI thickness. For more processing details refer to [13].

The measurements have been carried out at room temperature using confocal Raman microscope (alpha300R, Witech GmbH) with 0.8 cm^{-1} wavenumber resolution (which corresponds to about 0.15% strain resolution) and a 532 nm laser source with output power of 47 mW. This wavelength will give a penetration depth in the silicon of 800–1000 nm. This high penetration depth leads to a weak Raman signal from the FinFET with respect to the strong signal from the surrounding relaxed silicon. However, despite this penetration depth, this tool has been utilized successfully for device analysis [12]. The FinFET devices had metallic tiles on top of the device structure in the back-end. Since the metal layers were very thick and Raman inactive, they were removed using Focused Ion Beam (FIB) milling. Removal of these layers was necessary to obtain a good Raman signal from the area of interest.

3. Results and discussion

Fig. 4 shows the HR-SEM picture of the device before and after FIB removal of the metal layers in the back-end. To prevent the damage to the stressor TiN layer, FIB process parameters were optimized at a 47 pA beam current and a 5 minute process time. A cross section SEM image after FIB processing confirms that the stressor layer is still present. Raman spectroscopy on these samples was done by scanning the complete area of the channel region.

Fig. 5 shows the peak map of the scanned device region before and after the FIB process. To identify the Si channel from this map, the Raman peak at 520 cm^{-1} is highlighted. The contrast in this figure indicates different peaks of the Raman spectrum obtained from the channel. The Raman peak of the Si channel region was only detectable after the FIB process. This map helps us to identify the Si fin region from the rest of the substrate and it was used for extracting the Raman spectrum of the strained channel region.

Fig. 6(a) shows the Raman spectrum of the Si substrate. Since the Si layer is only 60 nm thick and the penetration depth of the laser is larger than the sum of the Si fin and BOX layer thickness, the substrate peak as well as the thin un-doped Si peak is present in the Raman spectrum. Since both Raman peaks are from Si they appear almost at the same wavenumber without stress (i.e. 520 cm^{-1}). The peaks are broadened because of the signal from the poly-Si layer on top of the fins [14].

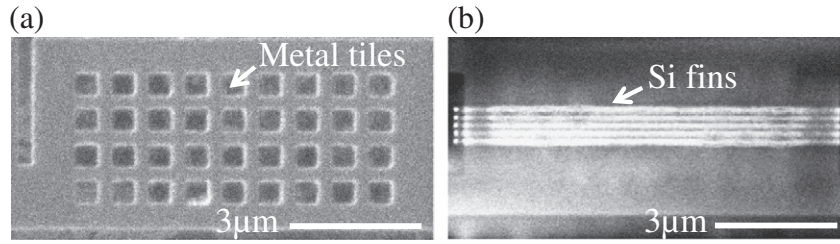


Fig. 4. HR-SEM image of the device before (a) and after (b) FIB removal of the metal layers.

Raman analysis has been performed for devices having 10 μm gate length and different fin widths. The samples have been analyzed by fitting the obtained Raman peaks with Lorentzian function. Except for the device with $W_{\text{FIN}} = 1000$ nm (Fig. 6(b)), Fig. 6(c)–(f) shows a second peak next to the substrate peak in the spectrum. The second peak is the Si fin peak which normally cannot be differentiated from the substrate peak. It can be seen from Fig. 6 that the Si fin peak shifts to higher wavenumbers when the fin width is decreasing from 30 nm to 5 nm. The shift to higher wavenumbers is an indication of compressive stress [15]. Since the stress is much lower for the 1000 nm wide fin device, the second, stressed, Si peak cannot be observed.

Strain values were calculated from the amount of Raman peak shift using the 1000 nm wide fin peak in Fig. 6(b) as a reference. The calculations are dependent on the stress calibration using Raman shift data and the fitting of the peaks. In this way the strain level and its evolution by fin width is provided. Fig. 7 shows the extracted strain values using the Raman shift data together with the

strain values obtained by N. Serra et al. [6]. The authors used the holographic interferometry method on the same set of devices to obtain strain information. The strain was calculated using the Raman shift according to the following relations [14]:

$$\sigma = -250 \text{ (MPa/cm)} \Delta\omega \quad (1)$$

$$\varepsilon = \frac{\sigma}{E} \quad (2)$$

where E = Young's modulus, σ = Stress, ε = Strain, $\Delta\omega$ = Peak shift.

For the strain calculations the Young's modulus of silicon along the Z axis is taken as $E_z = 130$ GPa [16]. Table 1 shows the peak positions and calculated strain values for each device. The strain value obtained for $W_{\text{FIN}} = 10$ nm with the Raman spectroscopy method is comparable to Serra's results while for $W_{\text{FIN}} = 20$ nm we find a larger strain value. The strain dependency on the fin width is clearly observed in both sets of data. The identical strain dependency on the fin width

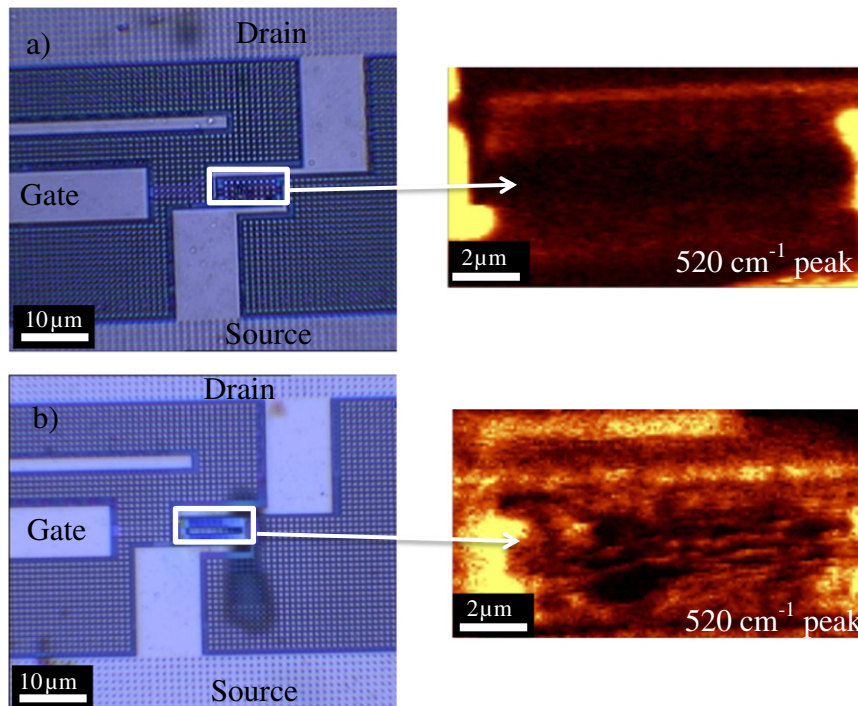


Fig. 5. Raman peak map of the channel region (a) before FIB, (b) after FIB preparation. The images on the right side shows the peak position map of the Raman spectrum. The 520 cm^{-1} peak is highlighted with light colors to identify the Si channel region from the BOX.

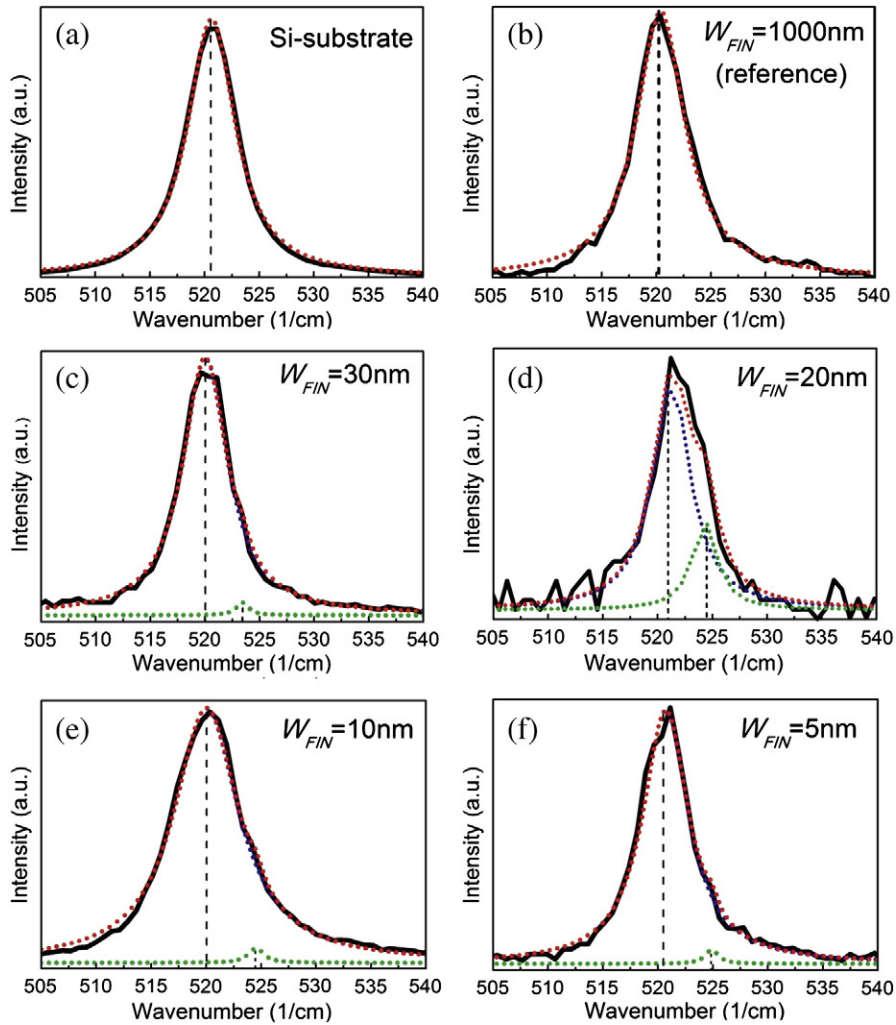


Fig. 6. Obtained Raman spectra of (a) the substrate, and that of the FinFET with a fin width of (b) 1000 nm, used as a reference, (c) 30 nm, (d) 20 nm, (e) 10 nm, (f) 5 nm. The blue dotted curves are the obtained Lorentzian fits corresponding to Si substrate. The green dotted curves are after fitting the second peak due to increased strain. The total fits are indicated by red dotted curves.

has also been reported earlier by employing electrical measurements on the FinFET devices used in this work [17]. Finally, Fig. 7 shows that

the strain values obtained from FEM simulations agree well with the Raman spectroscopy data for a wide range of fin widths.

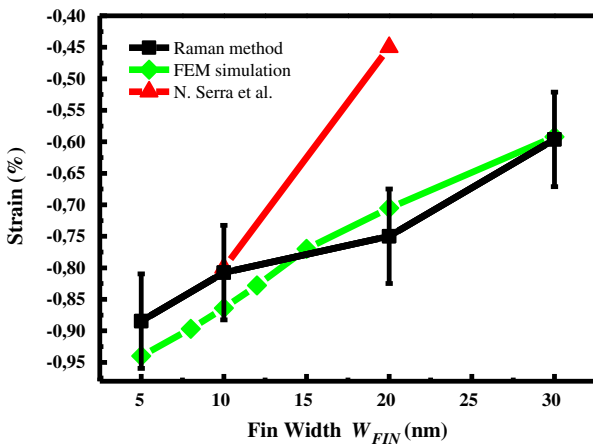


Fig. 7. Extracted strain values in silicon FinFETs using Raman spectroscopy. For comparison FEM simulation (see Fig. 3) and experimental data obtained from the holographic interferometry method [6] have been plotted in the same graph. Note that due to the limitation of the Raman microscope system, the strain resolution is about 0.15% for the Raman method.

4. Conclusions

Metal induced strain on the channel of silicon FinFET devices has been characterized using Raman spectroscopy and the results have been compared to FEM simulation data. Raman peaks from Si fins shift to higher wavenumbers for narrow fins indicating compressive strain. Up to -0.88% strain has been calculated from our Raman spectroscopy data. The FEM simulated strain values after a thermal cycle are in a good agreement with the measurements. In addition, the metal induced strain on Si fins was found to increase with reducing the fin width. However, the dependence is less than previously reported using holographic interferometry method.

Table 1
Strain values obtained from a Lorentzian peak fit.

Fin width (nm)	Peak position (cm^{-1})	Strain (%)
1000	520.3	Reference
30	523.4	-0.60
20	524.2	-0.75
10	524.5	-0.80
5	524.9	-0.88

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References

- [1] Intel's Revolutionary 22 nm Transistor Technology, <http://www.intel.com>.
- [2] D. Hisamoto, W.C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.J. King, J. Bokor, C. Hu, IEEE Trans. Electron Devices 47 (2000) 2320.
- [3] J. Song, B. Yu, W. Xiong, Y. Taur, IEEE Trans. Electron Devices 56 (2009) 533.
- [4] N. Serra, D. Esseni, IEEE Trans. Electron Devices 57 (2010) 482.
- [5] K. Maitra, A. Khakifirooz, P. Kulkarni, V.S. Basker, J. Faltermeier, H. Jagannathan, H. Adhikari, C.-Chen Yeh, N.R. Klymko, K. Saenger, T. Standaert, R.J. Miller, B. Doris, V.K. Paruchuri, D. McHerron, J. O'Neil, E. Leobundung, H. Bu, IEEE Electron Device Lett. 32 (2011) 713.
- [6] N. Serra, F. Conzatti, D. Esseni, M. De Michielis, P. Palestri, L. Selmi, S. Thomas, T.E. Whall, E.H.C. Parker, D.R. Leadley, L. Witters, A. Hikavy, M.J. Hytch, F. Houdellier, E. Snoeck, T.J. Wang, W.C. Lee, G. Vellianitis, M.J.H. van Dal, B. Duriez, G. Doornbos, R.J.P. Lander, International Electron Devices Meeting (IEDM), 2009, p. 1.
- [7] E. Anastassakis, A. Pinczuk, E. Burstein, F.H. Pollak, M. Cardona, Solid State Commun. 8 (1970) 133.
- [8] I. de Wolf, Semicond. Sci. Technol. 11 (1996) 139.
- [9] A. Ogura, D. Kosemura, M. Takei, H. Uchida, N. Hattori, M. Yoshimaru, S. Mayuzumi, H. Wakabayashi, Mater. Sci. Eng., B 159 (2009) 206.
- [10] S. Nishibe, T. Sasaki, H. Harima, K. Kisoda, T. Yamazaki, W.S. Yoo, 14th IEEE International Conference on Advanced Thermal Processing of Semiconductors, 2006, p. 211.
- [11] W. Xiong, C.R. Cleavelin, P. Kohli, C. Huffman, T. Schulz, K. Schrufer, G. Gebara, K. Mathews, P. Patruno, Y.M. Le Vaillant, I. Cayrefourcq, M. Kennard, C. Mazure, K. Shin, T.J.K. Liu, IEEE Electron Device Lett. 27 (2006) 612.
- [12] K.E. Moselund, P. Dobrosz, S. Olsen, V. Pott, L. De Michielis, D. Tsamadoa, D. Bouvet, A. O'Neill, A.M. Ionescu, Techn. Digest. International Electron Devices Meeting (IEDM), 2007, p. 191.
- [13] M. van Dal, N. Collaert, G. Doornbos, G. Vellianitis, G. Curatola, B. Pawlak, R. Duffy, C. Jonville, B. Degroote, E. Altamirano, E. Kunnen, M. Demand, S. Beckx, T. Vandeweyer, C. Delvaux, F. Leys, A. Hikavy, R. Rooyackers, M. Kaiser, R. Weemaes, S. Biesemans, M. Jurczak, K. Anil, L. Witters, R. Lander, VLSI Technology 2007 IEEE Symposium, Jun. 2007, p. 110.
- [14] V. Paillard, P. Puech, M.A. Laguna, P. Temple-Boyer, B. Causat, Appl. Phys. Lett. 73 (1998) 1718.
- [15] W.S. Yoo, T. Ueda, K. Kang, International Workshop on Junction Technology, 2009, p. 78.
- [16] Matthew A. Hopcroft, William D. Nix, Thomas W. Kenny, J. Microelectromech. Syst. 19 (2010) 229.
- [17] T. van Hemert, B. Kaleli, Kemaneci, R.J.E. Huetting, D. Esseni, M.J.H. van Dal, J. Schmitz, Proceedings of the European Solid-State Device Research Conference (ESSDERC), 2011, p. 275.