Plasma Charging Damage Reduction in IC Processing by A Self-balancing Interconnect

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Abstract

In this paper, a novel first order self-balancing interconnect layout design is proposed for reducing plasma-process induced charging damage (P2ID) in modern CMOS processes. According to the mechanism of P2ID, dense interconnect lines collect positive charges due to electron shading (ES) effect [1] while sparse interconnect lines collect negative charges due to extended electron shading effect (EES) [2]. If the layout of the interconnect lines is such that the spacing between the interconnect lines is alternately wide and narrow both negative and positive charges are collected. Because these charges balance each other, the P2ID is reduced.

1. Introduction

Plasma technology is key for enabling the ultra-large-scale-integration (ULSI) manufacturing of integrated circuits (ICs). The number of plasma processing steps increases with each generation of technology. However, plasma is also a very harsh environment. Both electrons and positive ions from the plasma are impinging on the exposed conductor of interconnects during processing. Because of the nonuniformity of the plasma or/and the shading effect caused by the local microscopic topography, the electron flux and the ion flux might not balance each other. The net positive or negative charges collected by the interconnect lines are channeled to the gate, where they are neutralized by the current tunneling across the gate oxide. However, traps are generated when the current tunnels across the gate oxide resulting in reliability loss or even in failure of the devices.

Interconnect layout has a considerable effect on this charging damage induced by plasma-process, since it affects the current-density stress levels experienced by dielectric layers. In this paper, a novel first order self-balancing interconnect layout design is proposed to reduce plasma-process induced charging damage (P2ID) in design phase. It was reported that dense interconnect lines collect positive charges due to the electron shading (ES) effect [1] but sparse interconnect lines collect negative charges due to the extended electron shading effect (EES) [2]. Using a first order self-balancing interconnect layout design, the P2ID is reduced because the extra charges neutralize each other. The experiment compares the P2ID of a dense line antenna, a sparse line antenna, and dense/sparse interlaced antenna structure. A special triple gate-antenna ("TriMos") frame is designed.

2. Experimental

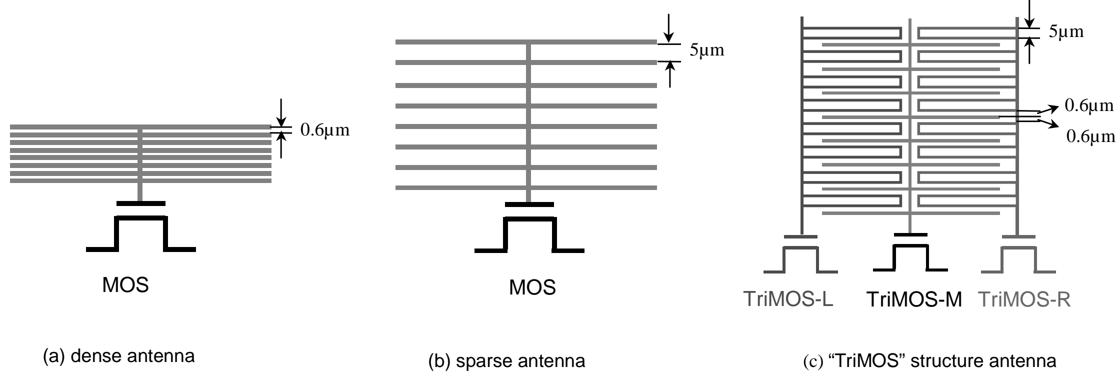


Fig.1: Schematic view of different antenna structures: (a) dense-line finger-shaped antenna structure with interspacing of 0.6μm, (b) sparse-line finger-shaped antenna structure with interspacing of 5μm and (c) "TriMOS" structure antenna (the antennas connected to a different MOS are all in the same level).

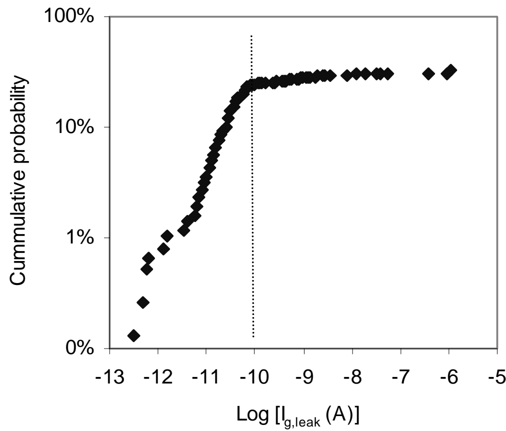


Fig.2: Distribution of gate leakage current.

The test structures have been subjected to an experimental 0.35 μm CMOS backend-of-line process. The test structures consist of small transistor with W x L = 2 μm x 0.35 μm. The gate oxide thickness is 7.5 nm. The interconnect metal lines are patterned with a medium density plasma system.

To simulate the interconnect lines, a finger-shaped conductor is designed and connected to the gate of the MOS transistor. The conductor collects the ions and electrons from the plasma during the processing and is therefore called antenna. The antenna ratio is defined as the area ratio of the antenna to the gate oxide. The induced gate tunnelling current density is proportional to the antenna ratio.

In this study, two types of conventional finger-shaped antennas —dense-line antenna and sparse-line antenna were designed and used, as shown in Fig. 1(a) and Fig. 1(b). They are dense-line finger-shaped antenna structure with interspacing of 0.6 μm and sparse-line finger-shaped antenna structure with interspacing of 5 μm, respectively. The antenna ratios of these charging testers are 10K and 100K.

Furthermore, a special structure combining 3 antennas with 3 transistors is designed as a special case study. The schematic view is shown in Fig. 1(c). Since they have 3 antennas and 3 transistors, they were called "TriMOS" structures. One transistor is in the middle (TriMOS-M), one is on the left (TriMOS-L), and another is on the right (TriMOS-R). The antenna ratio for each TriMOS is 100K.

To detect plasma damage, the gate leakage current ($I_{g,leak}$) is measured by applying a gate voltage of V_g = 3.74V. A charging tester is considered to fail when the $I_{g,leak}$ measured through its gate oxide exceeds 0.1nA, indicating that (soft or hard) breakdown occurred. The 0.1nA is selected as failure criterion based on the leak current distribution, as shown in Fig. 2. The devices with $I_{g,leak}$ higher than 0.1nA, diverge from the intrinsic slope, indicating extrinsic damage induced by plasma charging.

3. Results

Table 1: Failure fraction of TriMOS structures and conventional MOS charging structures that have only one finger antenna with same AR=100k as each MOS of the TriMOS

	New TriMOS structures			Conventional finger antenna structures	
	TriMOS-L	TriMOS-M	TriMOS-R	0.6μm spacing	5μm spacing
Lot A	6.7	1.7	7.5	12.5	69.2
Lot B	1.9	0.5	1.4	5.7	53.8
Lot C	26.7	22.1	25.9	55.7	77.6

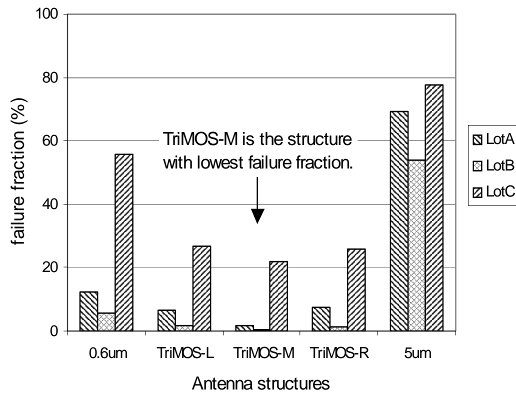


Fig. 3: Comparison of the failure fraction for different antenna structures.

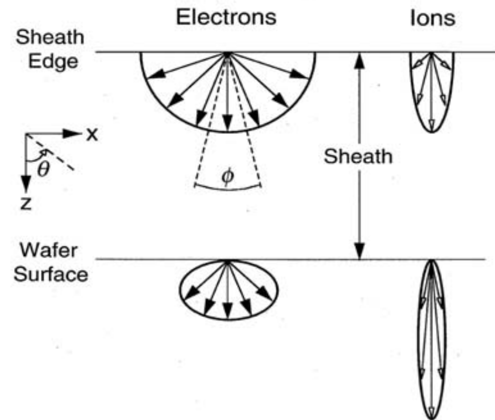


Fig. 4: Schematic depiction of the electron and ion angular distribution functions at the sheath edge and at the wafer surface.

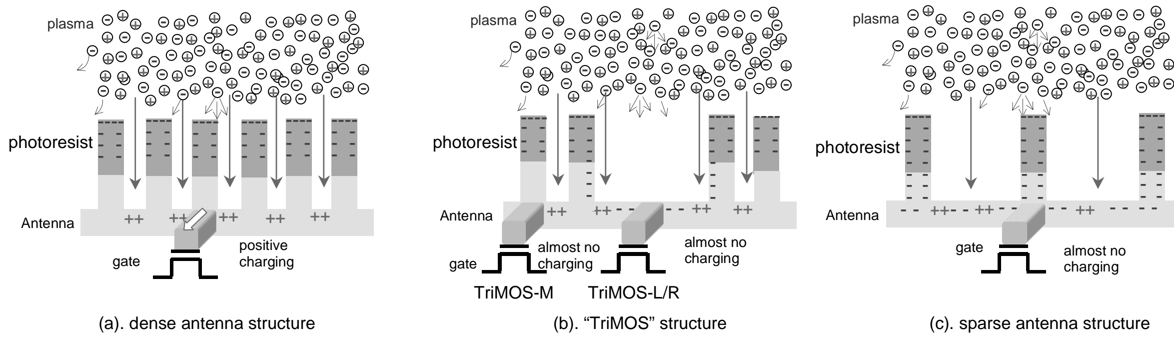
In Table 1 and Fig. 3, the failure fraction of our new TriMOS structures with two conventional MOS charging structures with a single 0.6μm or 5μm spacing finger antenna are compared. All test structures have the same 100K antenna ratio. The conventional MOS charging structures both with 0.6μm or 5μm finger spacing, failed more than any of the TriMOS structures. For the 3 different lots, the middle antenna (TriMOS-M) fails less than both the left antenna (TriMOS-L) and right antenna (TriMOS-R). The conventional MOS structures with a 5μm finger spacing antenna failed more than those with a 0.6μm finger spacing antenna.

4. Discussion of the Mechanism

The electrons and ions have significant difference in incident angular distributions [3]. Electrons are decelerated while ions get accelerated in the thin positively charged sheath, resulting in broad electron and narrow ion angular distributions. This difference implies that most of the ions impinge onto a wafer surface perpendicularly while most of the electrons arrive with oblique incident angles. A representative distribution is illustrated in polar format in Fig.4 [4].

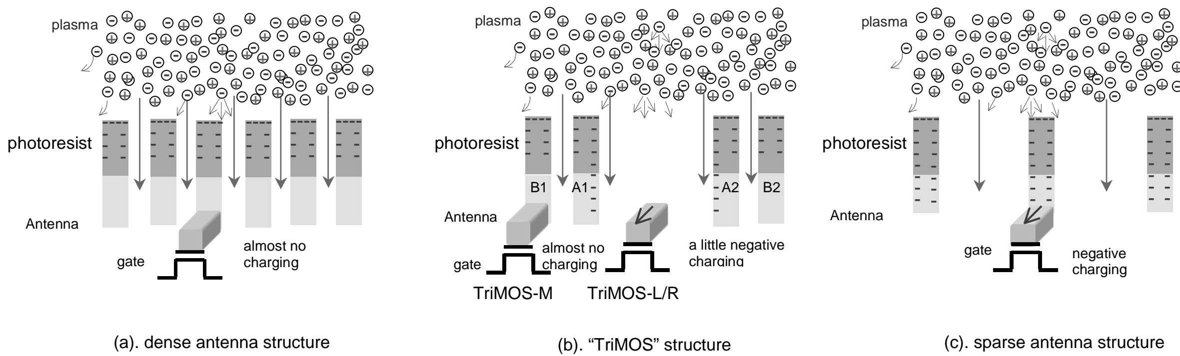
As a result of geometric and electrical shading, ions are so directional that none will hit the sidewalls on their way to the bottom. Electrons are so isotropic that most will hit the sidewalls and will stick there.

The imbalance between ions and electrons determines the amount of plasma-induced damage. How well they balance is related to the pattern of the antenna fingers (dense or sparse) and the phase of etching (during etching or over etching). The schematic view of the structures during etching and during over etching are illustrated in Fig. 5 and Fig. 6 respectively.



(a). dense antenna structure (b). "TriMOS" structure (c). sparse antenna structure

Fig. 5: Schematic view of the structures during etching



(a). dense antenna structure (b). "TriMOS" structure (c). sparse antenna structure

Fig. 6: Schematic view of the structures during over etching

4.1. Dense antenna structure

During etching, the photoresist was negatively charged. The electrons are repelled by the photoresist. The electrons moving in all directions can hardly enter into that narrow trench. However, it is relatively easy for the ions to reach the bottom. Hence the dense antenna collects positive charges during etching, as shown in Fig. 5(a).

During over-etching the antenna does not collect positive charges anymore since all conductive antenna material between the two fingers has disappeared. Only the sidewall of the antenna is exposed to plasma. Because the fingers are so close to each other, only few electrons reach the sidewall of the antenna. Hence, the dense antenna collects no charges during over-etching, as shown in Fig. 6(a). The gate collects positive charges during etching and no charges during over-etching.

4.2 Sparse antenna structure

During etching, because the fingers are far away from each other, the electrons can reach the sidewall and the bottom of the trench. The vertically directed ions only reach the bottom of the trench. Hence the sparse antenna collects more negative charges than positive charges, as shown in Fig. 5(c).

During over-etching, since the conductive antenna material between the two fingers has gone, the antenna does not collect positive charges anymore. Only the sidewall of the antenna is exposed to plasma and catches electrons. Hence, during over etching, the sparse antenna collects only negative charges as shown in Fig. 6(c). The gate collects negative charges both during etching and during over-etching

4.3 The antenna of "TriMOS" structure

During etching, some sparse fingers collected negative charges and some dense fingers collect positive. The antenna of the TriMOS-M and TriMOS-L/R are still connected by the bottom thin metal layer. The collected ions and electrons may partly balance each other. Hence, the TriMOS-M and TriMOS-L/R are almost not charged, as shown in Fig. 5(b).

During over-etching, the bottom layer is clear. The antenna of TriMOS-M and the antenna of TriMOS-L/R have been separated. The fingers of TriMOS-M are in the same situation as the "standard alone" dense finger structure mentioned above. It does not collect charges. Since the antenna of the TriMOS-M collects very little charge both during etching and during over-etching, the TriMOS-M suffers the smallest amount of plasma damage.

One side of the fingers of the TriMOS-L/R is in the same situation as dense finger structure and the other side is collects almost no charges during etching and no charges for TriMOS-M but a little negative charges for the TriMOS-L/R during over-etching in the same situation as sparse finger structure. On one side the finger has narrow spacing, on the other side there is wide spacing. One side collects no charges and the other side collects a few negative charges, as shown in Fig. 6(b).

However note that only one side of the antenna of left/right MOS collects negative charges, while both sides of the sparse antenna of the sparse antenna structures collect negative charges. The sparse antenna structures suffer more plasma damage than left/right MOS not only during the etching but also during the over-etching. This fact explains why the TriMOS-L/R fails less than the "standard alone" sparse antenna structures mentioned above. Hence, the TriMOS-L/R is negatively charged.

5. Conclusions

The results indicate how to reduce plasma damage in design phase. By adding dummy lines to the layout or laying out the interconnect lines like this way: one side of the line has narrow spacing but the other side of the line has wide spacing as the antenna in "TriMOS", the plasma-induced damage will be reduced.

References

[1] K. Hashimoto, "Charge damage caused by electron shading effect", Jpn. J. Appl. Phys., vol. 33, pp. 6013-6018, 1994.

[2] A. Hasegawa, F. Shimpuku, M. Aoyama, K. Hashimoto and M. Nakamura, "Direction of topography dependent damage current during plasma etching", Proc. 3rd P2ID, p.168, 1998.

[3] G. S. Hwang and K. P. Giapis, "On the origin of the notching effect during etching in uniform high density Plasmas", *J. Vac. Sci. Technol. B* 15(1), pp. 70, 1997.

[4] K. P. Giapis and G. S. Hwang, "Pattern-Dependent Charging and the Role of Electron Tunneling," Jap. J. Appl. Phys. , vol. 37, pp. 2281, 1998.