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Progressive degradation in a-Si:H/SiN thin film transistors

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Abstract

In this paper we present the study of gate-stress induced degradation in a-Si:H/SiN TFTs. The drain current transient during gate bias stress (forward or reverse bias) and subsequent relaxation cannot be fitted with the models existent in the literature but it shows to be described by a progressive degradation model (PDM). According to PDM the degradation of the electrical response is a combined effect of a fast interface traps generation and a slow charge trapping at the created defect sites and existing bulk defects in a-SiN:H transitional region.
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Keywords: Degradation; Charge trapping; Interface states; Modelling

1. Introduction

Majority of the work regarding degradation of electrical performances of a-Si TFTs when subjecting to light soaking or bias stress, focuses on the degradation of the threshold voltage. Among all mechanisms responsible for the threshold voltage shift, charge trapping in gate insulator and defect creation in semiconductor is the most important for TFT applications [1,2]. Some models in the literature account for one of these two mechanisms and in this paper we refer to the defect-pool model (defect creation in a-Si:H) [3] and dispersive charge injection (charge trapping in a-SiN:H transitional region) model [4].

There have been efforts to clarify which mechanism is dominant for a-Si:H TFTs instability and there were proves, for example, in the annealing behavior of stresses TFTs, that both charge trapping and defect creation contribute to the induced shift of electrical characteristics. Moreover, different authors show that the shift of electrical characteristics does occur in structures like polySi/thermal SiO_2/c-Si where no H is present [5] or in Cr/SiN/c-Si where the semiconductor is not amorphous material [6]. The stretched exponential time dependence of the threshold voltage shift is found in the relaxation of any disordered systems, for example, in chalcogenide glasses. In relation with a-Si TFTs instability this equation was interpreted in different ways. In the view of defect pool model, it had been rewritten in the form of a stretched-hyperbola [7] and explained by the dispersive hydrogen diffusion [8] and in the view of charge trapping model it had been explained by trapped charge in the insulator [9]. The dispersive charge injection model does not start from the stretched exponential equation but from Shlesinger-Montroll theory of continuous-random-walk and it interprets the threshold voltage shift as due to the charge injection from the semiconductor accumulation layer into the insulator [10].

In one of our previous publication [11], we proposed a novel approach to study the degradation in a-Si:H/SiN TFTs. In this paper, we present a complete study on the drain current degradation at different voltage stress and temperatures and we show that the current transient can be explained and modelled as a combination of the two mechanisms mentioned above. We show that the current degradation is related to the quality of the gate insulator.

In order to have a reliable estimate of the long-term degradation of a-Si:H/SiN TFTs under normal operating conditions, we subjected different a-Si TFTs to an uninterrupted sequence of positive gate voltage stress, relaxation and negative gate voltage stress, relaxation. The drain current is very sensitive to the charge trapped at the interface and thus we appreciate that valuable

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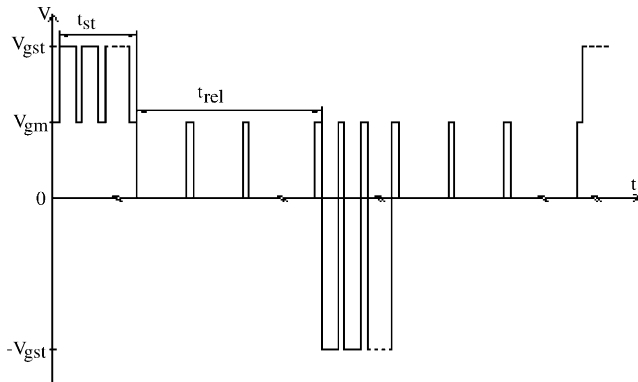

Fig. 1. Measurement sequence used in our experiments.

information about the interface and near interface region in both insulator and semiconductor layers can be retrieved from the decay/recovery of drain current in time. The advantage of the method we referred to is that the stress is automatically switch on and off in order to measure the drain current at selected time intervals during stress/relaxation. Hence, less influence of the charge relaxation from interfacial traps between the interruption and continuation of the stress should occur. Libsch shows that after each interruption of stress and continuation of stress a slight transient occurs [9]. The results were interpreted as due to the electron trapping within the gate insulator near the interface a-Si:H/SiN.

None of the models proposed to account for degradation fit entirely our experimental data (Fig. 1). For the positive gate voltage stress all the models show a good fit but for the periods of relaxation and negative stress we did not find an agreement between the experimental data and the defect-pool and charge injection models. In consequence it is difficult to explain the degradation in our devices using exclusively one of the models in the literature.

A new model named 'progressive degradation model' (PDM) is proposed. The model makes use of Heimann–Warfield theory of trapping/detrapping front [12]. The hypothesis of PDM is that I_{sd} decay/recovery during S+, R−/S−, R+ is due to charge trapping/detrapping on/from existing or created defects in the interfacial layer of a few atomic layers through a tunnelling process.

PDM achieves a consistent fit in any bias condition showing that the degradation can be modelled quantitatively yielding the number of traps involved, their position and the charge dispersion coefficient. To our knowledge it is for the first time when alternative periods of stress and relaxation can be described by a continuous function holding just a set of two parameters.

2. Devices and technique

We performed the tests in 5 duty cycles. Each cycle consists of 4 alternative periods of positive stress (S+)/relaxation (R+)/negative stress (S−)/relaxation (R−) (Fig. 2). In S+ and S− the gate was forward respectively reverse biased with the same volt-

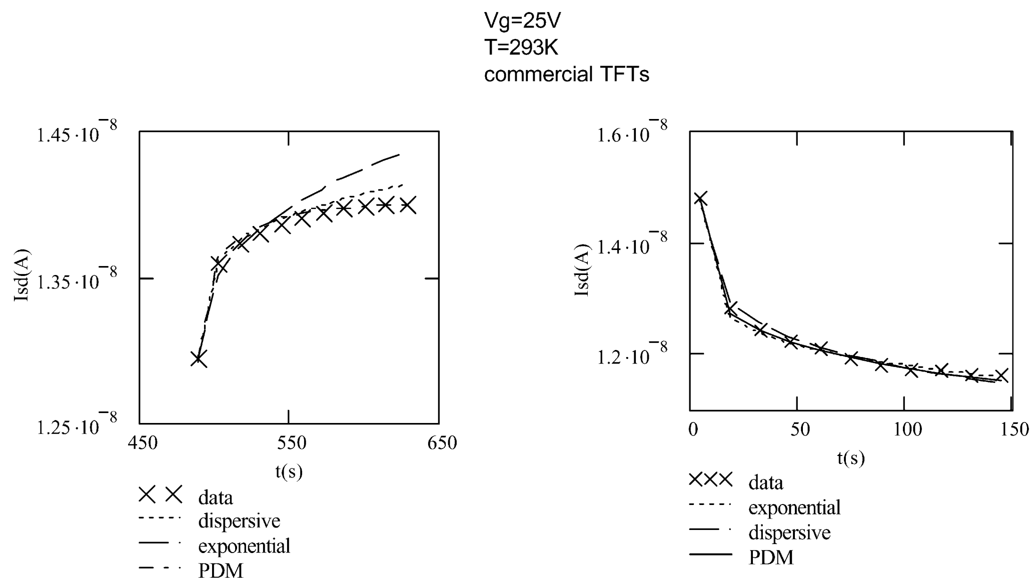

Fig. 2. Time dependence of the source to drain current for S+ (right) fitted by the stretched exponential equation, dispersive equation and PDM and time dependence of the source-to-drain current for S− (left) fitted by the dispersive equation, stretched exponential equation and PDM. Commercial TFTs.

Table 1
Bias value during stress and measurement

		S+	R+	S−	R−
Stress	V_{gst}	25	0	−25	0
	V_d	0.5	0	0.5	0
	V_s	0	0	0	0
Measurement	V_{gm}	10	10	10	10
	V_d	0.5	0.5	0.5	0.5
	V_s	0	0	0	0

age $|V_{gst}|$while $V_d=0.5$ V and $V_s=0$ V and in R+ and R−[1] the three terminals were grounded (Table 1).

The stress (t_{st}) and relaxation (t_{rel}) procedure are interrupted at selected time intervals to measure the source-to-drain current value (I_{sd}) (Table 2) at a low gate bias (above threshold voltage). We are aware of the fact that the time frame chosen for our test is maybe too short to clearly distinct between the degradation mechanisms. We choose this short time in order to avoid irreversible damage to the interface because of prolonged applied gate voltage stress. Apart of the test we subject some TFTs only to positive bias stress for 10^3 s and we notice that the decay of I_{sd} still fits with a power-time dependence.

The devices used in this study are a-Si:H/SiN TFTs (bottom-gated) deposited on Si wafer by r.f.-PECVD [13] (PECVD1 & PECVD2). Electrical characterization of PECVD2 in respect with PECVD1 shows a lower mobility (0.2 compared with 0.7 cm^2/eV) and a larger threshold voltage (3.7 compared with 2.2 V). Geometries (thickness of the layers) of PECVD 1 & 2 are similar. Quality of the amorphous active layer is similar but the nitride stoichiometry is different with a higher N content in PECVD1 device.

For comparison we use also PECVD commercial TFTs (top-gated) on glass which were characterized by $\mu=0.4$ cm^2/eV and $V_t\sim5$ V. Other specific details regarding the commercial TFTs used in this study cannot be provided.

Bottom-gated PECVD and commercial TFTs, after annealing at 220 °C in vacuum for 0.5 h, were subjected to repeated period of different gate bias stress and relaxation at different stress temperature while low drain biased and source grounded. For each experiment a fresh device was used in order to avoid repetitive accumulated stress.

3. Results

3.1. Theory of modelling

In the context of the tunnelling model we assume that the interface extends from the crystallographic interface into the SiN and in that region exist the traps that exchange charges with a-Si:H channel during the time frame of our experiments. Further on we refer only to charged/discharged (filled/emptied) traps.

The degradation due to the applied stress in one sequence of measurements (during 1 cycle) is characterized by two parameters D_{int} and α D_{int} represents the number of interface traps and α is a number related with the reliability of the interface. $D_0 \ll D_{int_0}$ ($\sim 10^3$ lower) and that is why this quantity is neglected in this discussion and it is kept constant throughout modelling.

PDM assumes that the interface traps are uniformly distributed over the energy range but exponentially distributed over distance with a decay length d from the interface according to: $D(x,t)=D_0+D_{int}(t)e^{\frac{-x}{d}}$. The experiments we perform clearly show a strong time dependence of the current especially for S+ and this motivated us to introduce into our model a time dependent interface trap density for the experiment time frame as $D_{int}(t)=D_{int_0}t^{\alpha}$.

The time dispersion coefficient is

$$\alpha=\begin{cases} >0 & \text{if } V_g>0 \\ =0 & \text{if } V_g=0. \\ <0 & \text{if } V_g<0 \end{cases}$$

This α quantity corresponds to an increase in the interfacial trap density during S+ and to a reduction in the interfacial trap density during S−, respectively. There is no enough evidence in the literature to suggest that some Si–Si bonds may recover and become stable by applying a reverse field, but some work reported a reduction of the defects during reverse field experiments [14].

The current measured in the external circuit is written as $I_{sd}(t)=I_0\mp I_D(t)$ where I_0 is the contact current, i.e. the initial measurable current and $I_D(t)$ is the displacement current due to trapping (in S+) or detrapping (in S−) of the carriers in time. This displacement current is expressed by the time variation of the interface electric field and, in consequence, is dependent on the chosen parameters D_{int} and α.

The time-dependence of the source-to-drain current is

Table 2
Time interval during stress and measurement

	S+	R+	S−	R−
Stress	$t_{st}=100$ s	$t_{rel}=300$ s	$t_{st}=100$ s	$t_{rel}=300$ s
Measurement	$t=10$ s	$t=30$ s	$t=10$ s	$t=30$ s

[1] R+/− discriminate between R after S+ and R after S−.

modelled as a time continuous function for the periods of time corresponding to positive stress S+, relaxation R and negative stress S−. For 1 cycle modelled $I_{sd}(t)$ is presented in Eq. (1). That means that for every data set it corresponds a unique pair of parameters (D_{int}, α) to fit all the sequences in one cycle.

$$I_{sd}(t)=\begin{cases} I_0-q\frac{W}{L}\mu V_d\int_{E_v}^{E_c}\int_0^{x_c(t_{st})}D(x,t)G(E,x,t)\mathrm{d}x\mathrm{d}E & \text{if } 0<t\leqslant t_{st} \\ +q\frac{W}{L}\mu V_d\int_{E_v}^{E_c}\int_{x_e(E,t)}^{x_e(E,t_{st})}D(x,t_{st})P(E,x,t)\mathrm{d}x\mathrm{d}E & \text{if } t_{st}\leqslant t\leqslant t_{rel} \\ -q\frac{W}{L}\mu V_d\int_{E_v}^{E_c}\int_0^{x_c(t_{st})}D(x,t)Q(E,x,t)\mathrm{d}x\mathrm{d}E & \text{if } t_{rel}<t\leqslant t_{st} \\ -q\frac{W}{L}\mu V_d\int_{E_v}^{E_c}\int_{x_e(E,t)}^{x_e(E,t_{st})}D(x,t_{st})W(E,x,t)\mathrm{d}x\mathrm{d}E & \text{if } t_{st}<t\leqslant t_{rel} \end{cases} \tag{1}$$

where I_0 is the very first measurement on the device; q, electric charge; W and L width and length of the device; μ-effective mobility; E_c and E_v are conduction and valence band edges, V_d, drain voltage. According to Heimann–Warfield theory $x_c(t)$ and $x_e(E,t)$ are the trapping and detrapping fronts; $G(E,x,t)$ and $P(E,x,t)$ are the trap occupation function for S+ and R+ and $Q(E,x,t)$ and $W(E,x,t)$ are the mirroring occupation functions for S− and R− [12]. Details about modelling of experimental data obtained by our method are going to be published elsewhere [15].

The scenario PDM suppose is that the bias induced defect creation at a-Si:H/SiN interface accompanied by charge trapping cause the t^{α} decay in I_{sd}. As a positive bias is applied on gate the Fermi level shifts closer to the semiconductor conduction band, the defects at the interface, where the channel is formed, fill with carriers and the energy barrier between semiconductor and insulator decreases. The electrons from the a-Si:H conduction band tunnel directly the crystallographic interface. Afterwards they undergo a multiple trapping event: traps whose energy falls below E_f ($E_q<E_f$) are filled with electrons accumulated at the surface.

Trapped electrons are then emitted in R+ since E_q goes above E_f ($E_q>E_f$). Those released electrons close enough to the crystallographic interface can directly tunnel back (charge back-tunnelling) to the conduction band.

In S−, R− periods, the results can be explained either in terms of: (1) holes trapping (S−)/detrapping (R−) or (2) electron detrapping(S−)/trapping(R−).

Once a reverse field is applied, the surface is depleted of electrons (when n-type Si substrate) and holes are attracted from the semiconductor (when p-type Si substrate). (1) The holes tunnel from the a-Si:H valence band and then get trapped in trap levels situated close to the valence band (S−). When the flat band is restored (R−), holes will then de-trap. (2) The electrons de-trap and tunnel back into the semiconductor conduction band (S−). Then, at flat band (R−), the electrons get trapped again.

3.2. Experiments and modelling

Measuring the source-to-drain current (at low gate bias and very low drain voltage in the linear region) when applying a period of gate bias stress gives a transient pattern of the current. During S+ the current decay has power-law time dependence, for R it has a logarithmic-like dependence. Chosen device under test (DUT) for our experiments has very different behavior with a very strong degradation for PECVD2 devices making impossible a characterization at high temperature stress or high bias. The values of parameters-pair $D_{int,}$ α calculated in PDM for all devices under test are shown in Table 3.

As can be seen in Fig. 3 of the experimental data, the pattern of I_{sd} is different for the three types of devices presented here. We investigate in this section why the rate of decay and recovery is different in DUT and what the explanation can be.

It is common for all devices under test that the first two cycles are different from the last three. After the second cycle the pattern become stable in time. PDM shows that this time stability is reached after the second cycle when neither the value of the interface trap density nor the dispersion coefficient change in time (Fig. 4). Our explanation is that, as time proceeds, more and more electrons get irreversibly trapped into the nitride resulting in a repulsive force for the channel charge.

Table 3
Values of the parameters D_{int} and α calculated in PDM

DUT/cycle	D_{int} (cm^{-3}/eV)×10^{18}	α (S+)	α (S−)
PECVD1			
1	4.51	0.17	−0.45
2	2.77	0.29	−0.38
3	2.7	0.3	−0.5
4	2.5	0.3	−0.5
5	2.2	0.3	−0.5
PECVD2			
1	1.8	0.21	−0.01
2	0.45	0.32	−0.01
3	0.4	0.32	−0.01
4	0.38	0.34	−0.01
5	0.36	0.36	−0.01
Commercial			
1	0.33	0.2	−0.7
2	0.16	0.25	−0.68
3	0.14	0.26	−0.66
4	0.13	0.27	−0.58
5	0.13	0.27	−0.56

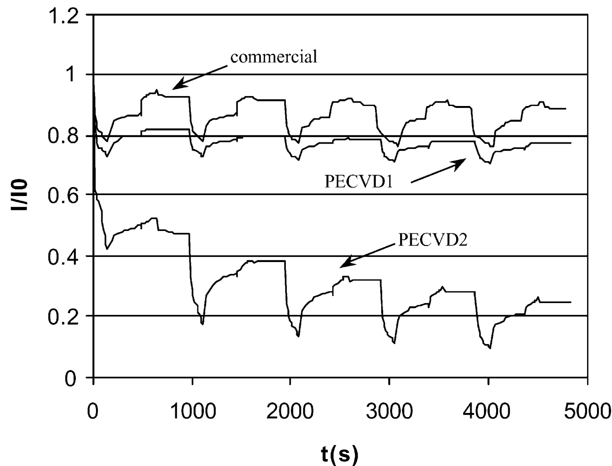

Fig. 3. Normalized currents during S+/R/S−/R sequence over stress time for different devices (5 cycles, room temperature, $V_{gst}=25$ V).

After tunnelling and trapping to some distance inside the insulator, as the bias remains constant, it should be easier for the carriers to redistribute inside the insulator than to tunnel directly from the semiconductor [9]. This accumulated trapped charge is responsible for the nitride degradation that ultimately can lead to instability and breakdown.

The density of charged interface traps depends on the applied bias stress supporting the idea that the relevant carriers (electrons or holes) are injected into SiN by direct tunnelling (Fig. 5).

It is noticeable in the experiment we performed that the current decay/recovery in S+/S− is larger/smaller in PECVD devices than in the commercial ones. For example, in the case of PECVD2 the density of charged interface traps increases rapidly in time (S+) but the density of discharged traps decreases slowly (R, S−) so that a lot of traps remained filled after R and S−. It seems that more charge is trapped than the amount of charge that can be released. This large decay of the displacement current in PECVD 1 & 2 that cannot be recovered even after 10 h of relaxation and negative bias stress suggests that there are large densities of charged interface traps and slow deep traps in the transitional region of a-SiN:H of PECVD devices. But in the commercial devices, a recover of the displacement current is noticed after 18 h of relaxation and 10 h of negative bias stress.

An explanation for the rate of decay and recovery of the displacement current in the devices under test lays on the sensitivity of $I_D(t)$ on the dispersion coefficient. The dispersion coefficient calculated in PDM for S+ is much higher for PECVD 1 & 2 than for commercial TFTs but it is characterized by an increasing step between the first and second cycle (Fig. 6). Meantime the dispersion coefficient in S+ varies very much

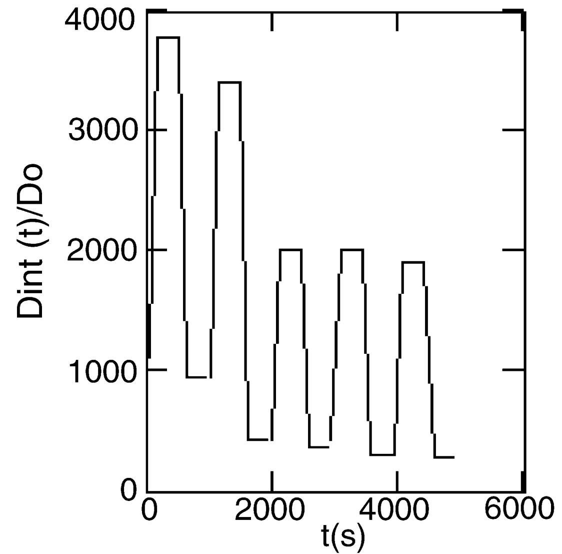

Fig. 4. Normalized ($D_{int}(t)/D_0$) interface trap density in time, commercial TFT at $V_g=25$ V and room temperature. Commercial TFTs.

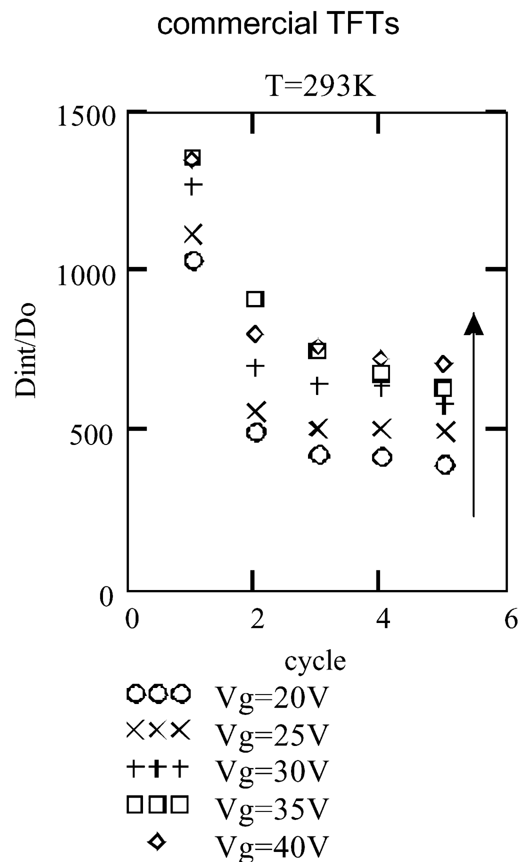

Fig. 5. Normalized interface trap density for each cycle of stress at room temperature in respect with the applied gate bias stress.

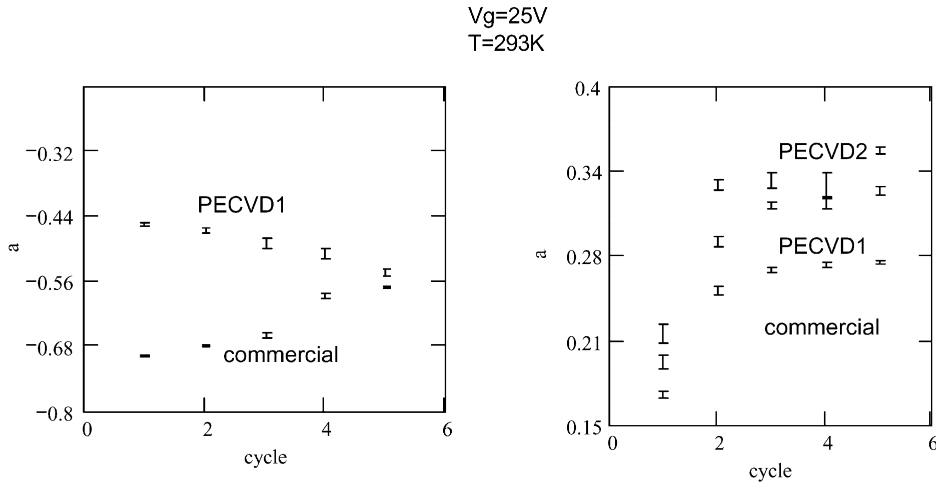

Fig. 6. The time evolution of α coefficient (left hand in S+; right hand in S−) calculated for the commercial and PECVD 1 & 2 TFT at the same stress condition (Table 1). Error bars of the stability of solution.

between the first and the second cycle, it varies only a little in S−. The dispersion coefficient calculated in PDM for S− in all devices is fluctuating around a mean value for all the cycles but it is just a very small value ∼ −0.01 for PECVD2 and therefore it is not included in Fig. 6.

The explanation is that the filling rate of the traps is directly proportional with α whereas the emptying is not. Experiments show that the filling (trapping) is a fast process (∼10 s) but the emptying of the traps (detrapping) in relaxation is a slow one (∼1 day). We believe that misbalance of these two processes results in the current degradation.

The current transient modelled in PDM is very sensitive on the rate of increase of the dispersion coefficient α and α depends on the applied bias and applied temperature. α increases much more when the applied temperature increases than when the applied voltage increases (Fig. 7) and we were able to establish a relationship between α and the applied temperature.

The defect pool model stated $\alpha = kT/kT_0$ where T_0, temperature related with H diffusion [8]. We found that

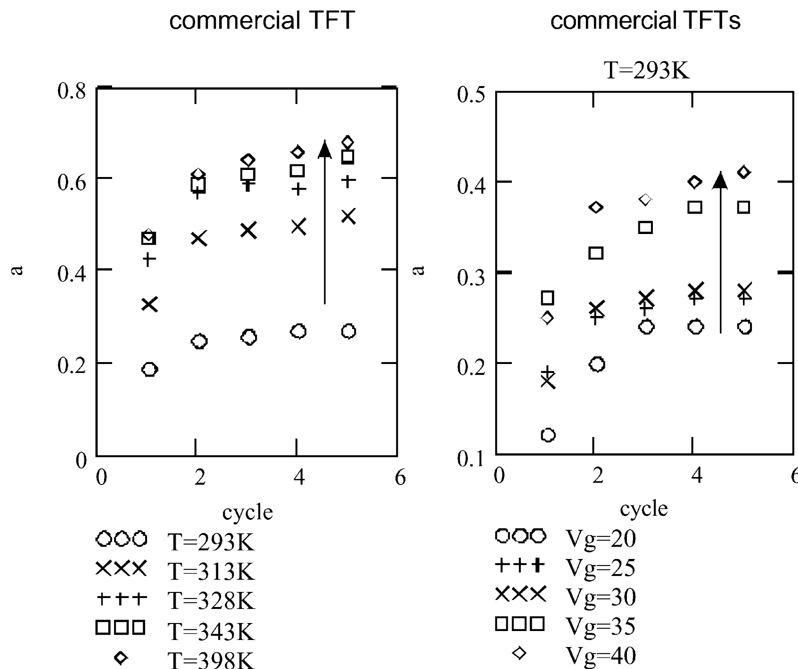

Fig. 7. Temperature dependency of the dispersion coefficient α in S+ of each cycle of stress at $V_g = 25$ V of bias stress (left). Bias stress dependency of the dispersion coefficient α in S+ of each cycle of stress at $T = 293$ K of applied temperature stress (right).

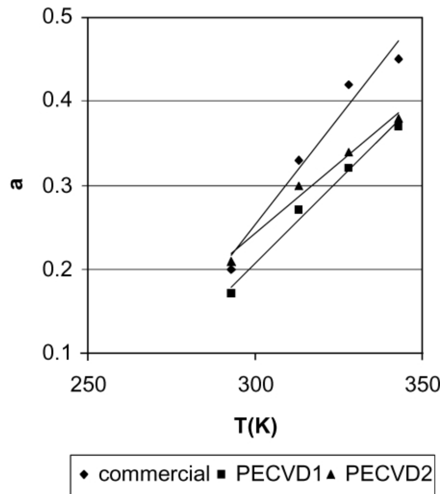

Fig. 8. α in S+ of the first cycle vs. temperature at $V_g = 25$ V bias stress (for $T > 343$ K it becomes temperature independent).

α is not directly proportional with stress temperature but $\alpha = kT/kT_0 + \alpha_0$ where $T_0 \approx 200$ K and $\alpha_0 \approx -1.29$ (Fig. 8) that cast some doubt on the application of defect pool model in I_{sd} transient investigation. For PECVD1 and PECVD2 we obtain $\alpha_0 \approx -0.98$ and $\alpha_0 \approx -0.76$, respectively, for $T_0 \approx 250$ and ≈ 294 K.

It has been shown in the literature that the interface between a-Si:H and SiN has a high density of defects resulting in significant electron accumulation and downwards band bending. The increase in the band bending is due to the decrease in x of SiN_x [16]. Lowering of the energy barrier between the semiconductor and the insulator in sub-stoichiometric insulator explains the difference in the rate of I_{sd} decay in PECVD 1 ($x=1.56$), 2 ($x=1.23$) and state-of-the art commercial TFTs. The degradation appears not to be dependent on the order of deposition of a-Si:H and SiN but to the composition of SiN.

4. Conclusion

In this paper we present a method and a model to study and characterize progressive degradation in a-Si:H/SiN TFTs. The PDM we propose considers that the degradation of source-to-drain current is rather due to a combined effect of charge trapping and interfacial defect creation than a contribution of a unique mechanism.

Stress induced interfacial defect creation at a-Si:H/SiN interface accompanied by trapping of the mobile charge that tunnel directly from the semiconductor leads to a current decaying in time. In other words, the injected carriers from a-Si:H are trapped in a-SiN:H transitional region and a space charge is built up affecting the value of the electric field at the interface. This space charge that is continuously provided from the channel is progressively extended into the gate insulator according to the tunnelling front model proposed by Heimann and Warfield. A possible explanation for the induced interfacial defects is that the interface a-Si/SiN exhibits a strong electron accumulation and SiN contains important quantities of bonded H that can potentially lead to defect states.

A reliable device should take into consideration the stoichiometry of the gate insulator as an important factor in reducing charge trapping and device degradation in a-Si:H/SiN TFTs. We consider the above result as a preliminary result and more work is going to be done in testing many more devices with different SiN composition in order to explain the origin of band bending at a-Si:H/SiN interface and the relation between this and the degradation of drain current under normal operating conditions.

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