Full chip model of CMOS Integrated Circuits under Charged Device Model stress

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***Abstract*— An ESD event which occurs when a charged IC touches a grounded surface is known as CDM type of ESD. The resulting static charge flow from CDM discharge causes large voltage overshoots across the IC causing gate-oxide damage. Measurements of exact internal voltage drops across the gate-oxide during CDM stress, is not possible because of the parasitic influence of the measurement set-up on the discharge path. This paper presents an efficient method of studying the voltage transients across the internal nodes of the IC during CDM stress, based circuit simulation. It presents a basic understanding of the charge flow during a CDM event, based on which an equivalent circuit model of the entire IC under CDM stress is developed. The correctness of the model is verified with the measurement data obtained for input protection structures in the 0.18μm CMOS technology node.**

***Keywords*— ESD; CDM; circuit simulation;**

I. INTRODUCTION

More than 30% of factory returns in the semiconductor industry is attributed to Electrostatic discharge (ESD) failures in the ICs. With the increased usage of automated handlers and decreasing device dimensions especially the thinning down of gate-oxide thickness, more CDM type ESD failure has been reported. Rubbing or sliding of an IC against another surface, results in tribo-electric charging of the IC. When such a charged IC touches a grounded surface, charge flow occurs resulting in large voltage overshoot across the IC. If the voltage overshoot across a gate-oxide exceeds its breakdown voltage, then gate-oxide failure results. It is a one pin event, where the charge from the entire IC flows into the grounded pin, through low impedance path available in the IC layout design.

The total charge stored in the IC depends on the package properties, while the discharge path is decided by the layout design of the IC. Hence CDM performance of an IC depends on both its package and circuit design. To protect the ICs from CDM damage, we need to redesign the protection design in such a way that the voltage overshoot across any gate-oxide is lower than its breakdown limit during CDM stress.

CDM measurements on ICs give only “pass”or “fail” type results and does not provide any further information regarding the circuit behavior during stress. Moreover any attempt made to do in-situ measurements during the CDM stress event, may not give any useful results, because of the large parasitic influence of the measurement set-up on the discharge current path. On the other hand, circuit simulations help us to probe into any of the internal nodes, which are inaccessible otherwise for direct measurements. But we should not forget, that the usefulness of the simulation results lie on how accurately we can model the source and path of the discharge current through the IC under CDM event.

Various simulation and modeling approach have been reported for CDM circuit simulation [1-2]. Most of them have concentrated on compact circuit modeling of the transient behavior of protection devices under CDM stress, or to the input/output protection structures. Jaesik Lee had presented a full chip model under CDM stress [3]. However the current source from the substrate capacitance and its path to the grounded pin was not modeled. In this paper, we present a systematic analysis on the various CDM current source and their discharge paths to the grounded pin. CDM results have been

reported to depend on package capacitance, substrate resistance, parasitic discharge paths in the design, bus line capacitances and resistances. The analysis helps us to understand the role of each of these parameters on the CDM current. Based on this an equivalent circuit model of the CDM test set-up is developed. CDM simulation helps to study the voltage transients across the IC. We then apply the proposed compact simulation method to an ESD input protection structure and the influence of few design variations on the voltage transients across the gate-oxide of their input buffer MOSts are studied.

This paper is organized as follows: In the first section, basic understanding of a CDM stress event is detailed. In the next section, building of the full chip circuit model of an IC under CDM stress is described. The CDM simulation results on the input protection structures are presented in section IV. The simulation results are compared to their CDM measurement results. The influence of design variations on their CDM performance is investigated in section V. In the final section we summarize the results of our work.

II. BASIC UNDERSTANDING OF CDM

A. *Field induced CDM (FCDM) test method*

Among the various test methods available to produce CDM stress, the non-socketed, field induced test method is proven to be more close to real life CDM event. Schematic sketch of the tester set-up is shown in figure1. The IC under test is placed in its dead bug position (pins facing up) on the field plate, which is connected to a high voltage supply. The value of the high voltage supply determines the stress level. The discharge is initiated by touching the desired pin with a pogo pin connected to the ground plane.

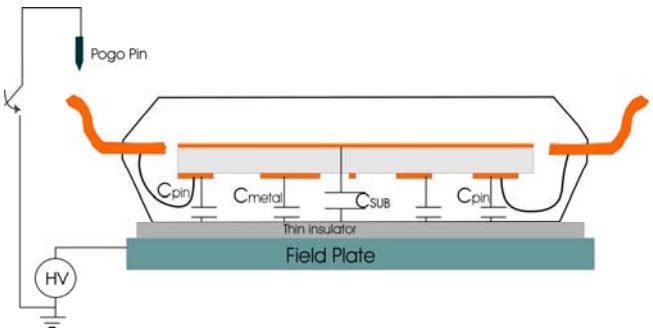


Figure 1. Chip under FCDM test conditions.

B. *Lumped circuit model of IC under FCDM*

An IC consists of several conducting layers, including the die attachment pad, various metal lines like the V_{SS}, V_{DD} VDD bus rails, lead pins, bond pads and so on. All these conducting layers form several capacitors with the field plate as shown in figure1. By placing the IC on a metallic chuck connected to a high voltage supply (field plate), its potential is raised to that of the field plate. When the grounded pogo pin touches one of the IC pins, discharge of these capacitors is initiated. Thus the total CDM current is nothing but the summation of all the discharge currents from these capacitors.

Evaluation of all these capacitors and inclusion of them into the model, can make it way too complicated in studying their individual contribution.

To keep things simple we only model C_P, C_{SUB}, C_{SS} and C_{DD} and neglect the rest. This approximation is fair enough because the influence of each of these capacitors on the CDM current depends on its magnitude (i.e the amount of charge in it).

C_{SS}, C_{DD} – Capacitance formed by the V_{SS} and V_{DD} bus line respectively with the field plate (package). Its value is highly circuit design dependent. Hence for the first step of analysis we have neglected its effect.

C_P – Capacitance of the lead frame with the package.

C_{SUB} – Major amount of charge is coupled with the capacitance formed by the die attachment pad. For convenience let us call it as C_{SUB}. The path of the discharge current from the die attachment pad to the ground is through the substrate (bulk material) into the grounded pin. The entire circuit design is in the top epilayer of the substrate. All the circuit elements are either directly or indirectly connected to the substrate and thus to C_{SUB}. See figure 2. This also explains the distributed nature of CDM failure and its sensitiveness to the substrate resistivity [4]. Unfortunately C_{SUB} capacitance, inspite of its obvious presence and significant role in CDM type of ESD stress, has been neglected in the models presented before.

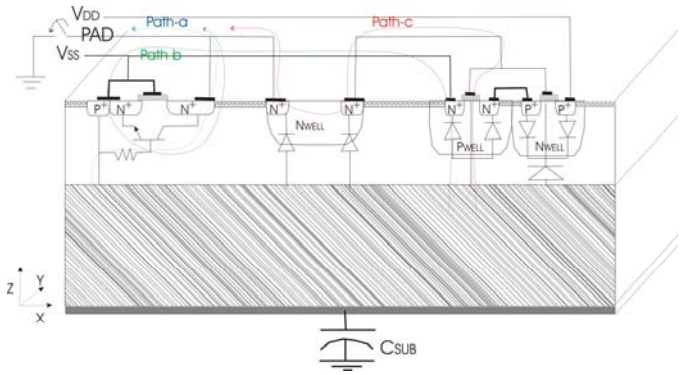


Figure 2. Cross-section of an IC showing the different discharge paths of C_{SUB}

The basic equivalent circuit that can well suit an IC under FCDM stress is shown in figure 3. The capacitors

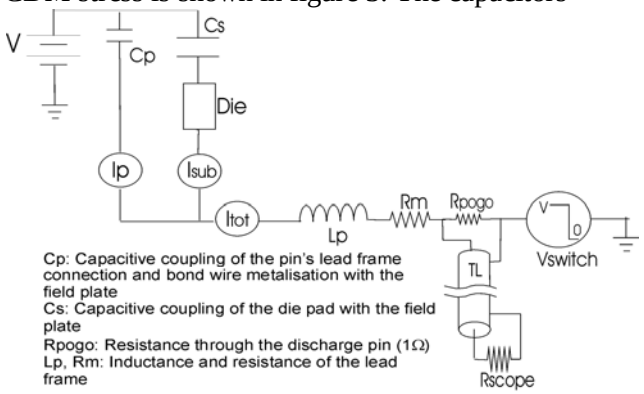


Figure 3. Lumped circuit model for an IC under FCDM test set-up

C_P and C_{SUB} are precharged to the initial stress level. CDM discharge is initiated by the sudden switching of V_{SWICTH} from the stress level say V_{CDM}V to 0V. Notice that the discharge current from CP does not flow through the circuit and hence does not have much influence on the CDM performance of the IC. But it will have a major contribution to the total CDM current measured. The important addition to the previous CDM models presented by other authors, is the inclusion of C_{SUB}. The correctness of this model is studied by comparing the simulated and measured discharge waveform of a 80 pin QUAD package when its $_{VSS}$ pin is discharged. See figure 4.

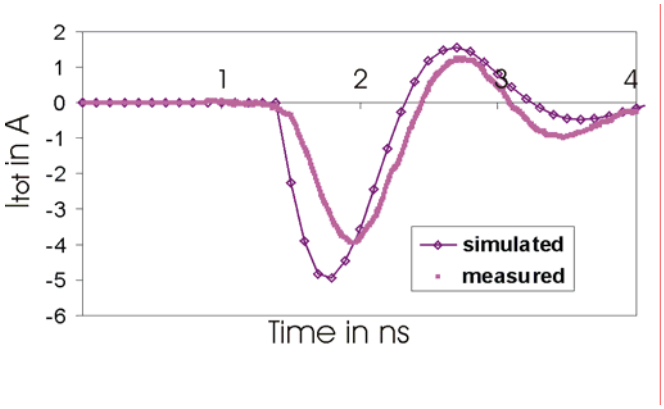


Figure 4 . Simulated and measured CDM discharge current of an IC in a 80 pin QUAD package. Lp = 10nH, Cp = 2pF, Cs = 8pF

III. CDM CIRCUIT MODEL

This section explains how the various elements of the IC are modeled in the full chip equivalent circuit.

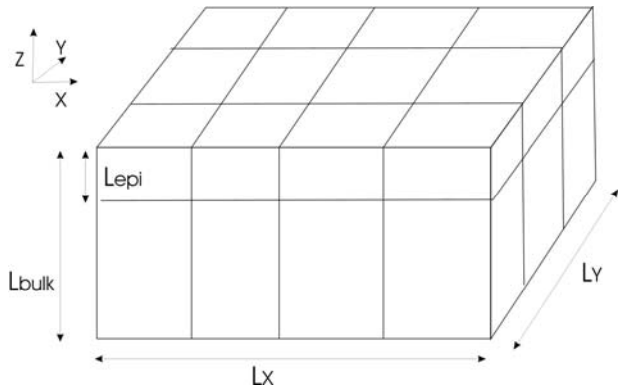
A. IC package

Package plays a significant role in CDM discharge current. They form the main source of charge and also part of the discharge current. The package material (capacitances associated with the IC package) determines the amount of charge stored on the IC. Other package parasitics like pin series inductance L_P and resistance also plays a significant role in the pulse shape of the discharge current. The package parasitics are measured from S parameter measurements.

B. Substrate capacitance and resistance

There are several research works done on modeling the substrate resistance and its impact on the performance of an IC. It is well beyond doubt that substrate has an important role to play, as it lies common to all the circuit elements. All the research in this field of substrate modeling is limited to the surface level. The conventional substrate modeling deals with modeling the substrate resistance from one point on the circuit to another. The scenario is a little different in the case of CDM where the current flow is from the die to a point on the circuit.

The entire volume of silicon die is subdivided into smaller unit volumes as shown in figure 5-a. Each subunit has atleast two layers and is modeled into a lumped resistive network as shown in figure 5-b. The epilayer and the bulk can has different doping densities and hence have different specific resistances.



5-a Subdivision of substrate into smaller unit volumes

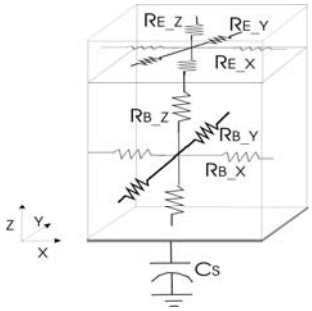


Figure 5-b. Lumped resistive model for a unit silicon volume

One end of this resistive network in Z direction is connected to the substrate capacitance and other end to the circuit elements in that volume. The equivalent resistance in the X, Y and Z directions and capacitance for each subunit are calculated as shown below,

$$R_i = \rho \cdot l_i / l_j . l_k$$
$$C_S = C_{SUB} \cdot (l_i \cdot l_j) / L_X \cdot L_Y$$

C_{SUB} – total capacitance of the die attachment pad with the field plate

ρ – substrate resistivity of the bulk/epilayer

l_i l_j, l_k – dimensions of the subunit in the x, y and z direction respectively

C. Protection device

The physical parameters strongly influence the device behavior under transient conditions. The behavior of the protection devices is modeled by its equivalent compact circuit model [5]. The transient device series resistance can increase up an order of magnitude during the fast rising slopes of CDM events. Hence, the transient turn-on behavior of protection devices has been taken into consideration in the model.

D. IC design

All the circuit elements are either directly or indirectly connected to the substrate. These different contacts on the substrate provide innumerable number of discharge paths for C_{SUB} to the grounded pad. Figure 2 shows the different discharge paths for the CDM current for an input cell structure. They can be divided into two different categories. The most desired path and the most unwanted path.

1) Desired path:

The most desired path of the current would be through

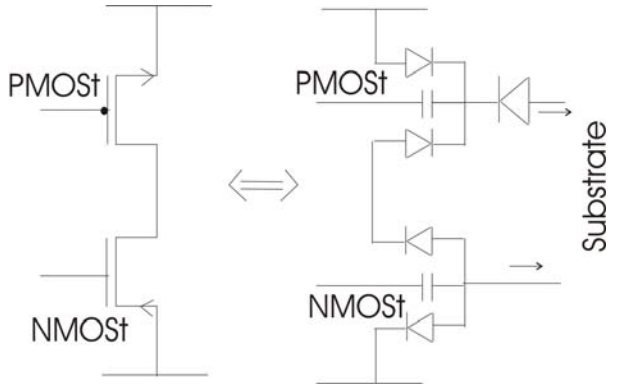


Figure 6 CDM circuit model for CMOSt

the V_{SS} and V_{DD} line contacts on the substrate via the protection device to the grounded pad. The reason is twofold. All the I/O pads are connected to the power rails via a protection device. Moreover the V_{SS} and V_{DD} line contacts are well spread and have large number of contacts on the substrate. The $_{VSS}$ contact can be viewed as a N+ to P substrate diode connection and that of V_{DD} as two diodes connected back to back. See figure 2. But here again we should not underestimate the resistance of the V_{SS} and V_{DD} power lines.

2) Undesired path

The most undesired or unwanted path is through the thin gate-oxides of the MOSt to the grounded pad. Also the internal core circuitry is strongly coupled to the substrate through the gate-oxides in the circuit. This parasitic capacitive coupling of the core circuitry to the substrate can provide unwanted discharge paths through the internal circuitry resulting in gate-oxide failures. This discharge path has not been addressed for the first time in this paper. An IC in the CMOS technology consists mainly of the CMOSts. Any CMOSt on the IC can be modeled as shown in figure 6 under CDM stress. This is because the MOSt is no longer active, as its drain and source connection are at the same potential. It is only the

parasitic path available on the design that provides the discharge path.

IV. GATE-OXIDE FAILURE THRESHOLD

A gate-oxide failure results when the voltage across the gate-oxide exceeds its oxide breakdown voltage $V_{BD,}$ or if the charge stored in it exceeds the charge to breakdown Q_{BD}. Gate-oxide damage is seen by the increased leakage current during it normal operational conditions. The DC dielectric breakdown voltage for the gate-oxides in input structures studied is 3.5V (3.5 nm thick gate-oxide). But under transient conditions, the breakdown voltage is extrapolated from 1/E model. The model states that V_{BD} depends on the length of the applied pulse and increases with shorter pulses [6].

From 1/E model extrapolation, the V_{BD} is found to be

~ 20V for a stress time of 1ns. But the extrapolation of this model to ultra thin gate-oxides is unreliable and we are likely to overestimate V_{BD}. This is because as the oxide thickness decreases, the direct tunneling current increases exponentially resulting in shorter time to breakdown [7]. CDM discharge results in large voltage and current transients across the gate-oxides. At these conditions the thermal and current crowding effects has to be considered as well [8]. Considering these effects into consideration, and applying the suitable correction, V_{BD} is estimated to be 15V.

V. CDM CIRCUIT SIMULATIONS AND MEASUREMENT RESULTS

Test structure with an I/O ring of input and output structures with several design variations were made in the 0.18µm technology node. CDM performance of two input protection structures is studied in detail in this section. The entire IC die is modeled as a resistive network with finer divisions (2µm) near the region of interest namely, the input buffer and courser divisions (80µm) at other locations, with gradual variation near their interface. The circuit design including its power lines and various circuit elements in the test structure design are replaced by their equivalent CDM circuit model and connected to the substrate resistive network in their respective locations as in their layout. Thus a

3-D circuit model of the entire IC under CDM stress condition is made.

A. Design 1

Schematic sketch of the input protection structure is shown in figure 7-a. The protection structure consists of a

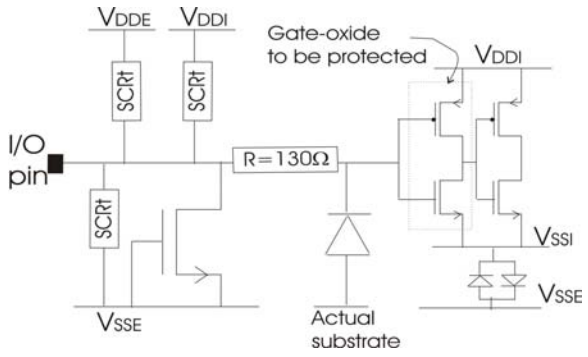


Figure 7-a. Schematic sketch of input cell - design 1

phi-network, with primary and secondary protection separated by a decoupling poly resistor of 130Ω. The primary protection is by an SCRt and a ggNMOSt connected across the discharge pad and the $_{VSS}$ line, while the secondary protection element is a diode connected to the substrate. Gate-oxide failures are generally reported in MOSt of the first input buffer. Any voltage overshoot beyond its gate-oxide breakdown voltage (> 15V) would result in CDM failure. This could be V_{GS} or V_{GD} or V_{GB} i.e Voltage drop across the gate-oxide can be between its gate and source or drain or bulk respectively. Voltage transients across the gate and bulk of both PMOSt and NMOSt at -250V CDM stress is shown in figure 7-c. Also shown in the figure is the potential drop across the gate and source of the NMOSt. Figure 7-b shows the potential drop across the gate and various substrate nodes in the input cell of design 1.

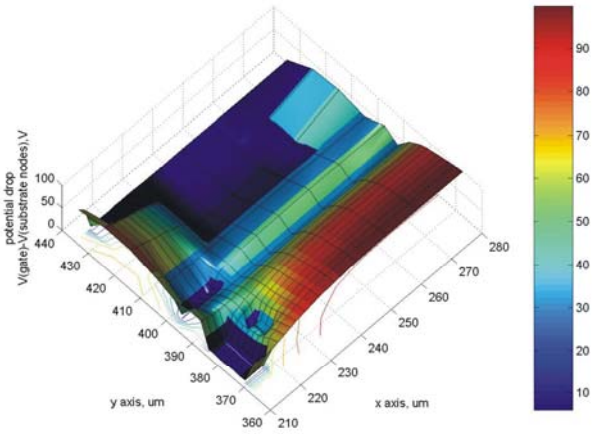


Figure 7-b. Potential drop across the gate and input cell substrate nodes

From figure 7-c, we see that the voltage across the gate and the substrate (Pwell) of the NMOSt exceeds

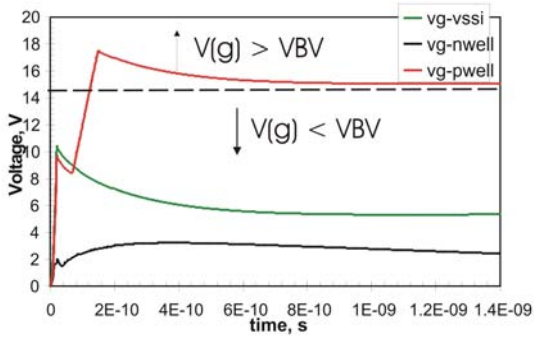


Figure 7-c. Voltage transients across the gate-oxide during CDM discharge simulation

VBD of the gate-oxide, while that of the PMOSt (Nwell) is much lower than the breakdown limit. CDM measurements on these test structures showed that almost all the input cells with this design had failed at very low stress level of -400V. FA on these test structures showed gate-oxide failure generally at NMOSt and occasionally at the PMOSt.

B. Design 2

Input protection structure of design 2 is shown in figure 8-a. Variation of design 2 from design 1 are,

- Additional secondary clamping device connected to the same $_{VSS}$ line as the input buffer
- Increase of poly resistor from 130Ω to 410Ω

Potential drop across the entire input cell substrate

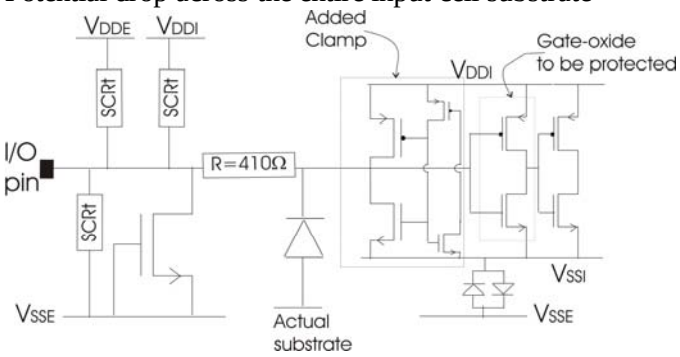


Figure 8-a. Schematic sketch of input cell - design 2

nodes and the gate of the input buffer under CDM stress of -250V is shown in figure 8-b. Voltage transients across the gate is shown in figure 8-c.

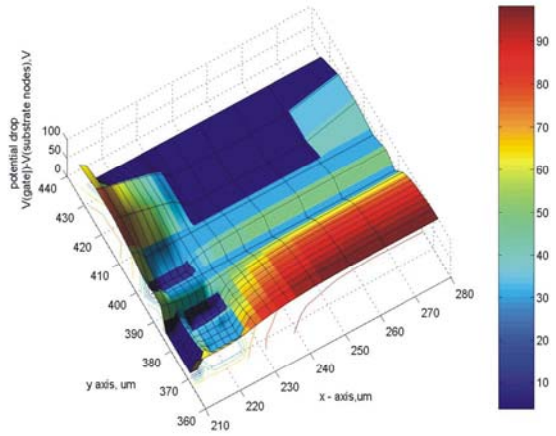


Figure 8-b. Potential drop across the gate and input cell substrate nodes

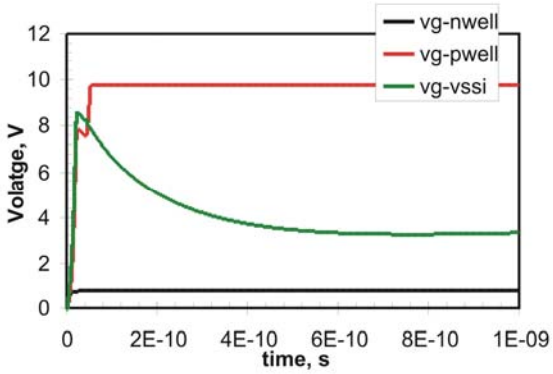


Figure 8-c. Voltage transients across the gate-oxide during CDM discharge simulation

Apart from these intended design modifications there has been an unintentional modification in the distance of the substrate contact from the gate-oxide location. The Pwell and Nwell regions have been expanded to include the additional clamping device. This has reduced the effective distance of the substrate contact (P+ contact of the substrate to the $_{VSS}$ line) from the gate-oxide of the input buffer. In this case transient voltage across the gate-oxide is much lower than its breakdown limit, hence they must be CDM robust. CDM measurements on these test structures with this input cell design did not show failure event at -1000V CDM stress.

VI. Conclusions

Basic understanding of the various sources and possible discharge paths during a CDM event is presented. This has helped in recognizing the most important source, namely substrate capacitance. Lumped circuit model for an IC under FCDM test set-up is presented. The correctness of the simulated discharge

waveform is verified with the measured CDM waveform. The model is then extended to include the distributed nature of CSUB and its discharge current path through the substrate. CDM simulation on the circuit model is used to study the voltage transients across the gate-oxide of the MOSt at the input buffer location, of the input protection structure in two designs. The voltage overshoot across the gate-oxide exceeds its breakdown limit in design 1 making it CDM weak design, while for design 2 it is well below its breakdown limit making it CDM robust design. CDM measurements also reveal design 1 to be CDM weak (fail above -400V CDM stress) and design 2 to be CDM robust (pass -1000V CDM stress). Thus we see a good agreement between the simulated and measured CDM results.

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