# Testing Superconductor Logic Integrated Circuits

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*Abstract—Superconductor logic has the potential of extremely low-power consumption and ultra-fast digital signal processing. Unfortunately, the obtained yield of the present processes is low and specific faults occur. This paper deals with fault-modelling, Design-for-Test structures, and ATPG for these integrated circuits.*

*Index Terms— Fault modelling, Design-for-Test, Defect Monitor Structures, ATPG*

## I. Introduction

Semiconductor technologies are struggling to provide the means for the requirements of realising the latest applications. Various hybrid technologies are being implemented for these purposes. Still, implementations of very high-end applications such as a real peta-flops scale computer [1] are beyond the scope of these technologies. Various superconductor-based technologies, especially based on Rapid Single Flux Quantum (RSFQ) circuits, are emerging as replacements for the implementation of these high-end applications [2]. Super-Conductor Electronics (SCE) suits best for applications requiring ultra high-speed switching and large-volume data processing per unit time, where other technologies are far behind in their performances [3].

Even though much research has been carried out in the past for device development, little work has been carried out with regard to the testing of SCE circuits. A systematic test methodology for testing devices in SCE is still in its infancy. We have started research on DBT for SCE circuits and presented already several results [4-7]. As a part of DBT, various fault models are proposed for SCE circuits. These are models based on work in structural testing and analysis of SCE processes [4-7].

A test methodology based on a DfT approach is required for the verification of fault models. The fact that an individual Single Flux Quantum (SFQ) pulse is extremely difficult to be detected has been hampering the verification process. We propose DfT schemes to detect an individual SFQ pulse and apply such a technique to verify the proposed fault models and even more enhance the *testability* in complex SCE systems.

As a continuation of our research in DBT of an RSFQ D-type Flip-Flop (DFF) [6, 8], extensive studies were conducted on such a DFF realised in a mature Niobium (Nb) process at HYPRES Inc., NY [9]. HYPRES is one of the leading SCE foundries where commercial production of RSFQ devices has been started. The operating temperature of these devices is 4 K. The defect-prone locations in the DFF were identified and defects were deliberately inserted into the device.

The organization of this paper is as follows. The next section summarises the results from our research on the occurrence of defects in SCE chips based on *defect*-monitors, and translates the results in occurring logic faults in SCE circuits via their layout and circuit simulation. Based on these results, a *logic* test chip was designed and manufactured including faulty devices, to verify the models to be used in ATPG. The last section focuses on Design-for-Test structures, which are used for fault evaluation and the increase of testability in complex SCE systems.

## II. Fault-modelling and ATPG in Superconductor Logic

Compared to standard Silicon technology, very little information is available on occurring defects in superconductor Niobium-based processing. This is related to the fact that the processing is less standardized and mature as compared to Silicon; furthermore, several implementations have a military background.

In the past four years, we have developed several test chips in two different though related processing technologies (JeSEF [8], is under development and a commercial process by Hypres [9]). In this paper, we discuss the details of the developed test-chips for verification of *logic* fault models in the HYPRES process. Extensive measurements with regard to the occurrence statistics of defects have been carried out previously [4-7]. In figure 1a, part of a large ranking list is shown

based on these measurements. The top seven of defects are dealing with *cracks* in the top metal layer M3. Ranking 8 and 9 are *shorts* between the metal layers M2 and M3. An out-of-specification critical current of a Josephson junction translates in a short. Of course this ranking assumes the equal occurrence of sensitive critical areas. In an actual layout of a circuit, this is usually not the case, and hence lower-ranking defects can still be the major cause of failure of a circuit. Figure 1b shows part of the layout of a DFF, where the M2 layer has been modified to *emulate* a crack in metal layer M2. Figure 1c shows on top the fault-free behaviour of this circuit, and the lower figure illustrates that three SFQ pulses have disappeared in the faulty case at the output.

| a) | | b) | c) |
|---|---|---|---|

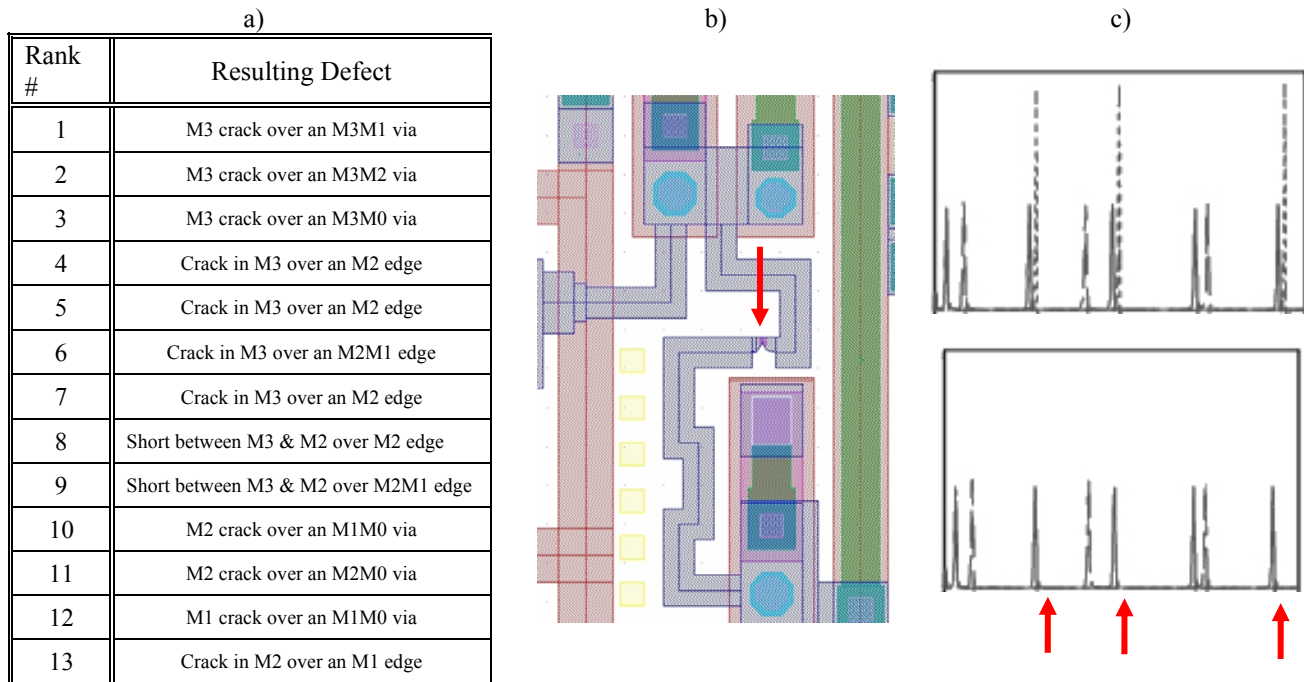| Rank # | Resulting Defect |
|---|---|
| 1 | M3 crack over an M3M1 via |
| 2 | M3 crack over an M3M2 via |
| 3 | M3 crack over an M3M0 via |
| 4 | Crack in M3 over an M2 edge |
| 5 | Crack in M3 over an M2 edge |
| 6 | Crack in M3 over an M2M1 edge |
| 7 | Crack in M3 over an M2 edge |
| 8 | Short between M3 & M2 over M2 edge |
| 9 | Short between M3 & M2 over M2M1 edge |
| 10 | M2 crack over an M1M0 via |
| 11 | M2 crack over an M2M0 via |
| 12 | M1 crack over an M1M0 via |
| 13 | Crack in M2 over an M1 edge |



Figure 1:   a) Part of the ranking list for defects in a Niobium-based process.  b) Modified layout of a D-type flip-flop emulating a crack in M2 (13 in a).
        c) Fault-free and faulty behaviour of the circuit in 1b as result of defect 13 in 1a.

In order to observe the behaviour of these faults under super-conducting circumstances and verify the modelling, a *logic* test chip has been designed by us and manufactured at Hypres [9]. In figure 2a, the total test chip is shown which includes one fault-free and a series of faulty D-type flip-flops including support circuitry. A single DFF circuit is shown in figure 2b. A detail of the Cadence Virtuoso layout of this DFF including an emulated crack (arrow, number 13 in figure 1a) in M2 is presented in figure 3a, and its actual implementation in figure 3b.

The modelling of the major (*static*) defects in the circuits can be mapped on a variable resistance in the circuit simulator JSIM [10] depending on the nature of an open (100k $\Omega$), a crack (e.g. 0.65 $\Omega$), short (between 1 –100 m$\Omega$) and an out-of-specs critical current. In the latter, a short replaces the Josephson junction. At logic level, a defect translates in either correct behaviour, or the absence or generation of SFQ pulses under certain input conditions. Hence, as *basis* a stuck-at based ATPG can be used. Experiments [7] show that the masking of faults occurs in superconductor logic. This means an inherent decrease in fault coverage, unless Design-for-Test structures are inserted at strategic positions.

In Table I, four test vectors have been used for the detection of several defects in superconductor DFFs. Defect number 4 (yellow) corresponds to the defect shown in figures 3a and 3b, being an intralayer M2 short. As the Table I shows, all 4 test vectors are each capable of detecting this defect. In contrast, defect 2, being an intralayer short in M2 between coils L2 and L3 in the DFF (figure 6), is not detected by these vectors. The shaded areas in the table indicate this lack of detection. Fault masking is one of the possible causes of non-detection.

Table I:   Test vectors and different defects in a D-type flip-flop. Grey areas indicate non-detection of the defect by associated vector(s).
        Yellow area concerns the defect as shown in figure 3a and 3b.

| Defect Number | Applied test vector and corresponding results | | | |
|---|---|---|---|---|
| | 10101010101 | 11011011011 | 11101110111 | 10010010010 |
| 1 | 00000000000x | | | |
| 2 | 010101010101 | 011011011011 | 011101110111 | 01001001001x |
| 3 | 000100100101 | 00010010101x | 000101010101 | 00001001001x |
| 4 | 101001101001 | 101101110101 | 101110111101 | 10010010001x |
| 5 | 010101010101 | 011101101101 | 101101110111 | 01010010010x |
| 7 | 010101010101 | 011011011011 | 0101110111x | 01001001001x |
| 9 | 00000000101x | 00000011011x | 000001011101 | 00000000000x |
| 10 | 00101010101x | 001011011011 | 001101110111 | 001001001001 |
| 11 | 010101010101 | 011011011011 | 011101110111 | 01001001001x |
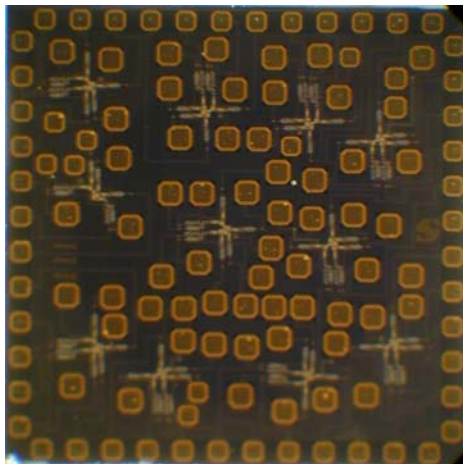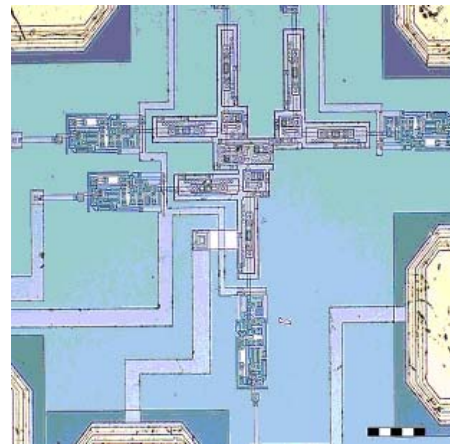


Figure 2: a) Photomicrograph of the complete test chip for super-conducting logic devices designed with Cadence at MESA+ and implemented by Hypress Inc. b) Detail of a superconducting D-type flip-flop including support circuitry.
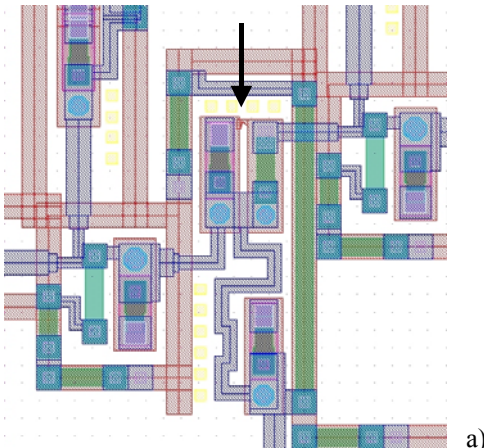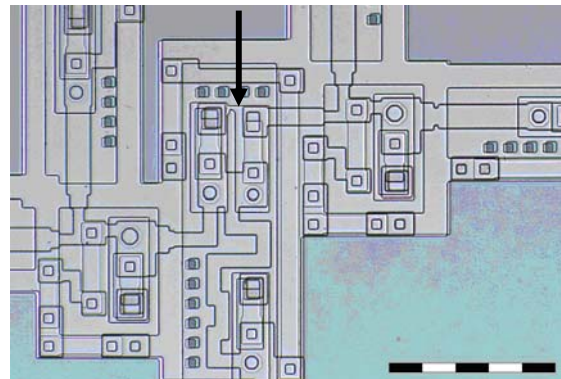


Figure 3: a) Cadence modified layout (arrow) emulating a fault (M2 intralayer short) in a D-type flip-flop. b) Photomicrograph of a faulty super-conducting D-type flip-flop including support circuitry emulating an intralayer M2 short.

## III. The Requirement for DfT in Superconductor Logic

Similar to the requirements of controllability and observability in CMOS digital circuits, also the testing of superconductor logic requires sufficient testability to guarantee the quality of the circuits. This especially holds in our case where detailed evaluation of faults in a circuit is needed, and extremely low temperatures (4 K) and high-speed (~20-40 GHz) are concerned. Besides also the complexity of superconductor logic is increasing nowadays, like implementations of microprocessors [1] and its application in peta-flop computing systems [2].

As an example, figure 4 shows the scheme of a serially connected three-stage adder in superconductor technology. A single stage (dashed box) in the serial adder consists of three basic blocks, which are also showed in detail in figure 4. The CSSA is a Carry-Save Serial Adder cell, consisting of 12 Josephson junctions. The NR and DR cells are respectively the non-destructive and destructive read-out blocks. The latter is actually a DFF. Hence a single slice of the adder requires 22 Josephson junctions.
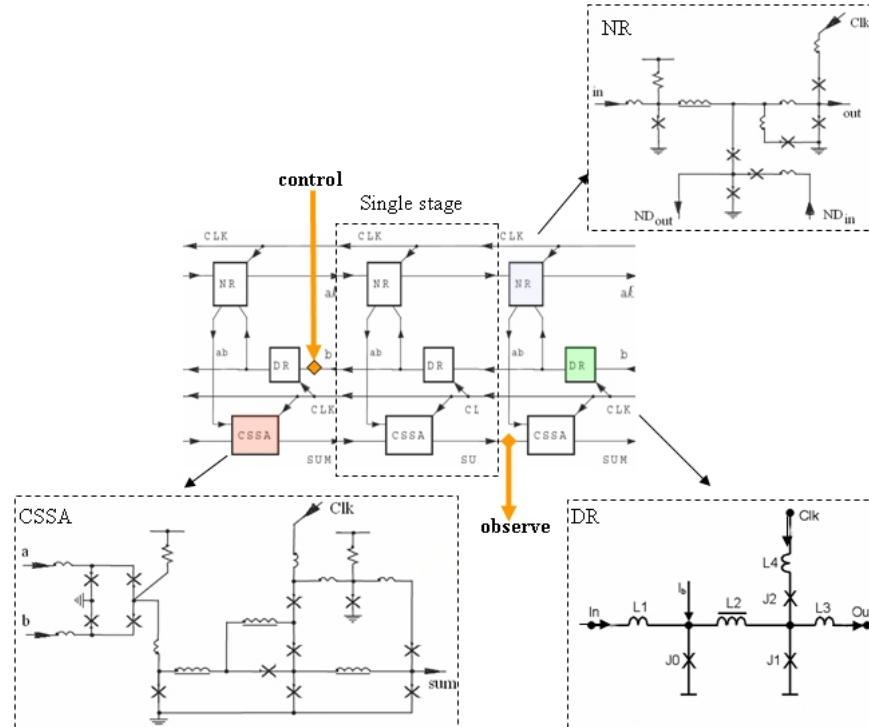


Figure 4: Scheme of a superconductor serial adder consisting of three stages, including the JJ schemes of the three basic circuits in a stage. The bold arrows indicate the required observability and controllability of embedded nodes in this adder.

The bold arrows in figure 4 with the text "control" and "observe" respectively refer to the desired external control and observation of embedded nodes in the serial adder for the purpose of enhanced testability. As JJ-based circuits miss the feature to have an easy fan-out and are normally read-out destructively, this complicates DfT circuits structurally.

## IV. Design-for-Test for Superconductor Logic

The Design-for-Test structures for superconductor logic can be divided into a structure for multi-observation and single control. This is a result of the necessity to convert common logic signals to short SFQ pulses and vice versa. In the next section these sections will be discussed in detail.

### a. The observation DfT section

In figure 5, the overall design of our multi-observation DfT circuit is shown. It is a simplified scheme, as fine-tuning in terms of timing is usually required by means of JTL (Josephson Transmission Line) elements. As an example only two observation inputs are shown. The multi-observation approach is favoured because the SFQ-to-DC circuit, required to measure the output using normal equipment, is a rather complex circuit as shown at the right side of figure 5.
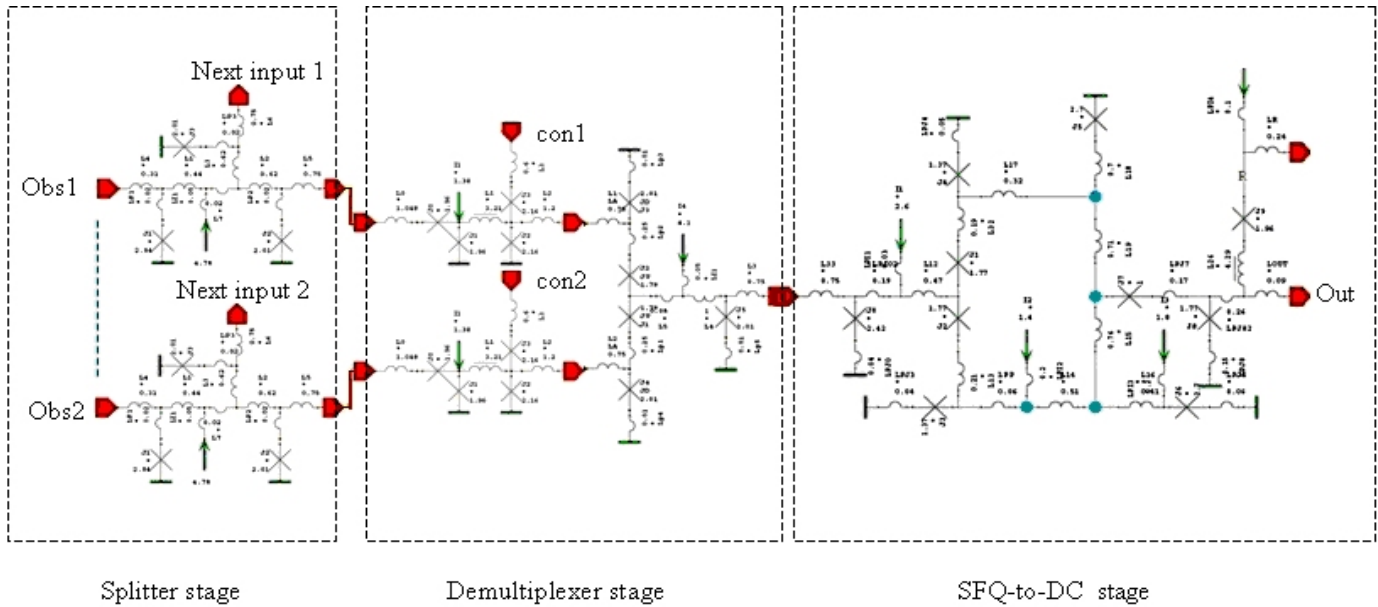
Figure 5: Scheme of the proposed multi-observation Design-for-Test section, consisting of a splitter, demultiplexer and SFQ-to-DC stage.

Because of the destructive nature of the logic operations, the observation inputs require so-called *splitters*, which is the first stage at the left of figure 5. The detailed scheme of a single splitter circuit is seen in figure 6a including the design parameters. In these splitter circuits, a copy is generated of the SFQ pulse at OUT1, which is used to be the input of the next stage within the actual logic (SU in figure 4). The other pulse at OUT is used for observation in the DfT structure and connected to the next demultiplexer stage (Figure 4).
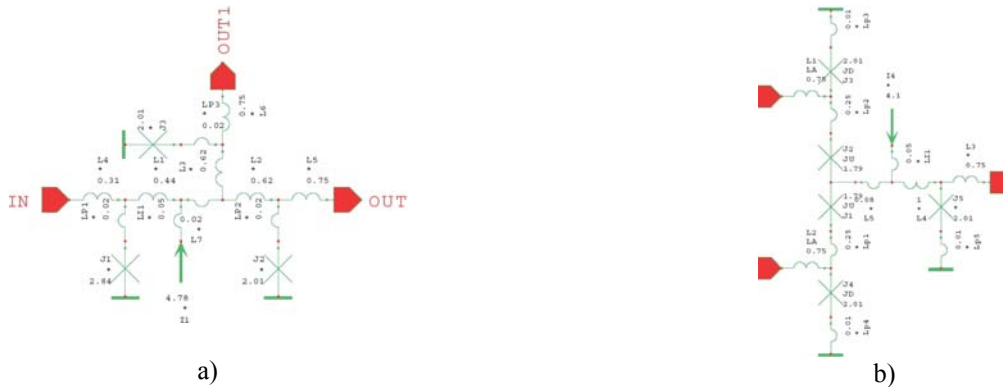


Figure 6: a) Detail of the splitter circuit in the DfT structure in figure 5. b) Detail of the merger circuit in the DfT structure in figure 5. Design parameters such as critical currents and coil values are included.

The second part of the DfT structure is the *demultiplexer* stage. Depending on the number of required observation points (here two), several demultiplexers are included. It was chosen to construct the demultiplexer with DFFs (see figure 3), which are combined in a tree-like structure with the help of merger circuits. In figure 5, in the case of two observation points, only two flip-flops and a single merger are necessary. The flip-flops are actually misused, by using the normal clock input as control input for the control signal (con1 and con2 in figure 5). The merger circuit, of which a detailed circuit implementation is shown in figure 6b, actually merges two SFQ pulses after each other in time. Hence, if one of the two does not appear, only the other one will, thus acting as a demultiplexer.

In the last stage, this SFQ pulse is converted into a signal, which can be handled by conventional test equipment. The output of the SFQ-DC converter can be observed using an oscilloscope, as the voltage-level will be around 400 mV. It is reminded that SFQ pulses have a very low output signal value and are extremely short in time. The operation and internal pulses of this rather complex block are shown in figure 7. This is also the reason why it is being shared by several observation points.
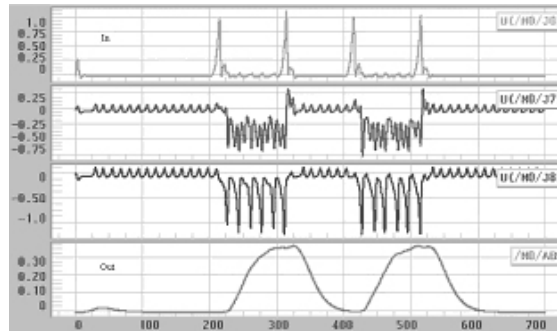
Figure 7: Behaviour of the SFQ-to-DC stage, including internal signals, at the end of the DfT structure.

### b. The control DfT section

In figure 4 of the serial adder, the embedded node b is assumed to need to be controlled. As already stated before, this operation requires another DfT circuit as compared to the previous one. In this case, a conversion from a normal word / bit generator to control the node in terms of an SFQ pulse at the node is a necessity. There have been made designs before to accomplish this, and it only requires four Josephson junction. Hence, a sharing of this resource is not that essential here. The resulting circuit is referred to as the control DfT section. The detailed scheme is shown in figure 8.

The front-end consists of two parts: first the DC-to-SFQ converter (left-top) and second a modified D-type flip-flop. The latter is basically capable of inhibiting the transport of any SFQ pulse from the original output of the adder slice under the control of signal con1 to the input of the next adder slice. This control input "con1" is normally the clock input for the flip-flop.

The last stage of the control DfT section is the previously discussed merger section. In combination with the D-type flip-flop it resembles the demultiplexer stage in the observability DfT section. The output of the merger section is connected to the input of the next adder stage, thereby controlling it via con1 and the bit generator. The total structure requires 13 Josephson junctions.

The combination of the previously proposed control and observability DfT circuits provide the possibility to have full access to any node in a superconductor circuit. It basically uses five standard circuits, being the converters, merger, splitter, and the D flip-flop. These are usually stored in the library of a superconductor design database anyway.
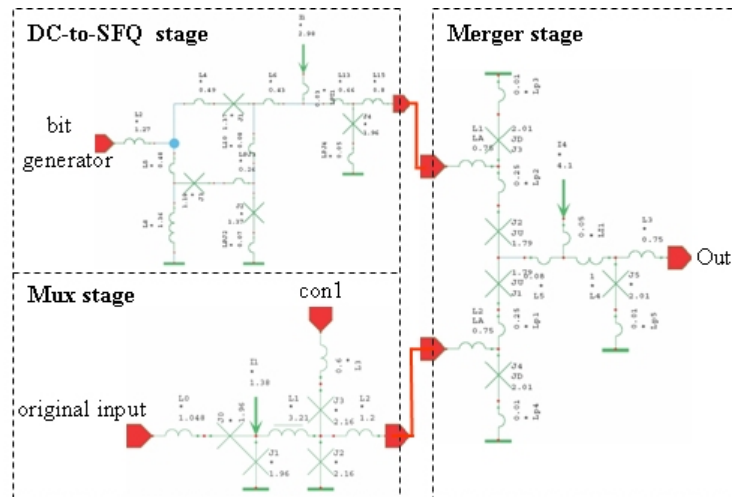


Figure 8: Detailed scheme of the controllability DfT structure, consisting of DC-to-SFQ pulse stage, the multiplexer to inhibit the original input, and the merger stage

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