Accessing On-Chip Temperature Health Monitors Using the IEEE 1687 Standard

Ghazanfar Ali, Ahmed Badawy, Hans G. Kerkhoff
Testable Design and Test of Integrated Systems Group
Centre of Telematics and Information Technology (CTIT)
University of Twente, Enschede, the Netherlands
{g.ali, h.g.kerkhoff}@utwente.nl

***Abstract*—The IEEE 1687 (IJTAG) is a newly IEEE approved standard to access embedded instruments. The usage of these embedded instruments (health monitors) is increasing in order to perform different online measurements for testing purposes as dependability is becoming a key concern in today's electronics. Aging and intermittent resistive faults (IRF) are two threats to a highly dependable system, and temperature can accelerate these two phenomena. In this paper, the work carried out for enabling online IJTAG control, observation and reconfiguration of the health monitors will be discussed. Three temperature monitors along with an IJTAG controller are used to demonstrate online temperature measurements using an IJTAG network interface. The simulation results show that the proposed (on-chip) methodology can reduce the dependency on the PC while observing the (static) embedded instruments in the field.**

Keywords—IJTAG, IEEE 1687 Standard, Embedded Instruments, Health Monitoring, Dependability

I. INTRODUCTION

As the technology advances in deep submicron following Moore's law, it enables the integration of millions of transistors on a single chip that besides increasing more functionality on-chip also leads to less dependable systems. One of the major dependability concerns in today's electronics is aging and no fault found (NFF) [1]. Aging induces significant delays in the circuits that causes eventually the system to fail [2]. In order to ensure reliable operations, several embedded instruments (health monitors) have been developed and presented in the literature for monitoring aging and NFF faults. Due to the increased integration level on chips, these health monitors are massively integrated on-chip. Temperature sensors, delay-sensors [3], built-in-self-test (BIST) engines [4] are some of the common examples of embedded health monitors. Temperature has proven to be one of the major parameters that can accelerate aging [5, 6] and has shown to enhance the probability of manifesting intermittent resistive faults (IRF) [7].

The IEEE 1149.1 standard (JTAG) is used to control, observe and reconfigure scan flip flops but recently the IEEE 1687 standard (IJTAG) seeks to optimize the access methods to embedded instruments [8, 9]. IJTAG uses the same TAP port previously used in JTAG to access scan flip flops. In order to use IJTAG compliant instruments, two different languages are being introduced by the IJTAG standard named instrument connectivity language (ICL) and procedural language (PDL). ICL is a hardware description language (HDL) for describing instrument interfaces, instrument test data registers (TDR) organization and the instrument network architecture. On the other hand PDL is based on the tool command language (TCL) that defines the procedures required to operate an embedded instrument [10].

In order to use health monitors (embedded instruments) online for the purpose of dependability, the current methodologies are more software-based where software running on a PC generates control signal (i.e. TMS) based on the ICL and PDL descriptions. This 'TMS' is used by the 'TAP controller' that generates further control signals (i.e. SelectEN, CaptureEn, ShiftEn etc.) to access the instruments. In this work, a dedicated architecture is proposed where the TMS-based control vectors (initially generated by software e.g. NEBOLA [9] on a PC during development time) are loaded into the TAP from a dedicated memory. In this way, one can accomplish the following advantages:

1. It will reduce the dependency on an external PC while observing the embedded instruments in-field.
2. The IJTAG network can use the same system clock as the instruments are using, which will reduce the effort to synchronize the different clock domains.
3. The proposed methodology will also help in reducing the overall test time as IJTAG is using the system clock.

The remainder of this paper will be organized as follows: in section II, the proposed methodology is explained. The details about the system-level architecture (case study) to observe online temperature health monitors are provided in section III. In section IV, simulation results are presented. Conclusions are provided in section V.

II. METHODOLOGY

The proposed system-level methodology is shown below in Figure 1. In order to reduce the dependency on a PC during online monitoring of the health monitors, as an external PC is essentially not available in normal infield applications, a dedicated memory-based approach to configure the IJTAG network is proposed in this work. 'TMS' and 'TDI' based vectors to configure the IJTAG-network and instruments are extracted from the waveform generation language (WGL) file that is generated by the software tool (e.g. NEBOLA) during the system level simulations. These extracted vectors are stored

978-1-5090-6113-6/16/$31.00 ©2016 IEEE

in a memory and executed using a simple finite state-machine (FSM).

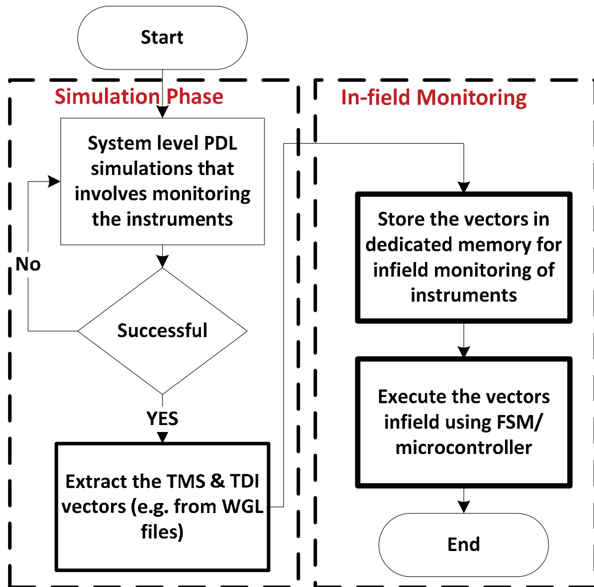

Figure 1: System level flow of the proposed methodology

III. System Level Architecture

The complete system level architecture of the case study is shown in Figure 2. The details with regard to the IJTAG Controller are discussed in subsection A. Instructions based on the control signal 'TMS' are stored in a dedicated memory inside the IJTAG Controller and applied directly to the TAP.

The example network consists of three instruments (Temperature Monitor-0, Temperature Monitor-1, Temperature Monitor-2) and three segment insertion bits (SIB). The instruments are interfaced to the scan path via shift-registers (TDRs) with parallel I/O. In this paper only a temperature monitor is used as an embedded instrument as temperature is an extremely important environmental parameter for aging and IRFs.

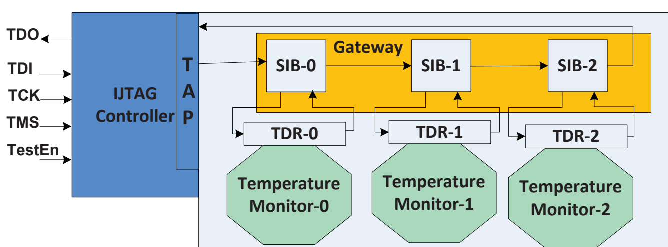

Figure 2: Complete system architecture

A. *The IJTAG Controller*

Figure 3 shows the detailed architecture of our IJTAG controller. It consists of three memory units "MEMORY-1", "MEMORY-2" and "MEMORY-3". The block "MEMORY-1" is used to store the response vectors from the instruments. In this case, these responses will be the temperature values which can be used by the operating system or task manager at a higher level to take appropriate actions. "MEMORY-2" is used to store the TDI-based vectors that are meant to be applied to the instrument. These vectors can configure the instrument in the desired mode of operation. "MEMORY-3" is used to store the TMS-based test vectors to configure the network (SIBs) in the desired mode of operation. Each memory bank contains a shift register to load the 'TDI' and 'TMS' signals serially into the network.

In order to make the proposed "IJTAG Controller" flexible, some multiplexers (MUXs) are introduced that can be controlled by the control logic to initialize 'ONchip' or 'OFFchip' instrument management. In the 'ONchip' mode, TMS and TDI based vectors are provided from the dedicated memory while in the 'OFFchip' mode, these vectors are supplied by the external software. These modes are initialized by a newly introduced signal 'TestEn'. This 'TestEn' control can come from an external PC (using a dedicated pin) or it can also be implemented in the form of control logic within the IJTAG Controller to reduce pin-overhead. The proposed architecture can also be enhanced to deal with synchronization issues between 'ONchip' and 'OFFchip' modes.

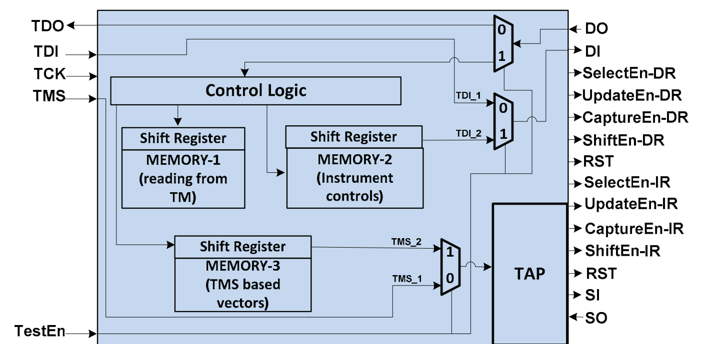

Figure 3: IJTAG Controller Architecture

B. *Segment Insertion Bits (SIB)*

A SIB can be thought of a bypass register as it allows the overall scan chain to be of variable length by enabling or disabling certain parts of the scan chain. As shown in Figure 2, when SIB-0 is 'OPEN' it will enable the access to TDR-0 and when it is 'CLOSED' it will disable this access. There are several different SIB implementations as presented in IJTAG standard description [8]. In this case study a "SIB with multiplexer *after* scan chain (SIB_mux_post)" design has been implemented as shown below in Figure 4.

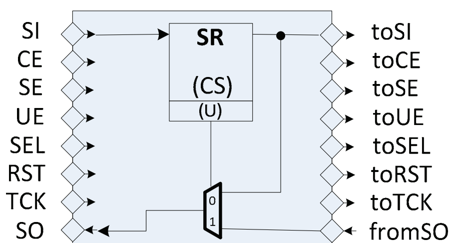

Figure 4: SIB with post MUX

C. Temperature Health Monitor (TM)

The temperature monitor used is based on a Wheatstone bridge. The design uses two types of resistances, one with a high temperature coefficient (Tc2, Tc3) and the other with low coefficient (Tc1, Tc4). As the temperature increases, the bridge resistances will increase but not with the same amount. This will lead to an almost linear output differential voltage V(ΔT) proportional to the temperature increase ΔT:

$$V(\Delta T) = \frac{1 + \Delta T * Tc2}{2 + \Delta T * Tc1 + \Delta T * Tc2} + \frac{1 + \Delta T * Tc4}{2 + \Delta T * Tc3 + \Delta T * Tc4}$$

This voltage is amplified with a carefully designed linear amplifier and then applied to an anti-alias filter. The filter output is converted to a 10-bits digital word using a "Successive Approximation ADC". The ADC requires 11 clock cycles for every word (1-cycle for sampling and 10-cycles for convergence). The monitor is controlled by a master enable-bit which is responsible for enabling of all the monitor sub-blocks (Amplifier, Filter and ADC).

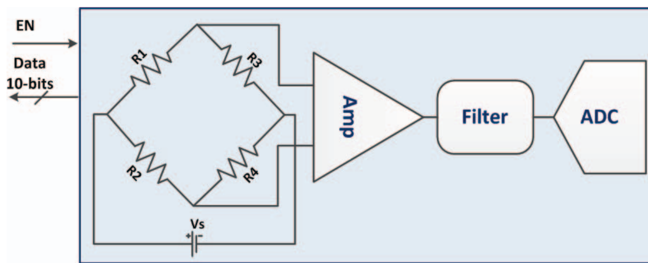

Figure 5: Temperature Health Monitor Set-Up

IV. Simulation Results

The simulation results of the "Temperature Health Monitor (TM)" are presented in Figure 6 using Cadence Virtuoso. It can be seen that when the enable signal 'EN' goes 'HIGH', it turns 'ON' the 'TM' and its output (10-bit word) stabilizes after 11-clock cycles. When the 'EN' control signal is 'LOW', 'TM' is turned 'OFF'. In order to functionally evaluate the complete system, we use this behavior of the 'TM' and performed a system-level simulation using 'ModelSim' software. The system-level functional simulation results are presented in Figure 7. It shows the access, enable and read operations of Temperature-Monitor-0 (TM0). 'TMS_2' and 'TDI_2' signals are applied from the memory units (TestEn=1) to configure the IJTAG network as discussed earlier in Figure 2.

Important events are highlighted as 'a', 'b', 'c', 'd', 'e' and 'f' in Figure 7. We'll now analyze the sequence of these events. First, SIB-0 is configured by loading '001' into the TDI (**a**) and then the control signal 'Enable' is loaded into TDR-0 (as can be seen in the shift part 'SCN') (**b**). The loaded control signals are then applied to TM0 (**c**). After some delay, the temperature reading is available at the output of TM0 (**d**). Subsequently the temperature reading from TM0 is captured into the scan part of TDR-0 and shifted out (**e**). Finally the temperature reading can be seen at the TDO port (in this case it is 1111001111) (**f**).

In the current case study, a 79-bit long TMS-based vector is stored in the memory to activate and read the value from temperature sensor. The memory required to store the TMS-based vectors to access and read each instrument can be estimated by using the following relationship, where 'TAP_{bits}' are the bits required to configure 'TAP' in different states. The 'SIB_{bits}' are the bits required to configure SIBs in open or close state. The 'TDR_{bits}' are actually the instrument interface bits required to configure the instruments in desired mode of operation. From the following relationship, it is expected that the memory required to store the TMS and TDI based vectors will increase linearly with the increase in the instruments.

$$Vector_{length} = TAP_{bits} + SIB_{bits} + TDR_{bits}$$

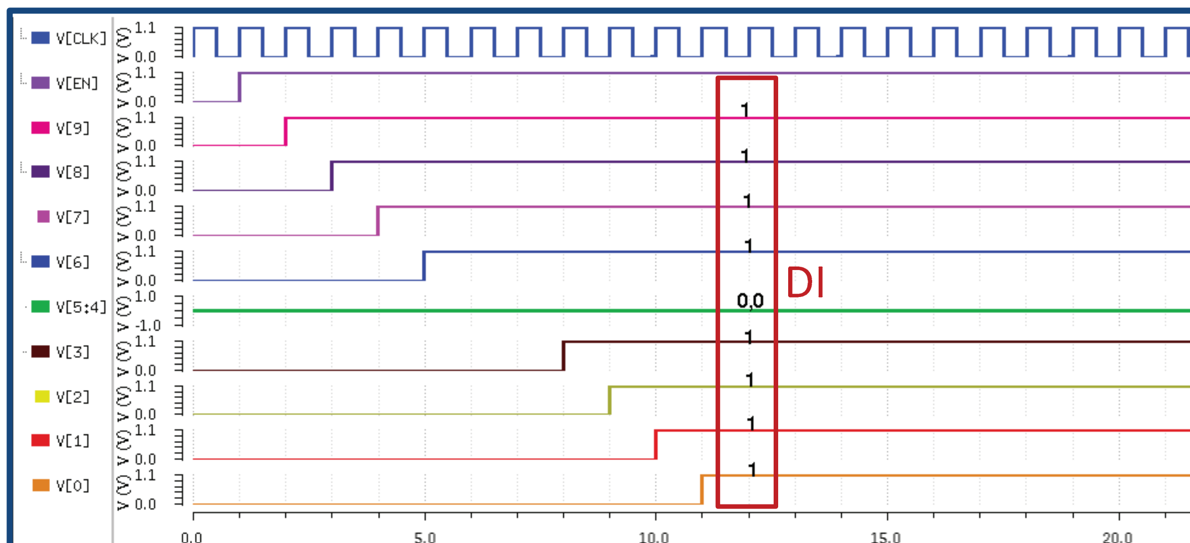

Figure 6: Functional simulation of the temperature health monitor (V[0]-V[9] is 10-bit output)

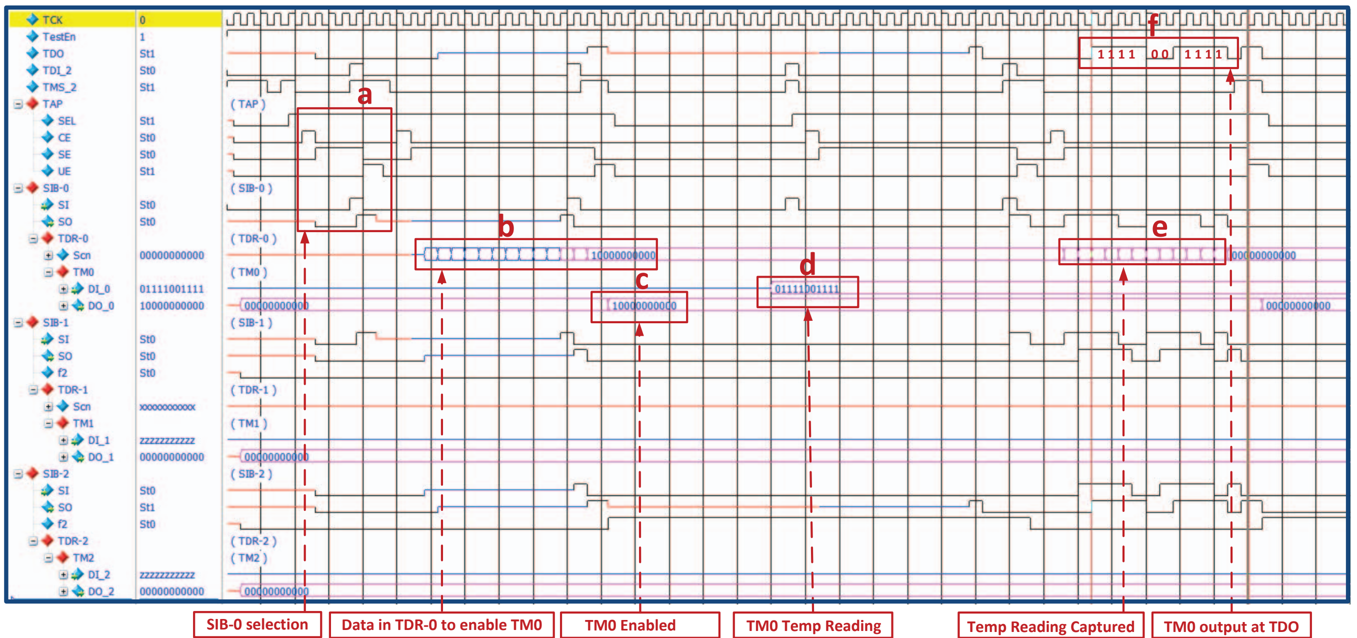

Figure 7: Functional simulation of the system for Temperature Monitor 0 (TM0)

V. Conclusion

After a brief introduction of the IEEE 1687 standard, next a complete system-level architecture has been presented with details on the proposed "IJTAG Controller" architecture for the online management of temperature health monitors. The proposed IJTAG Controller architecture loads TMS and TDI based vectors from the on-chip memory that reduces the dependency on a PC while observing the embedded instruments in the field. Simulation results shows that the proposed technique can be used to manage/control instruments in the field which is crucial to ensure the reliable operation of the chip over life time. The proposed methodology can also reduce the overall test-time as there is no off-chip interface present therefore system clock can be used instead of the test clock. The current architecture can also be useful to deal with static instruments (e.g. temperature monitor, slack monitor, Iddx monitor etc.) where no back-and-forth communication between controller and instrument is needed.

VI. Acknowledgements

This research was partly carried out within the FP7 BASTION project and Horizon 2020 project IMMORTAL, financed by the European Committee (EC) and the Netherlands Enterprise Agency (RVO).

References

[1] J. Wan and H. G. Kerkhoff, "The influence of No Fault Found in analogue CMOS circuits," in *International Mixed-Signals, Sensors and Systems Test Workshop (IMS3TW),* pp. 1-6, 2014.

[2] M. H. Sulieman, "Threshold-voltage variations effects on the reliability of nano-scale CMOS logic gates," in *IEEE Conference on Nanotechnology IEEE-NANO,* pp. 744-747, 2009.

[3] K. Tae-Hyoung, R. Persaud, and C. H. Kim, "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," in *IEEE Journal of Solid-State Circuits,* vol. 43, pp. 874-880, 2008.

[4] P. R. Savanur, P. Alladi, and S. Tragoudas, "A BIST approach for counterfeit circuit detection based on NBTI degradation," in *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFTS),* pp. 123-126, 2015.

[5] W. Wang, S. Yang, S. Bhardwaj *et al.*, "The Impact of NBTI Effect on Combinational Circuit: Modeling, Simulation, and Analysis," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 18, pp. 173-183, 2010.

[6] A. Bravaix, C. Guerin, V. Huard *et al.*, "Hot-carrier acceleration factors for low power management in DC-AC stressed 40nm NMOS node at high temperature," in *IEEE International Reliability Physics Symposium,* pp. 531-548, 2009.

[7] H. G. Kerkhoff and H. Ebrahimi, "Intermittent Resistive Faults in Digital CMOS Circuits," in *IEEE International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS),* pp. 211-216, 2015.

[8] "IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device," *IEEE Std 1687-2014,* pp. 1-283, 2014.

[9] A. Ibrahim and H. G. Kerkhoff, "iJTAG integration of complex digital embedded instruments," in *International Design & Test Symposium (IDT),* pp. 18-23, 2014.

[10] A. Jutman, S. Devadze, and K. Shibin, "Effective Scalable IEEE 1687 Instrumentation Network for Fault Management," in *IEEE Design & Test,* vol. 30, pp. 26-35, 2013.