# **Electronic Conduction Processes in** SiO<sub>2</sub> Films Obtained by ECR PECVD

Gratiela Isai, Jisk Holleman, Pierre Woerlee, Hans Wallinga

MESA<sup>+</sup> Research Institute, University of Twente P.O. Box 217, 7500 AE Enschede, The Netherlands. Phone: +31 (0)53 4894394 Fax: +31 (0)53 4891034 *E-mail:* G.I.Isai@el.utwente.nl

Abstract - Low temperature dielectrics are desired for realising thin-film-transistors on glass or plastic substrates. In the past silicon dioxide layers with stoichiometric composition and good electrical properties were deposited without substrate heating with an Electron Cyclotron Resonance Plasma source. This work is focused on determining the conduction mechanisms in the deposited films. The temperature dependence of the current density electric field characteristics were studied and Fowler-Nordheim was found to be the dominant conduction mechanism in SiO<sub>2</sub> films deposited with low silane flow and at low pressure. For higher silane flows and higher pressures, the current travels via traps in the oxide bandgap. Constant current stress measurements confirmed that low silane flow (5 sccm) and low pressure (4 mTorr) are ideal deposition conditions. For aluminium-gate capacitors with SiO<sub>2</sub> deposited at optimised parameters, a charge to breakdown of 1 C/cm<sup>2</sup> was found, comparable with the values obtained for thermally grown oxide.

*Keywords*: silicon oxide, PECVD, Fowler-Nordheim, Qbd,

### I. INTRODUCTION

The demand for high mobility TFTs realised on temperature unstable substrates is increasing [1]. These devices require thin, low-temperature, high-quality gate dielectrics. It is known however, that a low deposition temperature degrades the films properties. In this work, we compare the electrical properties of  $SiO_2$  layers deposited at room temperature with the ones of thermally grown oxide obtained at 950°C.

Multipolar ECR plasma enhanced deposition [2] was chosen for our research because it is a low process pressure, with low electron and ion energy [3], and high electronic density [4]. Because of the ECR plasmas characteristics ("soft" and "dense") [5] we believe that the deposition temperature can be lowered, without degrading the film quality. Previous results [6] have shown that ECR PECVD can deliver high-quality SiO<sub>2</sub>, without substrate heating, at low SiH<sub>4</sub> flow rate and low deposition pressure. In this work, we continued the electrical characterisation of the SiO<sub>2</sub> films, focusing on their electrical conduction mechanism and their oxide integrity.

#### II. EXPERIMENTAL

The deposition system consisting of a microwave plasma disk reactor (MPDR-300) has been described elsewhere [7]. Electronic pure  $N_2O$  and 2% SiH<sub>4</sub> diluted in helium were used as the gas precursors.  $N_2O$  was introduced in the quartz dome and silane was injected through a gas ring downstream of the plasma.

The SiO<sub>2</sub> films were deposited at floating temperature, without external heating. Due to the heating caused by plasma, the temperature of the substrate was around 60°C. During the experiments, the flow rate of N<sub>2</sub>O was maintained at a constant value of 20 sccm and the microwave power was adjusted at 400 Watts. The total pressure was in the range of 4-20 mTorr and the flow rate of 2% SiH<sub>4</sub>-in-helium varied between 5 and 15 sccm. Silicon oxide films with thickness of 40-70 nm were deposited.

3-inch (100)-oriented n-type Si wafers having a resistivity of 1-10  $\Omega$ -cm were used for the experiments. The wafer preparation included a standard cleaning procedure [8] followed by a 1% HF etch in order to remove the native oxide. Post-deposition anneal (PDA) in a wet N<sub>2</sub> ambient (N<sub>2</sub> bubbled through DI water at room temperature) has been performed for 60 minutes, at a temperature of 500°C, for all the films.

MOS capacitors with aluminium gate electrodes were manufactured in order to measure the electrical properties of the SiO<sub>2</sub> layers. All samples were subjected to post-metallisation annealing (PMA) for 5 minutes, at  $400^{\circ}$ C in wet N<sub>2</sub> ambient. The CV and IV curves were obtained with an MDC system and an HP 4156. Constant current stress measurements were made with an HP 4156, in order to calculate the charge-to-breakdown.

### **III. EXPERIMENTAL RESULTS AND DISCUSSIONS**

### A. Conduction mechanism

In the past [6], it has been observed that the leakage current of the deposited  $SiO_2$  layers rises with increasing the deposition pressure or the  $SiH_4$  flow rate, while keeping the other deposition parameters constant (figure 1 and figure 2).



Fig. 1 Current density versus electric field for films deposited with 5 sccm  $SiH_4$ /He and 20 sccm  $N_2O$ , at 400 Watts and different pressure.



**Fig. 2** Current density versus electric field for films deposited with 20 sccm  $N_2O$ , at 400 Watts, 12 mTorr and different silane flow.

The shape of the current density-electric field (J-E) curves presented in figure 1 and figure 2 varied

considerably with modifying the deposition parameters. In order to get more insight in the electrical behaviour of the deposited films, the mechanisms of electrical transport in the silicon oxide were investigated.



**Fig. 3** Current density versus electric field for a film deposited with 5 sccm  $SiH_4$ /He and 20 sccm  $N_2O$ , at 400 Watts and 4 mTorr; theoretical hopping current and Fowler-Nordheim current.

Figure 3 presents the current density, which passes through the sample deposited at the lowest pressure (4 mTorr), versus the electric field. The film is characterised by a low leakage current, high resistivity and high critical field. As one can see, the graphic can be divided in two regions. For electric fields lower than 6 MV/cm, the current corresponds to the electronic hopping conduction process [9]. It can be written as:

$$J_{hopping}(E) = C_1 E \exp(-\frac{q\phi_a}{kT})$$
(1)

where  $J_{hop}$  is the current density, *E* is the electric field, *q* is the electron charge, *k* is the Boltzmann constant, *T* the temperature expressed in Kelvin,  $\phi_a$  the thermal activation energy and  $C_1$  is a constant,. The current is caused by thermally excited electrons, which jump from one isolated state to another.

From electric fields higher than 6 MV/cm, the main conduction mechanism is Fowler-Nordheim tunnelling [10]. The current density for this case is given by:

$$J_{FN} = \frac{q^2 m_0}{8\pi \cdot k\phi \cdot m_e} E^2 \exp\left[-8\pi \cdot \frac{(2m_0 q\phi)^{1/2}}{3hE}\right]$$
(2)

where *h* is Planck's constant,  $m_0$  the free electron mass,  $m_e (= 0.44m_0)$  [11] the effective mass of an electron in silicon and  $\phi$  is the barrier height for electrons in silicon. To confirm our hypothesis, the Fowler-Nordheim plot was drawn (figure 4), in which  $\ln (J/E^2)$  was represented as a function of 1/E. The experimental data can be fitted with a straight line and from its slope the value of  $\phi$  was calculated as 3.11 V. Similar value is used for modelling the current in thermally grown oxide [12].



**Fig. 4** Fowler-Nordheim plot for a film deposited with 5 sccm  $SiH_4/He$  and 20 sccm  $N_2O$ , at 400 Watts and 4 mTorr.

Moreover, the extremely weak dependence of current on temperature (figure 5), for electric fields higher than 6 MV/cm, verified that Fowler-Nordheim tunnelling was correct identified as the major conduction mechanism in the oxide layer.



**Fig. 5** Current density versus electric field for a film deposited with 5 sccm  $SiH_4$ /He and 20 sccm  $N_2O$ , at 400 Watts and 4 mTorr measured at different substrate temperatures.

Next, the behaviour of an oxide deposited at a higher  $SiH_4$  flow with higher leakage current was studied at different temperatures (figure 6). The current that flows through the structure depends highly on temperature at low biases, while it is almost independent of temperature at electric fields higher than 8MV/cm. In addition, the

current reaches a regime, at fields around 4 MV/cm, where the current increases very slowly with the applied voltage. The "quasi-saturation" of the current may be caused by the charge trapping [13]. Consequently, an internal electric field is created, which is opposed to the external electric field, limiting the carriers flow [14].



**Fig. 6** *Current density versus electric field for a film deposited with 12.5 sccm SiH*<sub>4</sub>/He and 20 sccm  $N_2O$ , at 400 Watts and 12 mTorr measured at different temperatures.

In the first region before the saturation occurs, the current can be fitted with a Poole-Frenkel current [15], whose expression is:

$$J_{PF} = C_2 E \exp(\frac{-q\phi_T}{kT}) \exp\left[\frac{E^{1/2}}{rkT}\sqrt{\frac{q^3}{\pi\varepsilon_0\varepsilon_R}}\right] \quad (3)$$

where  $\phi_T$  denotes the barrier height of the trap,  $\varepsilon_R$  is the dielectric constant of the SiO<sub>2</sub> and C<sub>2</sub> is a constant. The Poole Frenkel effect is the thermal emission of charge carriers from Coulombic traps, enhanced by the trap barrier lowering due to the electric field applied [16]. Because of its high dependence on temperature, the Poole-Frenkel current was found to fit the measurements.



Fig. 7 Two consecutive measurements of current density versus electric field for the same capacitor made with a film

# deposited with 10 sccm SiH<sub>4</sub>/He and 20 sccm $N_2O$ , at 400 Watts and 12 mTorr.

To verify the trap-charging hypothesis, we measured the current until 8.5 MV/m, and then remeasured the capacitor's current (figure 7). The current is lower for the second measurement, as expected. The traps have captured carriers and therefore cannot assist the conduction process [17].



Fig. 8 Current density versus electric field for a film deposited with 10 sccm SiH<sub>4</sub>/He and 20 sccm  $N_2O$ , at 400 Watts and 12 mTorr, measured at 22°C; fitting theoretical current as a sum of Poole-Frenkel current and Fowler-Nordheim current.

The current measured after electrical stressing the sample can be written as a sum of Poole-Frenkel current and Fowler-Nordheim tunnelling current (figure 8).

$$J = J_{Poole-Frenkel} + J_{Fowler-Nordheim}$$
(4)

Poole-Frenkel effect dominates conduction at low voltages, while Fowler-Nordheim tunnelling appears at high voltages, where the temperature has no significant effect upon the current. Figure 9 shows the remeasured current through the oxide, plotted as a continuous line, and the theoretical current written as a sum of Poole-Frenkel current and Fowler-Nordheim current for four different temperatures: 8°C, 22°C, 62°C and 102°C, plotted as a dotted line. As one can see, there is a good fitting for all the temperatures.

The same conduction processes were found in all the films deposited at high pressure and high silane flow. Moreover, the leakage current for low electric fields increased with both silane flow and total pressure, indicating an increase of trap density. It is believed that the traps are a result of silicon dangling bonds in the case of oxides deposited at high silane flow [18]. For higher deposition pressure, the efficiency of energy transfer from the plasma toward the depositing film is lower. Consequently, there is less energy for particles to migrate on the film surface and for creation of strong chemical bonds; therefore, the probability of creating defects in the film is increased [19].



**Fig. 9** Current density versus electric field for a film deposited with 7.5 sccm SiH<sub>4</sub>/He and 20 sccm N<sub>2</sub>O, at 400 Watts and 12 mTorr measured at 8°C, 22°C, 62°C and 102°C, plotted with a continuous line; fitting theoretical current as a sum of Poole-Frenkel current at different temperature and Fowler-Nordheim current, plotted with dotted line.

In summary, it has been observed that ECR plasma enhanced deposition at pressures lower than 10 mTorr can provide silicon oxide layers with a Fowler-Nordheim tunnelling conduction mechanism, the same as in thermally grown oxide. With increasing either the pressure, or the silane flow, the conduction mechanism in the layer is modified, becoming a trap-related mechanism. It has been established that leaky films, which resulted from depositions with a silane flow bigger than 5 sccm and pressures higher than 6 mTorr, exhibit all the same type of conduction. The current can be written as a sum of Poole-Frenkel current and Fowler-Nordheim current.

## B. Oxide integrity

The oxide integrity was tested for further understanding of the deposited films performance. In picture 10, the Weibull plot for 4 different oxides and for thermally grown oxide was presented. Each curve is the result of 50 measurements, realised on Al-gate capacitors with an area of 0.01 mm<sup>2</sup>. A constant current of  $5 \cdot 10^{-3}$  A/cm<sup>2</sup> was forced through the oxide by applying positive voltage on the gate. Electrons were injected from the substrate.



**Fig. 10** Weibull plot for films deposited with 5 sccm  $SiH_4$ /He and 20 sccm  $N_2O$ , at 400 Watts and different pressure and for a thermally grown oxide.

It is noticeable that the films deposited at lower pressure (4 and 6 mTorr) have high values for the charge-to-breakdown (around 1C/cm<sup>2</sup>) and only a few structures experienced extrinsic breakdown. The Weibull plot for the oxide deposited at 4 mTorr is similar with the one for the 25 nm reference silicon oxide film grown at 950°C.

On the contrary, the Weibull plot for layers deposited at higher pressure featured a smaller charge-tobreakdown and a larger extrinsic distribution. This indicates a higher density of defects in the bulk of dielectrics deposited at higher pressure. It is confirmed once again that multipolar ECR plasma is an efficient deposition system for very low pressures.

The effect of silane flow rate upon the oxide integrity was studied next (figure 11). Low values for the chargeto-breakdown and large distributions of defect-related breakdowns can be observed for the films deposited with high silane flow. A possible cause for the oxide reliability degradation is the increased number of silicon unsaturated bonds.



**Fig. 11** Weibull plot for films deposited with 20 sccm N<sub>2</sub>O, at 400 Watts and 12 mTorr and for a thermally grown oxide.

While stressing the dielectrics with a constant current, the voltage increases. A higher voltage is required to sustain the same current through the material, since an electric field opposed to the one applied, is built-in by the charges trapped in the oxide. The voltage variation can be related to the trap density in the oxide bandgap. For the reference sample the voltage increased for about 4 volts during stressing, while for the best ECR oxide it increased only with 2 volts. This illustrates the similarity between the thermal grown oxide and the low deposition pressure film. The experiments presented in this section demonstrate that oxides with good reliability can be deposited at room temperature.

### IV. CONCLUSIONS

We have identified the main conduction mechanisms in the ECR PECVD silicon oxide films. For the films with higher critical field, obtained at lower pressure and lower silane flow, the conduction mechanism detected was Fowler-Nordheim tunnelling. For films deposited at higher flows or higher total pressures, the conduction mechanism is trap related. The leakage current increases increasing this two deposition parameters, with indicating a higher trap density. The IV characteristics are transient, the current after stressing can be written as a sum of Poole-Frenkel and Fowler-Nordheim current, for different temperatures. The constant current stress measurements showed that decreasing the silane flow and pressure could improve the oxide integrity. The best films have charge-to-breakdown values comparable to the ones for thermally grown oxide.

### V. ACKNOWLEDGEMENTS

This project is financially supported by FOM.

We wish to thank E. H. J. Ruiter, A. A. I. Aarnik, P. W. C. Linders, G. Boom, A. Kooy, S. W. Kruger, H. van Vossen, Samantha, Marion of the MESA+ Clean Room for general technical support; H. de Vries and M. H. H. Weusthof of the MESA+ Test Centre for their help with the measurements.

### VI. REFERENCES

- S. Uchikoga, N. Ibaraki Thin Solid Films; Vol. 383 (2001), pp. 19-24.
- [2] K. T. Sung and S. W. Pang, J. Vac. Sci. Technol.; 10 (1992), pp. 2211-16.
- [3] M. C. Hugon, F. Helmonte, B. Agius, J. L. Courant J. Vac. Sci. Technol. A; 15 (1997), pp. 3143-3153.
- [4] N. Jiang, B. Agius, M. C. Hugon, J. Olivier, M. Puech J. Appl. Phys.; 76 (1994), pp.1847-1855.
- [5] S. Garcia, I. Martil, G. Gonzalez Diaz, E. Castan, S. Duenas, M. Fernandez J. Appl. Phys.;83 (1998), pp. 332-338.
- [6] G. Isai, A. Kovalgin, J. Holleman, P. Woerlee, H. Wallinga Thin film transistor technologies V, Electrochemical Society Proceedings Volume 2000-31; (2001) pp.169-175.
- [7] G. Isai, A. Kovalgin, J. Holleman, P. Woerlee, H. Wallinga J. Phys. IV; 11 (2001) pp.747-753.
- [8] A. Y. Kovalgin, G. I. Isai, R. Dekker, J. Holleman, P.H. Woerlee, H. Wallinga – SAFE99, The Netherlands, 24-25 November 1999, pp. 239-246, ISBN 90-73461-18-9.
- [9] C. Chaneliere, J. L. Autran, R. A. B. Devine J. Appl. Phys.;86 (1999), pp.480-486.
- [10] E. Kameda, T. Matsuda, Y. Emura, T. Ohzone Solid-St. Electron.; 42 (1998), pp.2105-2111.
- [11] M. Depas, B. Vermeire, P. W. Mertens, R. L. Van Meirhaenghe, M. Heyns – Solid-St. Electron.; 38 (1995), pp.1465-1472.
- [12] V. Houtsma Gate oxide Reliability of Poly-Si and Poly-SiGe CMOS devices, pp. 23.
- [13] V. S. Lysenko, I. P. Tyagulski, Y. V. Gomeniuk, I. N. Osiyuk – Microelectronics reliability; 40 (2000), pp. 799-802.
- [14] B. L. Yang, H. Wong, Y. C. Cheng Solid-St. Electron.; 37 (1994), pp.481-486.
- [15] W. R. Harrell, J. Frey Thin solid films; 352 (1999), pp.195-204.
- [16] J. R. Yeargan, H. L. Taylor J. Appl. Phys.; 39 (1968), pp.5600-5604.
- [17] H. Krause Phys. Stat. Sol (A); 52 (1979), No. 8, pp.565-575.
- [18] A. Yokozawa, Y. Miyamoto. Applied Physics Letters; Vol. 73 (1998), No. 8, pp. 1122-1124.