Fast Thermal Cycling Stress and Degradation in Multilayer Interconnects

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Abstract- **The thermal cycling stress method is popularly used to study the thermal mechanical effect on metallization films in VLSI applications, specially in interconnect systems of power IC. The fast thermal cycling stress method reported in this paper has several advantages compared with using a conventional oven for thermal stress. A special test chip is designed to demonstrate the application of this method. A diode in the test chip plays a part as temperature sensor. The diode thermal coefficient is determined to be 1.8mV/^{O}C. The first experiment of temperature cycling stress is done with temperature ranging to be from 46 to 286°C (ΔT of 240°C). The failure analysis is done by SEM equipment with Backscatter Electron (BSE) detector. The results show the mechanism observed that the failure mechanism is quite similar with temperature cycling stress using a conventional oven.**

Keywords- **Thermal cycling; multilayer interconnects; chip temperature measurement**; **SEM**; **BSE**

I. INTRODUCTION

In recent years, increasing failure rates during temperature cycling are noted due to the increased power specifications. Temperature cycling is one of the main factors that create stress cracking in passivation and metal layers [1]. The mechanism of fatigue failure is mainly due to mechanical stress caused by temperature cycling [2]. However, a very fast thermal transients experiment to mimic temperature cycling of operational conditions cannot be carried out using an oven. The test condition in an oven is far from the real operation of power ICs, which work at very high frequency. This paper presents a method to study fast temperature cycling without using an oven. It is useful to study interconnect systems for power ICs under more realistic to temperature cycling conditions. The exact temperature in the chip can be measured by using a diode as temperature sensor. Otherwise, it can be used to study the combination of temperature cycling with electromigration. The fast thermal cycling can be used as accelerated factor in electromigration experiments. A special test structure will be introduced to demonstrate the study method. The details of the experimental set-up using this structure will be presented. Finally, the first results of fast temperature cycling will be shown. SEM verifications showed that the failure and degradation of multilevel interconnects system caused by extrusion and voiding.

II. EXPERIMETAL TECHNIQUE AND RESULTS

A. Description of the Test Chip

The test structure is briefly showed in figure 1. There is a very large 4Ω poly-silicon resistor just below the die surface where a very long meandering metal level 1 (M1) is located. This resistor can be used to generate a high temperature transient. This temperature can be measured with an integrated diode in the middle of the resistor. Extrusion monitors in M1, between the meandering line, and in metal level 2 (M2), large plate above the whole structure, allow detection of short circuit due to extrusion cause by thermal transients or electromigration. A part of the very long meandering M1 resistor (about 14Ω) can be used for electromigration testing. In this paper we only study the effect of temperature. No current is applied so electromigration dose not take place. The module is encapsulated in a 17 pins power package.

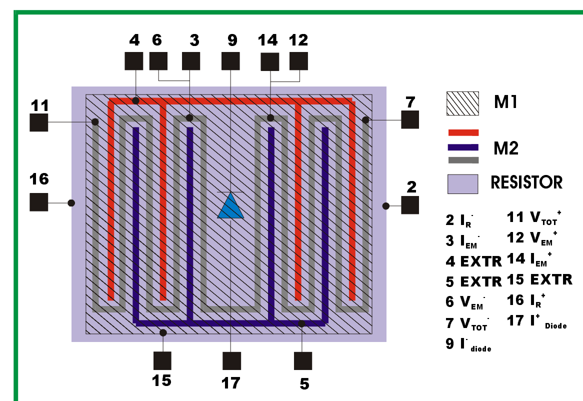


Fig. 1. *Test chip with specific connections.*

B. Experiment Set-up

To carry out the fast temperature cycling with test chip as described above we engaged the experiment set-up as shown in figure 2. The resistor is connected to pulse current source to generate temperature peaks. This pulse current source can change amplitude, I_{max} and duty cycle, D. The diode is connected to a DC current source to force the DC current to the diode. A digitalizing oscilloscope is also connected to diode to monitor the change of diode voltage due to change of temperature.

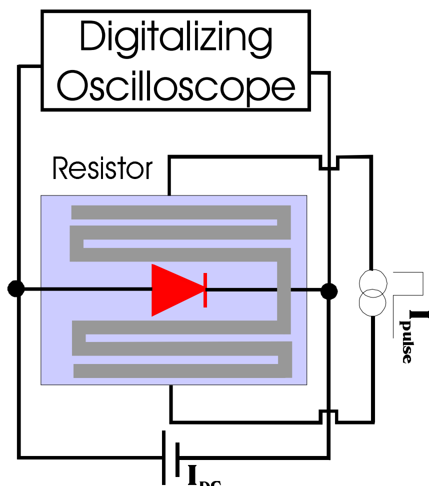


Fig. 2. The scheme to force pulse power for heating-up the chip and to monitor temperature cycling.

C. Measurement of Test Chip

- Diode as Temperature Sensing

This method is based on Shockley's relation for the current, I, versus forward voltage, V, characteristics of an ideal diode. Here is only briefly introduced and details can be found in [3]. The relation is of form:

$$I = I_s\{e^{\left(\frac{qV}{kT}\right)} - 1\} \tag{1}$$

Where, q is the elementary electron charge, k is the Boltzman's constant, T is the absolute temperature, and I_s is the reverse saturation current. I_s is temperature dependent and can be expressed as:

$$I_s \cong KT^r e^{\left(\frac{-E_g}{kT}\right)} \tag{2}$$

Where, K, r, and E_g are independent of temperature. E_g is energy gap.

In the forward direction $I >> I_s$, equation (1) can be written as

$$I = I_s e^{\left(\frac{qV}{kT}\right)} \tag{3}$$

Most real diodes follow these relations approximately over a limited range of current and experimental results are the best represented by empirical form [3]

$$I = I_s e^{\left(\frac{qV}{nkT}\right)} \tag{4}$$

Assumption that the diffusion current dominates, we will take the value of n to be 1.

Equation (3) can be combined with equation (2) to get a relation in term of forward voltage, V as

$$V = \frac{E_g}{q} + \frac{kT}{q}(\ln I - \ln K - r\ln T) \tag{5}$$

This relation shows that at constant current, the forward voltage drop is almost a linear function of temperature. For most practical purposes this relation can be expressed as

$$T = A + BV \tag{6}$$

The constants A, and B are determined by using isothermal calibration. The B value will be called diode thermal coefficient, α_D.

The chip peak temperature is can be determined by the equation below:

$$T = T_{amb} + \Delta V / \alpha_D \tag{7}$$

Where ΔV is difference of diode voltage from ambient (room) temperature, $\Delta V = V_T - V_{amb}$, and T_{amb} is ambient temperature.

The average temperature of chip during temperature cycling is usually calculated by equation below [4].

$$T_{avg} = T_{amb} + R_{th} * P_{avg} = T_{amb} + R_{th} * D * P \tag{8}$$

Where, R_{th} is thermal resistance, P is pulse power, and D is duty cycle.

- Experiment To Determine Diode Thermal Coefficient

The characteristics of diode in our test chip used in this study, is show in figure 3.

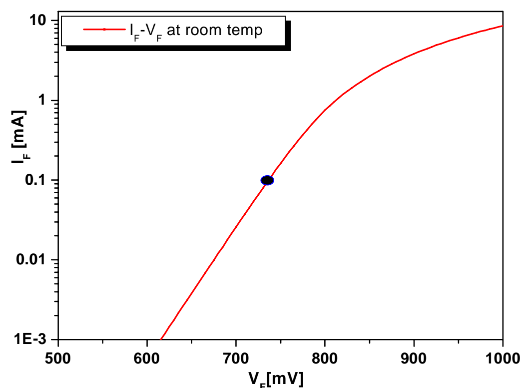


Fig. 3. Current versus voltage characteristics obtained from the temperature sensing diode in the thermal test chip.

The data shows that this diode essentially follows the current versus forward voltage relation in equations over arrange current of about 0.01 to 0.5mA. Hence for temperature sensing, this diode must be operated within this range current range. In this study, we selected the

current at 0.1mA. To calculate the diode thermal coefficient, the temperature and diode voltages are sequentially measured at a constant current of 0.1mA during the isothermal step by using a oven. These measurements are done using a computer controlled data acquisition system. The results are shown in figure 4 for different isothermal step. The time of an each isothermal step of 1 hour is long enough to stable temperature. It thanks to the very high temperature stability of equipment (about 0.02°C), the diode voltage and temperature measured are almost stable. To find the diode thermal coefficient we take the average value of diode voltage and temperature at each isothermal step. They are fitted using the least squares linear fit. The result is shown in figure 5.

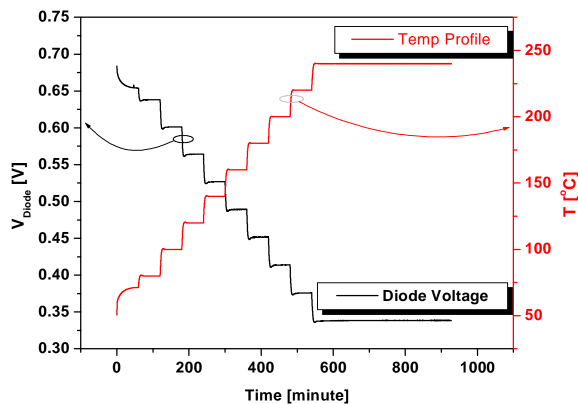


Fig. 4. *Temperature steps and diode voltages are sequentially measured.*

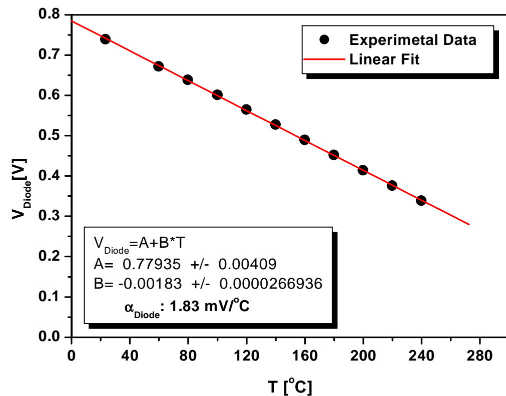


Fig.5. *Calibration data for the diode (at 0.1 mA current) fitted to a linear curve.*

The diode thermal coefficient obtained to be 1.83mV/°C. The approximation of linear fit is good enough, because the standard deviation is only about 0.006mV/°C.

-Thermal Resistance Measurement

Equation (8) shows that in order to calculate the average temperature, we need to know the thermal resistance. Normally, the thermal resistance is calculated by equation below [4]

$$R_{th} = \frac{\Delta T}{P} \tag{9}$$

Where P is power, R_{th} is thermal resistance, and ΔT is a difference of temperature comparing with ambient temperature. The thermal resistance of our chip is calculated as follows. The different powers are applied on the resistor, and each power induced a different ΔT. After applying the power, we waited for 1/2 hour, and then measured the voltage of diode by applying a current 100μA. From the change of diode voltage comparing with ambient temperature, the ΔT is calculated basing on equation (8). The data of ΔT and power P are fitted using the least squares linear fit to find R_{th}. The results are showed in figure 6.

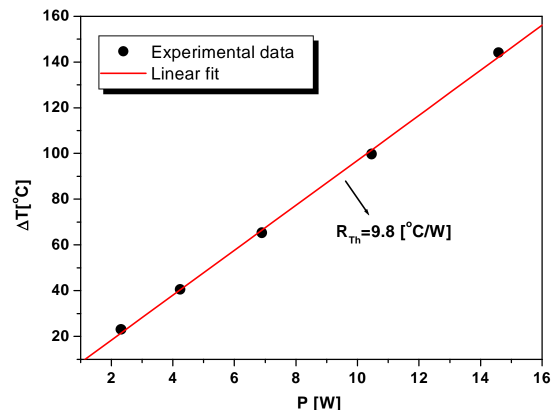


Fig. 6. *The curve fit to find the thermal resistance R_{th}*

D. Fast Temperature Cycling Experiments and Results

- Experimental Details

The experimental set-up as shown in figure 3 is used to carry out temperature cycling stress with ΔT, period, and duty cycle to be respective 240°C, 100ms, and 10%. Figure 7 shows the diode voltages waveform and resistor voltage waveform (from 4Ω resistor to heat up the chip) by using the digitalizing oscilloscope. The peak temperatures (T_{max}, T_{min}), and average temperature, T_{avg} are calculated from diode voltage which are shown in table I.

TABLE I

T_{min} [°C]	T_{max}[°C]	ΔT[°C]	T_{avg}[°C]
46	286	240	77

The transient temperature profile and power pulse are calculated from diode voltage waveform and resistor voltage waveform (4Ω poly-silicon resistor to heat up the chip) as qualitatively shown in figure 8.

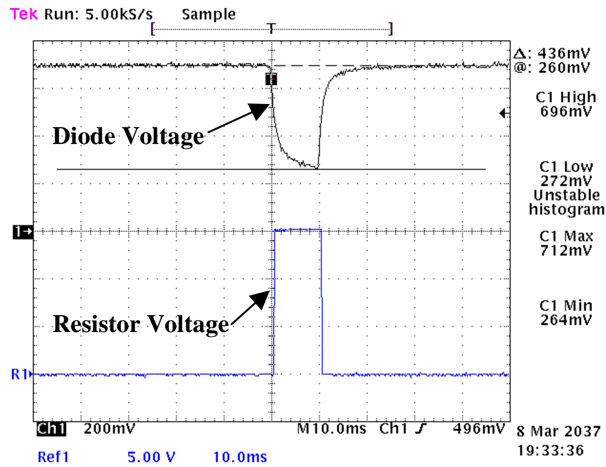


Fig.7. The changing of diode voltage due to the changing of temperature, and applying pulse voltage for the resistor heating up to get ΔT of 240°C.

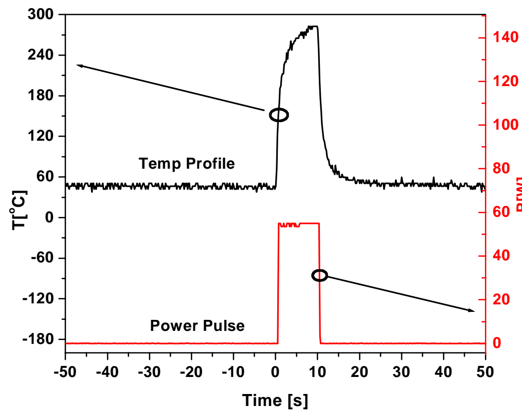
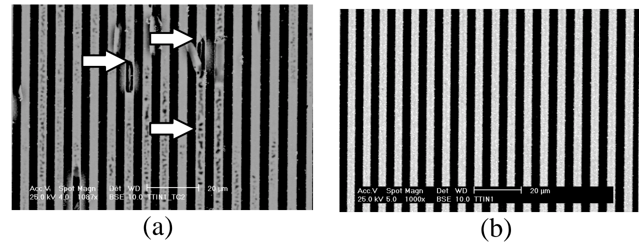


Fig. 8. Transient thermal response for a single power pulse.

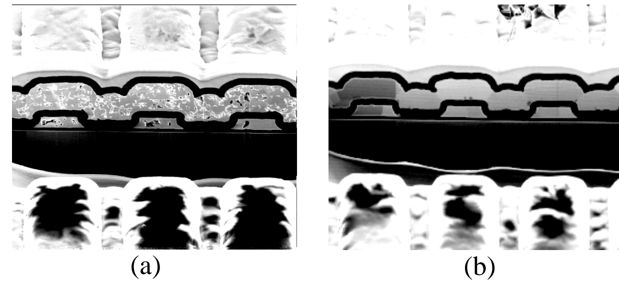
-Observing Failure and Degradation of Metal System

Four chips were stressed for 200 hours. We found that they all were already failure due to the extrusion in metal level 2 as well as from metal level 2 to metal level 1. This time stress is only roughly selected. The detail lifetime of this test chip will be discussed with another paper when are experiments will be finished. The devices were unpackaged, the passivation layer and the top metallization layer (M2) are completely removed. Then the interlayer dielectric (ILD) is etched using plasma etcher with end-point detection. The ILD is etched until 200nm left. The surface of M1 is inspected using SEM equipment with a Backscatter Electron (BSE) detector. The detail of this method can be found elsewhere[5]. This method is better than in case the ILD is completely removed as the commonly used method SEM, because the voids were observed without influence of etching silicon precipitates.



(a) (b)

Fig. 9. BSE image of M2, (a) the stress device, (b) the virgin device.



(a) (b)

Fig. 10. The cross-section by FIB; (a) the stress device, (b) the virgin device.

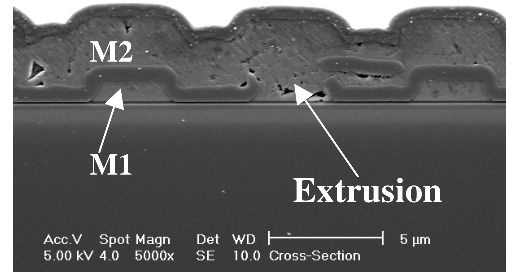


Fig. 11. The cross-section by mechanical polish showing the extrusion from M1 to M2.

The cross-section by FIB also shows voiding in both M1 and M2. To look for the extrusion from M1 to M2, the cross-section is made by mechanical polish and is inspected by SEM. The ILD is etched from cross-section away about some micrometers before SEM inspection. The SEM image of the cross-section is shown in figure 11.

III. DISCUSSION

The temperature stress method presented above can used to study thermal cycling stress very flexibly. However, we cannot get very big ΔT comparing with using conventional oven because the T_{min} cannot get a misuse temperature value like using oven. The advantage of this method comparing with oven stress that, it can get much higher number of cycles in a shot time, and the stress condition is closer by operation condition of power IC. Literature experimental data presented that the failure of thin films by temperature cycling could be fitted to Coffin-Manson law as below [2];

$$N_f \ \alpha \ (\Delta T)^{-m} \quad (10)$$

Where N_f is the lifetime in cycles, ΔT is the temperature range, and m is the exponent determined experimentally. From (10) we can see that when ΔT is small resulted N_f is very high. In this method, although the ΔT is small, a very large number of cycles can be gotten in a short time. Therefore, the testing time did not last for a long time. The test chip described above is used to carry out the fast thermal cycling experiment of multilayer interconnects. Otherwise, it can be used to carry out electromigration experiment with acceleration of temperature cycling. In this test chip, the diode is used as temperature sensor with sensitivity much higher than using a resistor, because thermal coefficient of a diode (1.8mV/^{o}C in this test chip) is higher than that of resistor (<0.5mV/^{0}C, normally).

BSE image and FIB cross-section showed a lot of voiding as well as extrusion in M1 by fast thermal cycling, the extrusion seem to be due to crack growth. The cross-section in figure 11 showed the extrusion from M1 to M2 due to cracking of IDL. Also M1 to M1 has been observed. The failure mechanism of temperature cycling can be considered fatigue failure; in which crack is a part of fatigue failure[2]. The failure mechanism in this study is found to be similar with oven temperature cycling in [1,2,6,7,8].

IV. CONCLUSION

The method of fast temperature cycling has been presented to study the failure and degradation of interconnection system by thermal stress. The temperature in the chip can be measured exactly and a million or more of cycles stress can be done with this method in shot time, which cannot be done with using oven for thermal stress. A special test chip has been designed and fabricated, and it has been successfully used with this thermal stress method. Otherwise it can be used to study electromigration using temperature cycling as an accelerated factor. The failure analyse by SEM of surface and cross-section of metal films showed that the failure mechanism are quite similar with failure metal films with using oven for thermal stress. The research program did not finish yet. The thermal stress experiment of metal films using in specified power IC industry products will be done with this test chip together with this method.

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