Highly Dependable Multi-Processor SoCs Employing Lifetime Prediction Based on Health Monitors

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***Abstract*— This paper describes the usage of I_{DDX} monitors, which provide (periodic) data to be employed for predicting the remaining lifetime of processor cores in homogeneous multi-processor SoCs during their lifetime. This forms the basis of self-repair with no mean down time for these SoCs and dramatically improving their dependability. We accomplish this goal by optimally choosing and combining our designed health monitors, such as delay and current monitors to provide non-redundant measurement data. These can be implemented nowadays as IJATG-compatible embedded instruments. Accelerated stress tests were carried out using a set of processor cores in combination with a number of health monitors providing *historic* data. These results form the basis of a remaining lifetime prediction model for delay (processor clock frequency), where the coefficients are determined by a genetic algorithm. After the final test of an individual SoC, these stored coefficients can be periodically updated in an embedded processor during its lifetime by the health monitors. In the case of seriously degrading cores, counteractions are automatically taken, like core isolation and (e.g. spare) replacement. In this case, use is made of advanced run-time mapping software. The result is a zero mean downtime SoC with 40% reliability improvement in our 9 processor-core SoC.**

***Index Terms*—I_{DDX} testing, delay testing, iJTAG embedded instruments, health monitors, HTOL, TC, lifetime prediction, dependable MP-SoC**

I. Introduction

With the decreasing dimensions in the low nanometres range (12 - 28 nm), the option of many processor-cores (> 64 - 100) is becoming viable nowadays [1]. Unfortunately, the reliability of these systems is also decreasing [2] and hence especially in safety-critical applications, counter actions are required. Also for less advanced technology nodes, this necessity already exists.

In this paper, a complete approach for implementing highly dependable multi-processor SoCs is presented, backed up by a large number of actual stress measurements. It follows the line of approach as suggested for the development of the future generation of SoCs [3].

This paper is organized in the following way. In section two, several health monitors are briefly explained which have been used in monitoring key information with regard to clock frequency degradation, the most likely issue to occur in terms of reliability (aging). These health monitors were employed together with a set of 46 processor cores during two types of accelerated stressing procedures. In section 3, high temperature operating life (HTOL) tests were carried out on 46 devices, being the Xentium processing core, during 1002 hours. It showed a high correlation between delay and quiescent I_{DDQ} and transient I_{DDT} (referred to as I_{DDX}) current measurements.

In section 4, a temperature cycling (TC) procedure was employed to further accelerate stress conditions; although degradation continued, no failing devices resulted. The previous significant amount of measurement results of a set of processor cores versus aging was used as *historic* data for determining the remaining lifetime, which is discussed in section 5. Use is made of a genetic algorithm that tries to find the best coefficients of the degraded delay of the *set* of processor-cores. These coefficients are stored in *individual* SoCs, and the coefficients are updated in an embedded processor during their lifetime based on new measurements from e.g. its I_{DDX} monitors. Here also the decision is made to replace a core or lower internal stress conditions (e.g. frequency, voltage, and power). In section 6, the core "repair" process is briefly described, via isolation and replacement of a core; sophisticated run-time mapping software (allotting tasks to specific cores) is a key element in this case. Finally, we provide conclusions.

II. Health monitors

(Health) monitors have already being used for a long time in chips and are normally part of a process-control module on a wafer to ensure flawless processing. A well-known example is the ring oscillator (RO). In addition, on-chip health monitors have also been used during the lifetime of a SoC, of which a temperature sensor is a good example for monitoring the overall chip temperature. More recently, other on-chip monitors are also being integrated, for instance in the case of aging [4]. A ring oscillator, is also referred to as odometer in the case of aging (processor speed degradation) [5]. However, one can also implement them as separate health monitors in SoCs; in that case, we will further refer to them as embedded instruments (EI). Figure 1 shows a construction of our RO-based embedded instrument, which can be *configured* in three different modes: frequency, temperature or voltage

measurement mode. The RO configuration, as well as the measurement data transport, has been accomplished via a hardware infrastructure using the IJTAG (IEEE 1687) standard [6] as shown in the figure.

A 90nm and 65nm CMOS design of our ring oscillator raw instrument was made and validated in the past, and a 40nm TSMC version is on the way.

A ring oscillator set as shown in Figure 1 is, beside able to monitor clock frequency degradation, in addition very well suited for temperature and voltage measurements over the entire SoC lifetime.

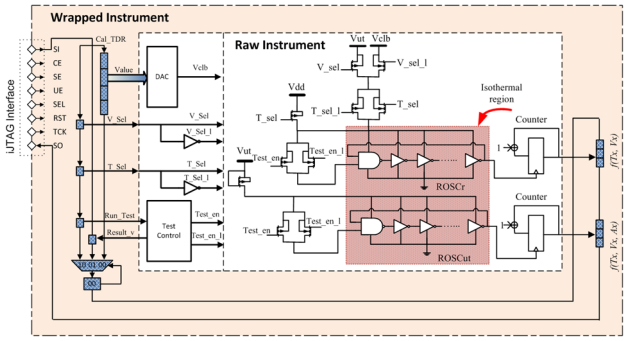

Figure 1. An IJTAG-compatible multi-sensing health monitor implemented by two ring oscillators.

Also other embedded instruments are used in *combination* with the previous EIs for our purpose of remaining lifetime prediction. Other temperature EI implementations without an RO are also possible, like for instance in [7], and they also appear now in IJTAG-compatible versions [8].

The employment of other types of EIs, like delay-slack monitors in critical paths in e.g. [9], and I_{DDQ} and I_{DDT} monitors [10, 11] have also been carried out. We monitored temperature, power-supply voltage, delay and I_{DDX} in our next experiments. In practice, ten EIs are being considered per core.

III. HTOL Stress Measurements

In order to investigate the aging behaviour of the processor core in combination with the used health monitors, in first instance 46 cores, in two batches of 23, were stressed following high temperature operating life (HTOL) procedure. It is (partly) based on the JEDEC standard (JESD22-A108) [12]. The stress temperature was 125^0C, a stressed power-supply of 1.2 volt was used (1V typical) and a stressed clock frequency of 240MHz (200MHz typical) applied during 1000 hours.

Temperature, power-supply voltage, I_{DDQ} and I_{DDT}, as well as degraded clock frequency (i.e. delay) in an actual application were measured every week.

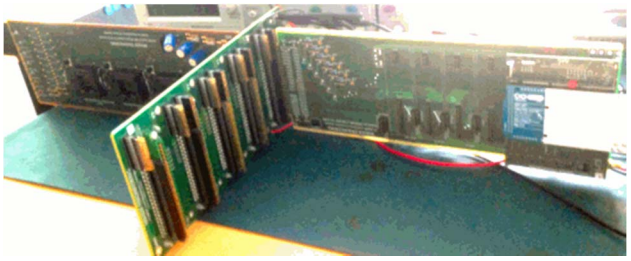

Figure 2. Hot (left) and cold (right) PCBs for carrying out HTOL and TC measurements. Health monitors and MP-SoCs are included. (Courtesy of Maser Engineering)

As the Xentium core was deeply embedded within the used MP-SoC with several other core types (UMC 90nm), creating the correct functional testing programs for I_{DDQ} and I_{DDT} tests were far from trivial and required the expertise of the actual designers. Inherently, these tests are pseudo on-line (a core has to be isolated temporarily).

One can find details on these test programs in [10] and [11]. Figure 2 shows the hot and cold (left) parts of the boards used in our test setup.

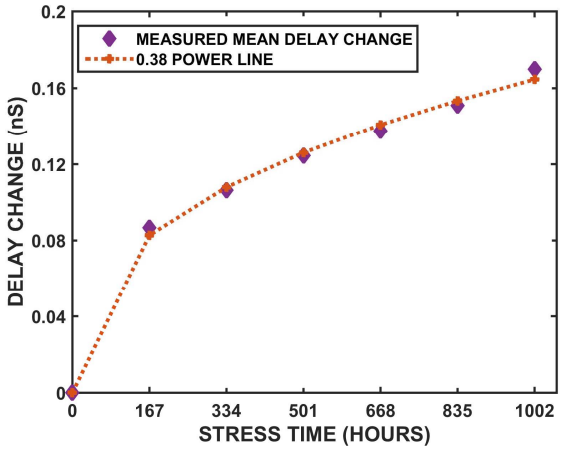

Figure 3. Delay change measurements of processor cores versus aging hours (1002 hrs.), based on HTOL of 46 devices.

In Figure 3, one can see the measured delay of the Xentium processor core versus the stress time of around 6 weeks (HTOL). The increase in delay is the strongest in the first week, after which a more modest slope appears.

Curve fitting techniques reveal a power-line relationship with 0.38 as the power coefficient. This forms the basis of our remaining lifetime algorithm, as discussed in section IV.

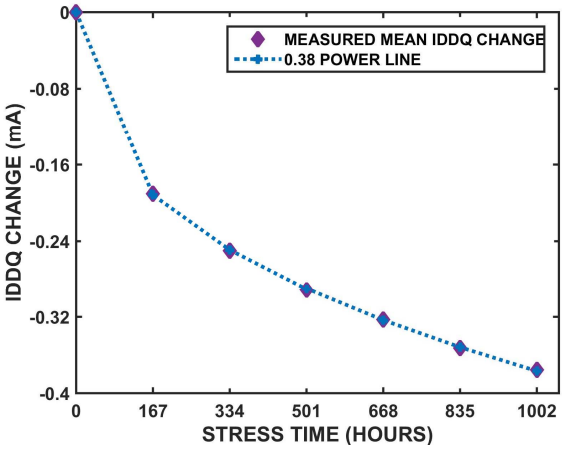

Figure 4. I_{DDQ} measurements of processor cores versus aging hours (1002 hrs), based on HTOL of 46 devices.

In Figures 4 and 5, the average of changed measured quiescent current I_{DDQ} and transient current I_{DDT} (of the P unit) values are shown versus the stress time. In both cases, one observes a decrease in current versus stress time. As is indicated in both figures, they also follow a power line, with different constants respectively, being 0.38 and 0.44. Although the different I_{DDT} values result from the different units in the Xentium processor, being arithmetic (A), load (LD), multiplier (M), pointer operations (P), logic operations (S) and storage (ST), they are all very similar.

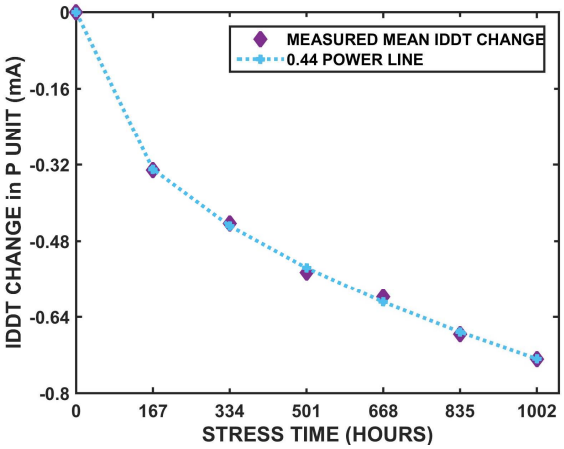

Figure 5. I_{DDT} measurements of processor cores (P unit) versus aging hours (1002 hrs.), based on HTOL of 46 devices.

It is obvious from these results, that it suggests a correlation between delay and I_{DDX} measurements. Data analysis indeed confirmed a strong correlation between them. The results are provided in Table I. It also does not matter much which unit of the Xentium is taken as a reference. It turns out the quiescent current measurement has the highest correlation coefficient. This favors the use of an embedded IJTAG-compatible current instrument.

TABLE I. CORRELATION COEFFICIENTS BETWEEN DELAY AND I_{DDX} MEASUREMENTS FOR DIFFERENT XENTIUM PROCESSOR UNITS.

SoC	I_{DDT_A}	I_{DDT_LD}	I_{DDT_M}	I_{DDT_S}	I_{DDT_ST}	I_{DDQ}
Xentium	0.937	0.953	0.956	0.957	0.941	0.971

Besides the above measurements, also data from other test array structures, like NBTI and HCI were gathered, confirming the expected V_T behaviour. The results have been used as cross-reference material. We have also carried out several frequency-aging (HTOL) measurements on different ring oscillator architectures, all showing similar frequency behaviour: rapid degradation in oscillation frequency in the beginning (weeks), and subsequently slowly rolling off after this phase. Even after more than 2000 hours HTOL, a small sample of processor cores operated still correctly within the tolerance margins.

IV. TEMPERATURE CYCLING STRESS MEASUREMENTS

For further accelerated tests after the previous 1000/2000 hours HTOL, temperature cycling (TC) stress tests (similar to JESD22-A104D) have been carried out to evoke a processor failure [13]. As TC results in mechanical stress, beside die stress changing electrical parameters, also package and wire-bond failures might occur. Use was made of a Vötsch heating/cooling system, cycling between 0ºC and 125ºC. Ramping time was 30 minutes and the dwelling times 5 minutes. The set-up of the PTC tests, as well as the used MP-SoC chip (inset) one can see in Figure 6.

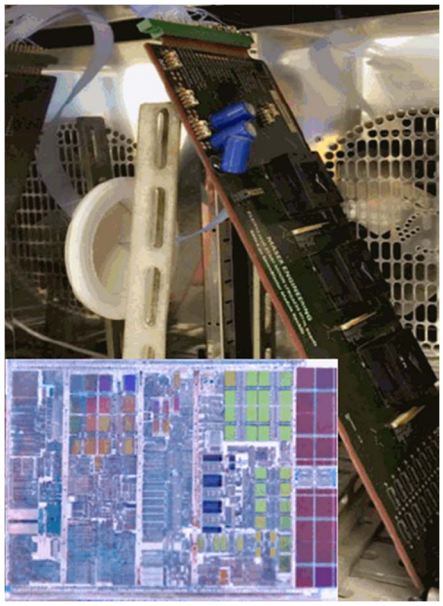

Figure 6. Test setup for the TC tests, incorporating three MP-SoC chips and an external work-program control (Arduino) board. Inset: photograph of the MP-SoC used. (Courtesy of Recore Systems)

The duration of the tests was more than 670 cycles. This added around 2000 hours (acceleration factor of 3) to the previous tests [14, 15]. Even for this extended duration, the previous power laws remained valid. This is indicated in Figures 7 and 8 for I_{DDQ} and I_{DDT} versus delay time respectively. In the latter case, several I_{DDT} sections have been included.

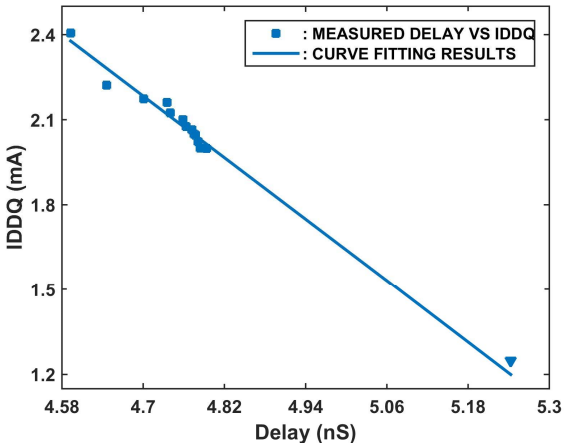

Figure 7. Representative measurement result of the I_{DDQ} of the Xentium processor core. The symbol ▼ represents PTC equivalent lifetime.

Even in the most aged available case we had for Xentium processors, equivalent to more than 4000 hours, the devices continued to operate fault-free. This at least supports our lifetime prediction calculations in the next section V.

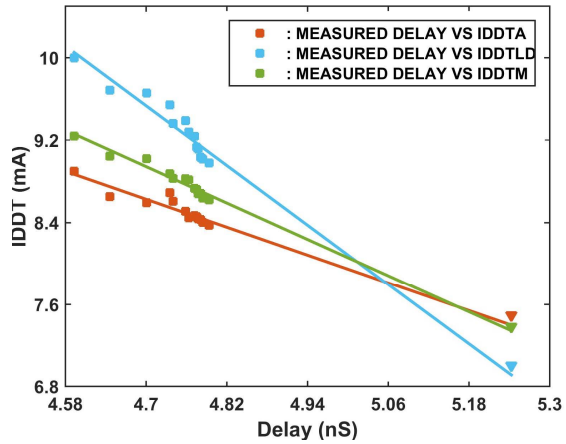

Figure 8. Representative measurement result of the I_{DDT} of the Xentium processor core; for several functional blocks. The symbols ▼ represents PTC equivalent lifetimes.

V. Lifetime Prediction Calculations

In the past several papers have been published on delay monitoring, critical path determination, and machine-learning techniques for lifetime prediction [16 -18]. Based on the many stress measurements of critical path delay, and I_{DDX}, we developed a generic algorithm (GA) based degradation model optimization and remaining lifetime prediction (RLP) method for processor cores in SoCs [19].

A. Proposed prediction method with alternate I_{DDX} testing.

Genetic algorithms [20] are a well-known technique for optimization modelled after the natural evolution process. The GA is employed to determine the combination of coefficients in our model which minimizes the degradation trend error for *all* measured processor cores via HTOL and TC (historic data). The steps are briefly described as follows and depicted in Figure 9:

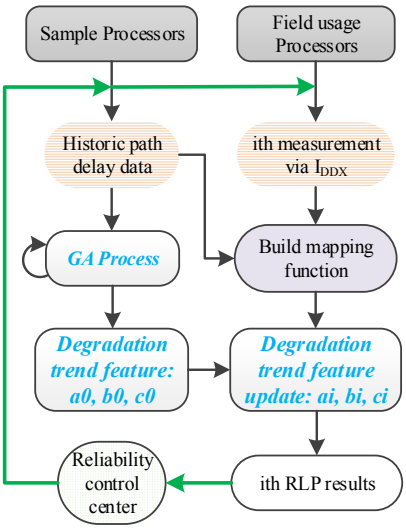

Figure 9. Overview of used lifetime prediction method via life-testing I_{DDX} testing for a specific Xentium processor in the field. In addition power-supply and temperature monitors have been included in the actual procedure. For simplicity they are omitted here.

1) Employ a set of sample processors to perform the delay testing, which will induce the general degradation trend. While health monitoring via (delay-correlated) I_{DDX} testing is employed during lifetime in each of the field-usage processors.
2) Apply the GA procedure in the case of the sample processors: prepare inputs for the GA-based delay-degradation model *f(t)*. Use the delay-measurement-driven power-law relation with respect to the time *t* to the learning model:
$$f(t) = a + b * t^c \quad (1)$$
subsequently define the so-called chromosomes (*a*, *b* and *c* in our case) representing the degradation feature, the fitness function, the selection function, cross-over method, etc. [17]. Extract the original feature parameters *a0*, *b0* and *c0* after the learning process.
3) Build the mapping function via historic delay and I_{DDX} testing data from the set of sample processors and field usage ones respectively.
4) Update the feature parameters *ai*, *bi* and *ci*, and evaluate the remaining lifetime prediction result via

the *i*th I_{DDX} testing, based on the mapping function and the GA-learned degradation model.

5) Send the RLP results to the reliability control centre for decisions on replacement (see section VI).
6) Update the RLP results based on the new (field-usage) *core-specific* I_{DDX} measurements by reliability centre. (Repeat from step 3).

B. Example of RLP in the field usage

Figure 10 shows the field usage of our RLP method. Six times, measurements have been carried out during the HTOL test, while the RLP results are *updated* in an interval of three weeks. The value of RLP1 is generated from the first 3 weeks results while RLP2 is the update based on the following 3 weeks results (Figure 10).

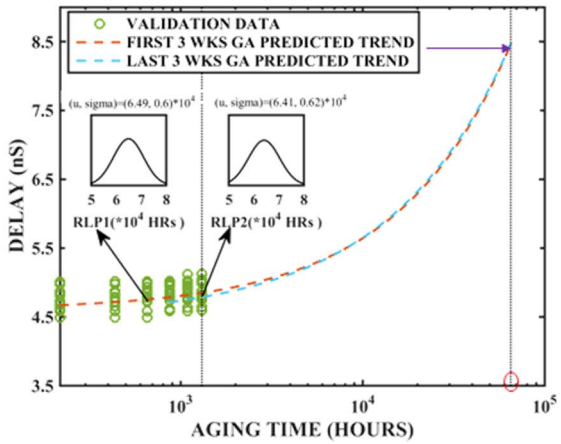

Figure 10: Example of RLP results update in field usage with available new measurements of I_{DDX} data; the update interval is 3 weeks.

The GA predicted trends do not change significantly for both cases (blue and orange). As can be seen from the figure, the fault-free device after the TC tests does not violate our previous RLP results (RLP>0). The most right grey vertical line shows the lifetime on the aging axis (red circle) after it passes the 8.5ns clock boundary (faulty processor). Furthermore, RLP results for these two cases have a mean and standard deviation of (6.49, 0.6)*10^4 and (6.41, 0.62)*10^4 hours separately (Figure 10), indicating a decrement of remaining lifetime of:

$$(6.49 - 6.41) * 10^4 \text{ hours} = 800 \text{ hours} \quad (2)$$

Considering the acceleration factor (AF) in the HTOL test, 3 weeks HTOL stress equals to $3\,weeks * AF = 3 * 7 * 24 \text{ hours} * 1.296 = 653 \text{ hours}$ (3) which is close to the updated RLP results.

VI. Highly Dependable MP-SoCs in Beam Forming

A system application in the area of beam forming for radar applications, requiring correct working operation even in the case of a potentially failing processor, has been designed using a number of many processor-core SoCs [21]. A photograph of our 9-core SoC (inset) and the complete beam-forming PCB are shown in Figure 11. The beam-forming operation is carried out using five 9-core SoCs (45 cores). Experiments with *emulated* problems (faults) in specified cores have been performed to show the correct repair by isolation and replacement of a faulty processor core. The processor core is the same (Xentium) as used in all previous paragraphs.

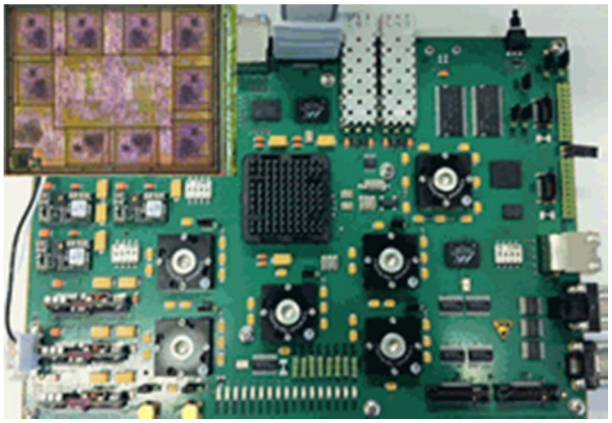

Figure 11. Photograph of the 9 processor-cores SoC (upper left), and the 45-core (5 SoCs) PCB for radar beam-forming applications. (Courtesy of Recore Systems)

Use is made of a (regularly updated) resource map showing correct and faulty cores in SoCs resulting from tests. Sophisticated run-time mapping software [22] has been applied to isolate and replace cores of the Network-on-Chip based data communication; this software runs on an embedded ARM processor. Many performed dependability tests showed the success of our isolation and repair concept.

However, the problem with that approach is that it had to perform periodic tests, and only *after* detecting a *fault* during these periodic tests (BIST), a repair could take place which requires overall an additional 42ms (100MHz clock) [21]. In our new approach, a repair action is decided following degradation measurements (RLT), well before an actual fault will occur. This enables a zero mean time, often required in safety-critical systems, like radar beamforming. Based on previous calculations [18], the reliability improved with 40% of the 9-core SoC, having two spare processor cores available.

VII. Conclusions

This paper has presented a complete (test) flow and validation of the development of a highly dependable multi-processor SoC as used in a very safety-critical application under (harsh) aging conditions. Our principle is based on incorporating a number of health monitors per processor core, implemented in practice by IJTAG embedded instruments. An efficient IJTAG infrastructure has been developed for this purpose.

The measurement data from these health monitors during lifetime are being used by our developed lifetime prediction

model, stored in an embedded processor and locally executed. Based on this, it is decided which processor core is at risk and hence phased out and which core is being used as (partial) replacement; this action is supported by an API and resource map. Compared to previous work, a *zero* down time is now accomplished, while the SoC reliability has improved by 40% in the case of just two spare processor-cores.

ACKNOWLEDGMENTS

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