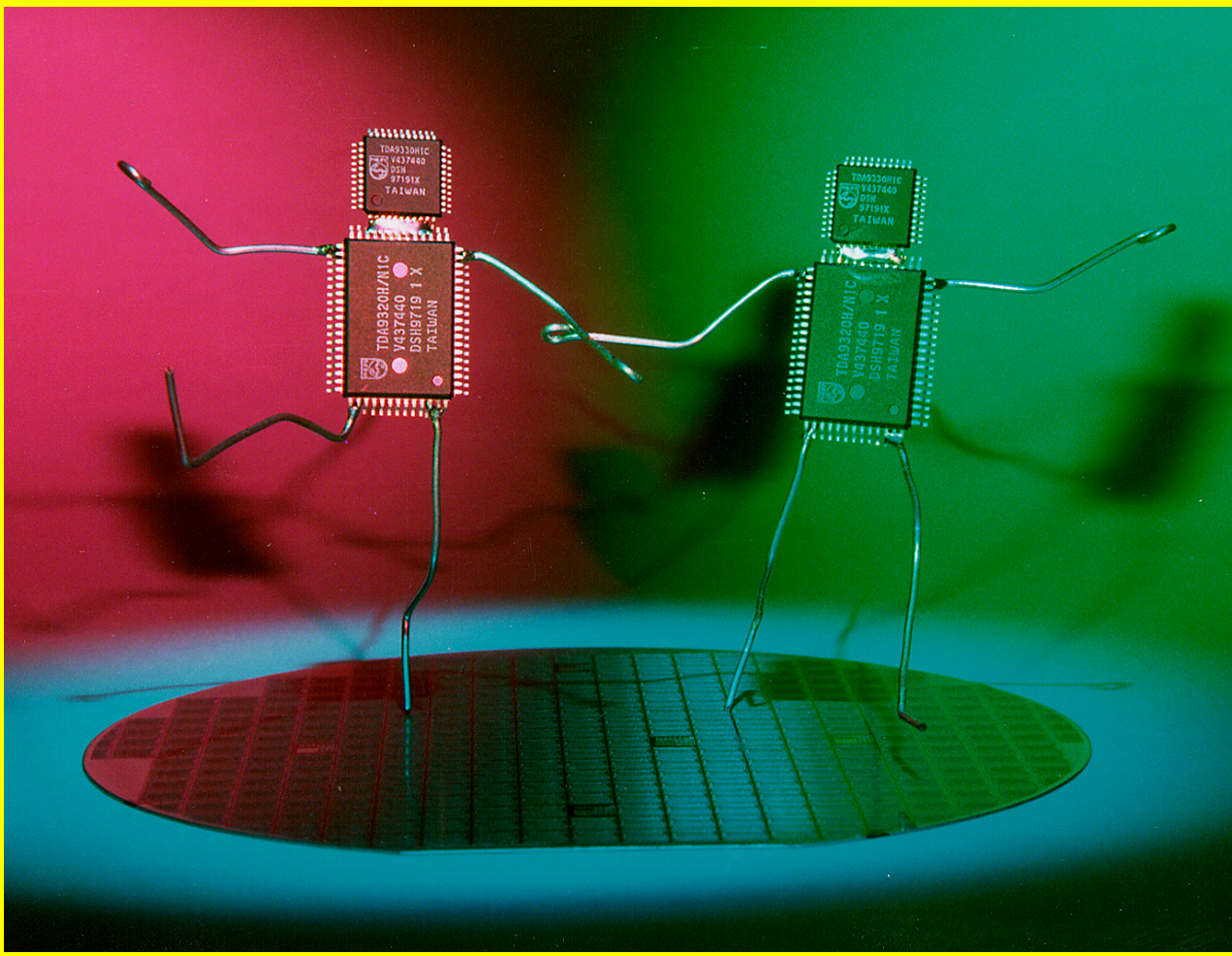
The design of low-cost one-chip TV systems



Joop van Lammeren

The design of low-cost one-chip TV systems

Joop van Lammeren

The work descibed in this dissertation was carried out at Philips Semiconductors, Nijmegen, The Netherlands, as part of the regular Philips Research and Development Programme.

Cover photograph[1]:

Hi-tek unstill life #4.0.3

HIPHOP

Title: The design of low-cost one-chip TV systems

Author: J.P.M. van Lammeren

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1. The IC making up the torso is nicknamed HIP, the IC making up the head is nicknamed HOP. HIP and HOP are members of a family of high-end TV ICs.

THE DESIGN OF LOW-COST ONE-CHIP TV SYSTEMS

PROEFSCHRIFT

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de promotor prof. dr. ir. B. Nauta

“Alles soll so einfach wie möglich gemacht werden,
aber nicht einfacher”
A. Einstein

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contents

chapter 1 7
Introduction 7
A brief history of television 7
Nipkow's electric telescope 7
from theory to practice 9
all-electronic television 9
colour television 10
The video cassette recorder 12
Cost reduction as innovation driver 13
cost and design strategy 13
TV assembly 16
ways to reduce cost 17
Outline of this dissertation 17

chapter 2 19
Analogue TV systems 19
Introduction 19
A virtual TV broadcasting system 19
Television set 26
Differences between the TV broadcasting systems 27
Differential phase errors 28
Television ICs 28

chapter 3 33
Integrator with a low unity-gain frequency 33
Introduction 33
Scope of this work 34
Continuous-time integrators 34
ideal integrator 34
practical integrator 34
Circuits for continuous-time integrators 35
Miller effect 35
active RC integrators 36
transconductance-capacitance integrators 38
Making a low unity-gain frequency 39
Low unity-gain frequencies and leakage currents 39
Integrator with gm reduction 41
Comparison with the Miller-effect circuit 43
Circuit implementation 43
influence of the bias components on the DC gain 45

Simulation results 46
Common-mode loop 47
Noise performance 48
Increasing the DC gain of the integrator 48
elimination of the influence of the collector-emitter resistance of T3 48
elimination of the influence of the collector-emitter resistance of T2 49
elimination of the influence of the collector-emitter resistance of T1 50
Simulation results 52
Verification of the integrator design 52
The oscillator design 52
Offset in the oscillator 54
maximum allowable offset on the output signals of the oscillator 54
The single-to-differential converter 55
Eliminating the offset in the oscillator 56
The offset cancellation circuit 58
the input stage of the offset cancellation circuit 58
the unity-gain frequency of the offset cancellation circuit 59
DC gain of the offset cancellation circuit 59
the output stage of the offset cancellation circuit 60
Simulation results 61
The oscillator including offset cancellation circuit 64
Measurement results 67
Conclusions 71

chapter 4 73
Mixed-signal narrow-band quadrature PLL-demodulator with programmable centre frequency 73
Introduction 73
The colour decoder part of a TV 74
Differences between the PAL/NTSC and the SECAM colour decoder 74
Traditional analogue PAL/NTSC colour demodulator 75
PAL H/2 ripple 77
dynamic behaviour of the PLL in the colour decoder 78
simulation of the open-loop response 79
specification of the PLL in the analogue colour decoder 80
Requirements on the new colour decoder 81
Towards a new design 82
Alternative PLL configurations for the colour decoder 82
PLL with matched oscillators 82
analogue PLL with digital frequency watch-dog 83
replacing analogue by digital circuitry 84
time-domain solution to the DTO jitter 86
frequency-domain solution to the DTO jitter 89
Comparison of the time- and frequency-domain solutions 91
The complete colour demodulator 91
Comparison of the DAC and MULDAC based systems 93
The component parts of the mixed-signal colour decoder 93
the direct digital synthesiser 94

the DTO 94
phase jitter on the subcarrier 96
word width of the DTO 97
number of bits in the quadrature output stage 98
saw-to-sine conversion 98
phase alternation for PAL 101
simulation of the spectra of the DTO and quadrature output stage 101
the HUE control stage 101
the input stage of the DDS 103
The digital loop filter requirements 104
The loop filter configuration 105
avoiding quantisation noise due to the burstkeying process 107
line averaging for PAL 108
the differentiator 109
The sigma-delta converter 110
The DAC for the sine and cosine signals 111
The analogue low-pass filter 114
The multipliers 116
the demodulating multipliers 116
the multiplier in the phase detector 117
Simulation results of the complete PLL 117
Circuit realisation 119
Measurement results 121
spectrum of the sine wave at the output of the low-pass filter 121
response on EBU colour bar input signal 121
output spectrum with a continuous 4.43MHz input signal 122
dynamic behaviour of the colour demodulator PLL 123
other measurements 124
The colour decoder in a one-chip TV processor 125
Conclusions 126

chapter 5 127
Analogue VLSI testing 127
Introduction 127
Functional and non-functional IC test methods 128
Current testing in analogue ICs 131
Simulations 131
current distribution due to defects 134
current distribution due to process spread 135
reject criterion based on current measurements 135
Measuring currents inside an IC 137
amplifying the voltage drop in the supply lines 138
The ICCQ test method 140
ICCQ test circuitry 141
simplified ICCQ set-up 141
Comparison of I_{CCQ} with other techniques 143
IDDQ testing 143
built-in current testing 144

macro-based testing 144
analogue scan testing 144
oscillation-based testing 145
current test techniques 145
ICCQ in a mass production IC 145
Experimental results of the ICCQ test circuitry 147
Experimental results of the ICCQ test technique 150
Determination of test limits 152
Interpretation of test results 153
ICCQ effectiveness at wafer testing 154
first experiment 154
second experiment 155
Analysis of ICCQ test data of ten batches 156
ICCQ effectiveness at final testing 158
ICCQ as a reliability test 158
ICCQ and boundary scan testing 158
Future research 159
Conclusions 159

appendix A 161
Simple noise analysis on the circuit of Fig. 29 161

appendix B 165
Mixed-signal quadrature demodulator with a multi-carrier regeneration system 165

appendix C 171
Calculation of the transfer function of the analogue PLL 171

appendix D 175
Calculation of the transfer function of the mixed-signal PLL 175
PLL model 175
Transfer of the phase detector 175
Transfer of the digital loop filter 178
Transfer of the DDS 179
Transfer of the mixed-signal demodulator 180

appendix E 183
Influence of the differential amplifier on the measurement error 183

references 185
References chapter 1 185
References chapter 2 185
References chapter 3 186
References chapter 4 187
References chapter 5 189

original contributions 193

publications 194
Papers 194
Patents 195
Pending patents 195

summary 197

samenvatting 198
Circuittechnieken voor low-cost one-chip TV systemen 198

dankwoord 199

biografie 200

chapter 1

Introduction

A brief history of television

The word television was coined in 1900 by Constantin Perskyi in a paper he read at the International Electricity Conference. Up to that time the work that was aimed at making it possible to not only hear, but also see, what's going on at a remote place was referred to as "distant vision" or "seeing by electricity".

After the invention of the telegraph and the telephone "distant vision" was the next step in the development of means of communication. However, it wasn't until the discovery in 1873 of the phenomenon that the resistance of selenium varies with the amount of light that falls upon it, that a physical mechanism was available that made the instantaneous transmission of moving pictures possible. From that time on, many attempts were made to make a system for "seeing by electricity". All early systems were electro-mechanical. The most renowned of these systems is the one invented by Nipkow in 1884.

Nipkow's electric telescope

As Nipkow's invention is an important landmark in the history of television, it will be discussed in some detail. Fig. 1 shows the original drawings of the patent.

Nipkow's system (which he called an electric telescope) uses two discs with 24 holes that are arranged on a spiral. Although the disc is big, the picture is rather small. The picture size is indicated by the dashed rectangle in Fig. 1. One disc in the system acts as the scanner (Station I of Fig. 1), the other as the display (Station II of Fig. 1). To transmit an undistorted picture, both discs must rotate synchronously.

An optical system in front of the scanning disc throws the light of the scene on the disc in such a way that there is always only one hole of the disc within the picture frame. Through this hole the light falls on a selenium photo cell. As a result the current through the photo cell is modulated. This modulated current is fed to a light modulator (Kerr cell) in the receiver. The Kerr cell is an optical device that rotates its polarisation angle, depending on the magnetic field in which it is placed (Faraday effect). The current from the photo cell is fed to the coil that is wound around the Kerr cell, so the magnetic field in the coil will change as the current changes. Light enters the Kerr cell through a polariser on the left (lower part of Fig. 1). The

PAUL NIPKOW IN BERLIN.

Elektrisches Teleskop.

Fig. 1.

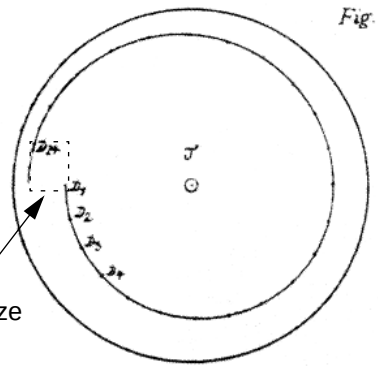


Fig. 2.

Station I.

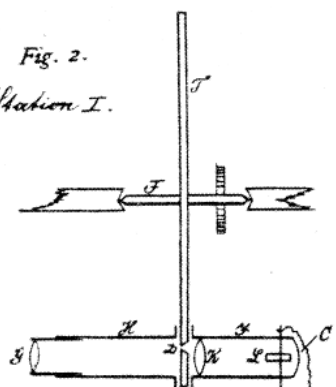
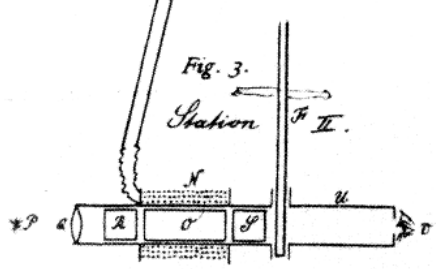


Fig. 3.

Station II.



Zu der Patentschrift

№ 30105.

PHOTOGR. DRUCK DER REICHSDRUCKEREI.

Fig. 1 Drawings in Nipkow's patent.

polarisation angle of the light is rotated as it passes the Kerr cell, and after passing through the analyser (i.e. a polariser that is placed in a right angle with respect to the input polariser), the light passes through a hole in the display disc that is in the same position as the hole of the scanning disc.

from theory to practice

Nipkow never put his idea into practice. If he had tried he would not have been successful. First, because the change in resistivity of selenium is too slow to generate an acceptable picture. Secondly, because the power needed to drive the Kerr cell is so high (ca. 10W), that in a time when power amplifiers had not yet been invented, there was no way to turn the small signal generated by the selenium cell into a strong magnetic field. But, despite these problems, the basic concepts of Nipkow's system were used by many others. In fact, the first publicly demonstrated TV system (by Baird in 1925) was based upon Nipkow's system.

all-electronic television

In the early 1900s ideas for all-electronic television, i.e. television without moving parts, were proposed by Campbell Swinton. His system was based on the then brand-new vacuum tube technology. However, it wasn't until the early 1930s that an acceptable picture tube (Zworykin's kinescope) was developed. The quality of this picture tube was such, that it soon became the standard TV display device.

Good camera tubes, on the other hand, weren't available until the end of the 1930s. Mechanical devices, such as Nipkow's discs and rotating mirror devices, remained in use until that time. Two different types of camera tube competed to become the standard: Farnsworth's image dissector and Zworykin's iconoscope. However, in the end the image dissector was no match for the iconoscope. The main reason for this was the very low sensitivity of the image dissector (something it had in common with all mechanical devices). This was due to the fact that only the light that fell on a particular picture element during the time this particular picture element was scanned, contributed to the output signal. The iconoscope was far more sensitive, as all picture elements integrated the light that fell on them between the moments they were scanned. The fact that this integrating feature is vital for a good sensitivity (and a good signal-to-noise ratio) is something that most early workers on television cameras seem to have overlooked.

The first public demonstration of an all-electronic TV system was given by Farnsworth in 1928.

As the early TV cameras were rather insensitive, for a time even "chemical signal amplification" was used by some experimenters. In these systems the scene was recorded on film (the

same type as used for cinema), and instead of winding the film on a pick-up reel, it was led into a developing/washing/fixing machine. After passing through this machine, the film was scanned with a TV camera. As the light was now concentrated on just the film frame, instead of the whole scene, good sensitivity could be obtained with even an insensitive TV camera.

Another way to get round the insensitivity of the camera tubes was to use no camera at all. Some systems used a so-called flying spot to obtain a picture signal. In these system the scene to be televised was in a darkened room. Through a Nipkow disc the light of a powerful lamp was projected on the scene. So only a small part of the scene was lit at any given time. The picture signal was generated by a light sensitive cell that was directed at the scene. As the light was illuminating just one "picture element" at a time, the light sensitive element only needed to measure the reflected light, without the need for any additional hardware such as lenses.

The first TV systems that were demonstrated in the late 1920s used approximately 30 lines. This is just enough for "head and shoulder" images. In 1933 the number of lines had grown to about 180. This was approximately the limit for the number of lines in mechanical systems and allowed full-length images of persons of reasonable quality to be televised. The number of pictures per second grew from 10 in the first systems to 60 (in the USA) and 50 (in Europe). The latter frequencies were chosen equal to the mains frequencies. Using other frequencies would have required very expensive shielding in TV sets to prevent interference between the picture and the mains frequency.

In 1937 the London Television Station (LTS) started as the world's first, high-definition, regular, public TV station. The LTS adopted a 405 lines/field and 50 fields/second standard. This was the highest definition standard at the time, and it was used in the United Kingdom until 1982.

It is interesting to note that the rapid development of low-definition to high-definition TV took place during the world-wide economic depression of the 1930s. Many companies felt the potential revenues of TV justified the high investments, despite the dire economic situation.

The second World War brought the development of TV to a halt. After the war black-and-white TV broadcasting was gradually introduced in more and more countries.

colour television

The first demonstration of a colour TV system was given by (again) Baird in 1928. The basis of his system was identical to his black-and-white system. All he did was use coloured filters in the holes of his Nipkow disc.

Some of the early colour TV systems were based on two colours only. The majority of workers soon concentrated on systems based on the three primary colours. Systems were developed in which the frames were scanned by one colour at a time. Alternative to these were systems in which the successive lines were scanned with different colours. These types of sys-

tems unfortunately could not be received on a black-and-white TV.

In 1953 the NTSC (National Television System Committee) colour TV system was introduced in the USA. In this system the colour information is not straightforwardly transmitted. Instead it is coded in such a way that the TV signal that is transmitted is the standard black-and-white signal plus two signals that carry the difference between the black-and-white information and the colour information. The latter signals are called colour difference signal. This meant that the signal could be processed by both black-and-white and colour TVs. This was a major advantage, as there was no need now to build both black-and-white and colour TV networks.

NTSC is an elegant and clever way to broadcast colour TV signals, but it is susceptible to a particular type of distortion in the transmission channel (differential phase error). New colour TV systems were developed to combat this problem. Two different lines of approach were chosen. The first way was to cancel the error in one line with an equal error, but with opposite sign, in the next line. The other way was to use another method to transmit the colour difference signals (using frequency modulation instead of quadrature amplitude modulation). In the 1950s and 1960s many variations of these two basic systems were tried out. In the 1960s the PAL (Phase Alternation on Lines) and SECAM (SEQuentiel A Memoire) colour TV systems were introduced in Europe. PAL is based on the first approach, SECAM on the second.

The most challenging component that had to be designed for the colour TV systems, was the colour display device. Even though black-and-white TV was all-electronic, some researchers opted for electro-mechanical colour displays. Others used one picture tube per colour and merged the signals of two or three tubes into one picture. The shadow mask CRT (Cathode Ray Tube) (Fig. 2) became the most commonly used picture tube. In this tube the picture is built up with the three primary colours. For each colour there is an electron gun that sends a stream of electrons to the light-emitting islands on the glass front of the tube. The electrons

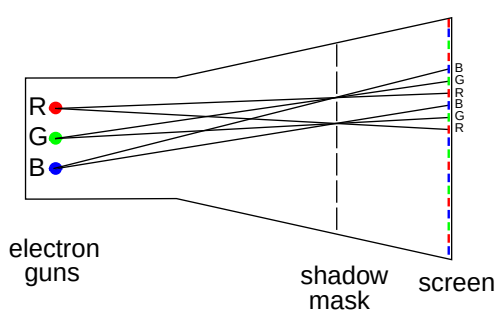


Fig. 2 Operating principle of the shadow mask CRT.

from the electron guns of one colour can only reach the light-emitting islands of their own colour. A metal screen (shadow mask) blocks their way to the light-emitting islands of the other colours.

Since their introduction the basic standards for analogue colour TV transmission have remained largely unchanged. But, additions such as stereo sound and information services, like teletext and closed captioning, have been made to the original standards.

Many attempts have been made to introduce new TV systems with a higher resolution (e.g. MUSE, D2MAC, HDMAC). All these attempts have failed to gain a large market share. In the 1990s digital TV systems have emerged. At the time of writing it is not yet possible to assess the impact of these systems.

Although the analogue TV standards have remained largely the same, the technology with which they are implemented have undergone tremendous changes. Vacuum technology has been replaced by solid-state technology in nearly the whole chain from the camera through the signal processing to the display. The only vacuum component still in use is the CRT. Numerous alternatives to the CRT have been developed (e.g. liquid crystal displays and plasma displays), but none of these have been able to gain a substantial part of the TV market up to the time of writing.

The information in this section is a compilation of material from [1]-[7].

The video cassette recorder

Closely linked to the TV is the machine that is most dreaded by consumers and TV designers alike: the video cassette recorder (VCR). Fig. 3 shows a photograph of a typical specimen. The reasons why both groups regard the VCR with such awe are, however, completely different. Many consumers think that a Ph.D. degree is a prerequisite for a successful attempt to program a VCR. To the TV engineering community, on the other hand, the VCR is the epitome of Murphy's Law: if there is a way in which a VCR signal can deviate from the TV standards, it will. Due to the constraints imposed on it by the mechanics, the output signal of an analogue VCR often bears only a superficial resemblance to a TV signal as defined in the standards (see chapter 2). When playing back tapes with a copy-protection signal things are even worse, as the copy-protection signals do not adhere to the standards (on purpose!) to make recording impossible. At the same time a TV is supposed to be completely insensitive to these aberrations. Therefore turning a VCR signal into an acceptable picture is one of the big challenges of TV design.

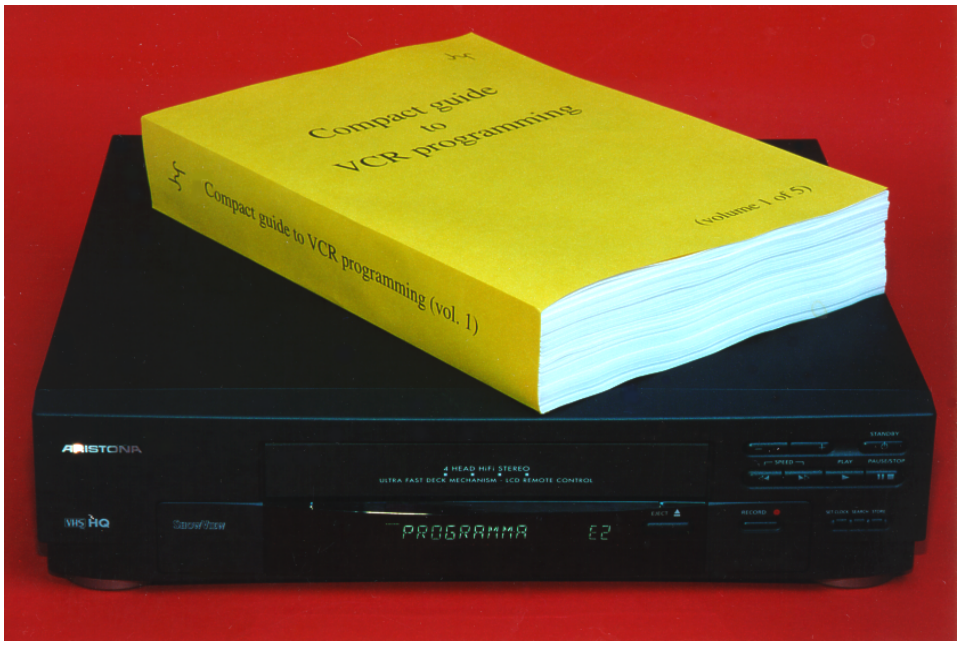


Fig. 3 Specimen of the most awe-inspiring machine on earth.

Cost reduction as innovation driver

Ever since colour TV broadcasting was first introduced in the USA in 1953, colour TV sets matured to a very high level of quality. As a result of this, the major driving force for innovation today is no longer higher performance, but lower cost. Only in the most expensive TV sets performance improvement is still an issue with innovations like motion estimation/compensation, that provide a smoother portrayal of movements on the screen. However, in by far the biggest part of the market (>80%), *cost* is the most important issue. The cost for the customer can be lowered in two ways: provide more functions for the same price, or provide the same functions for a lower price.

cost and design strategy

In the early years of black-and-white television it took up to 20 valves to make a good TV receiver. Considering that most types of valve represent two amplifying functions, it should be possible to make a good black-and-white TV with 40 transistors. As colour TV pictures are the

addition of a red, a green and a blue picture, a colour TV should basically need no more than 120 transistors. However, even the simplest TV nowadays contains many thousands of transistors. The reason for this lies in the fact that the valves were expensive components, whereas components like resistors and capacitors were (relatively) cheap. Nowadays transistors are extremely cheap, and components like inductors are (relatively) expensive. So the design strategy which was focused on using as few active components (i.e. valves) as possible has shifted to a strategy in which the number of passive components (i.e. inductors and capacitors) must be kept at an absolute minimum. This shift in design strategy was caused by the introduction of integrated circuits. The thousands of transistors are not individual components (like ye olde valves), but they are embedded in ICs. This makes individual transistors (and also integrated resistors and capacitors) very cheap indeed. Therefore the introduction of ICs was a major breakthrough in lowering the cost of TVs.

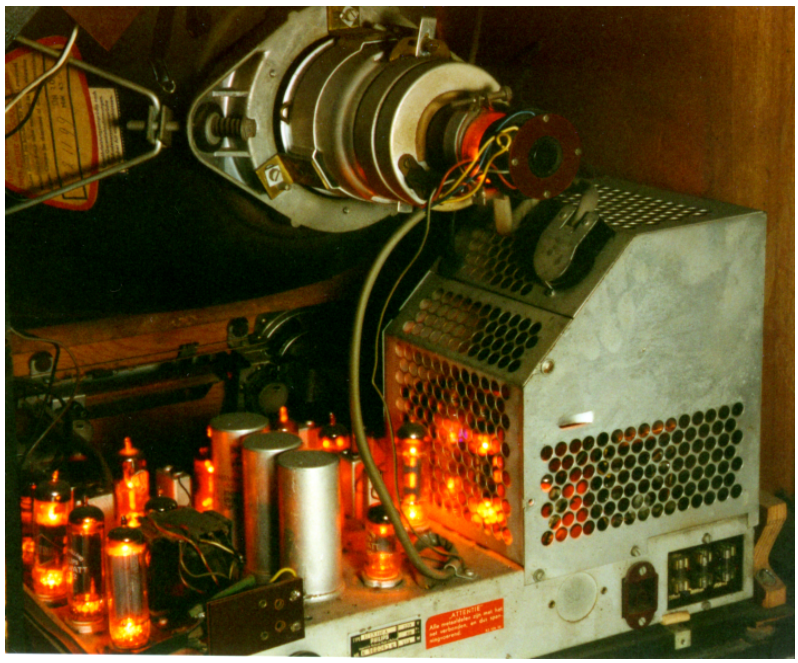
Table 1 gives an rough indication of the relative prices of components in 1962 [8] and 2000. The dramatic reduction of the relative price of an integrated transistor is also valid for integrated resistors and capacitors (up to several 10pF).

component	1962	2000
resistor	1	1
capacitor	2	1.5
inductor	25	15
valve	50	n.a.
transistor	50	2
integrated transistor	n.a.	0.01

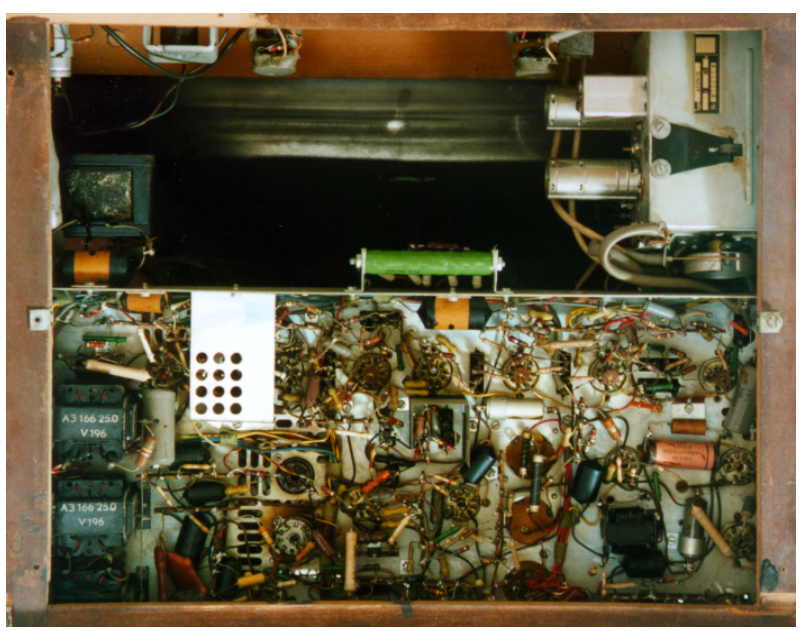
Table 1 Approximate relative prices of components in 1962 and 2000. The price of a discrete resistor is chosen as reference for both years. The table gives no information of the relation of the relative prices between the years.

In 1960[1] the price of a 66cm black-and-white TV was approximately Dfl. 1200. In 2000 a 66cm stereo colour TV with teletext and remote control has a price tag of approximately Dfl. 1200. So despite many years of inflation the nominal price of a TV has hardly changed. But, the number of features, as well as the quality of the picture and sound, has gone up tremendously.

1. Before 1960 the TV market was not really a mass market. It is not fair to compare prices of a mass market with prices in an emerging market.



(a)



(b)

Fig. 4 Internal organs of a black-and-white TV set, model year 1955.
(a) rear view, (b) bottom view.

TV assembly

Fig. 4 shows a 1955 model black-and-white TV. In this TV 18 valves and numerous passive components perform all the signal processing and power amplification functions. Most of the passive components are placed at the underside of the chassis. All components in this TV were mounted by hand. Fig. 5 shows a 2000 model stereo colour TV, with teletext and remote control. All signal processing and control functions, except the stereo decoding, are performed in the indicated IC (with the aid of just a few external components). This IC is actually a multi-chip package in which two ICs, made in different processes, are combined. Even though the assembly of the printed circuit board is completely automated, combining two ICs in one package reduces the production cost of the TV set (less board space, fewer components needed on stock).

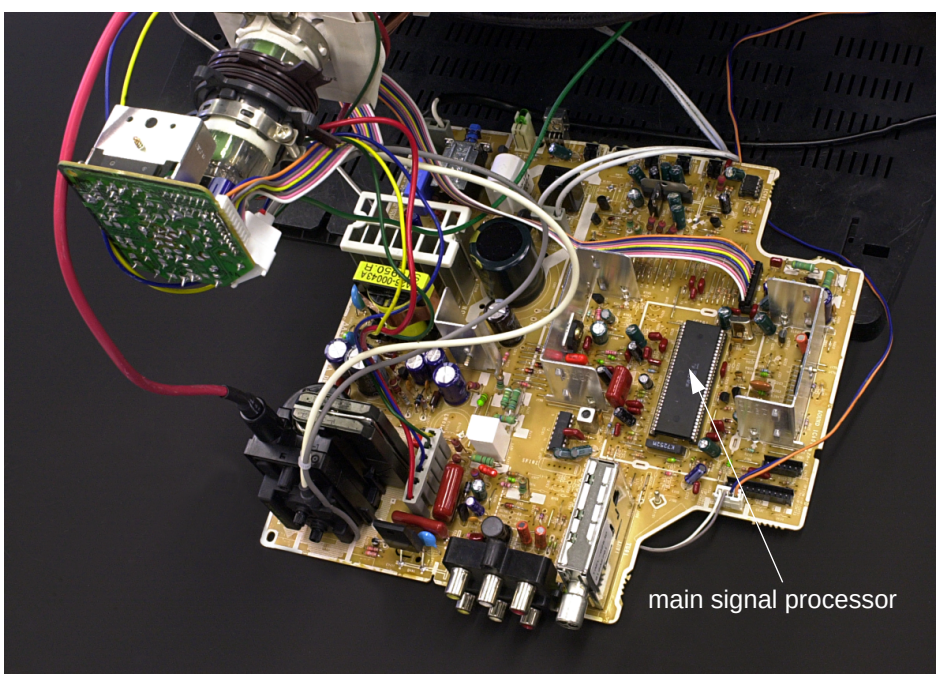


Fig. 5 Stereo colour TV chassis, with teletext and remote control, model year 2000.

ways to reduce cost

As all signal processing functions of TVs are nowadays performed by integrated circuits, lowering the cost of the signal processing part of a TV receiver is equivalent to lowering the cost of these ICs and their peripheral components. A lower cost of the application of an IC can be accomplished by e.g.

1) using a process with smaller dimensions

2) integrating external components

3) designing smaller circuits

4) designing circuits that do not need external components

5) eliminating adjustments needed for the correct operation of the IC

6) design/layout for manufacturability to maximise the yield

Apart from the silicon- and design-related costs there are also other cost factors in IC manufacturing, e.g. encapsulations and test costs. To keep these costs down the number of pins of the IC must be kept as low as possible. This means that external components that only serve the correct operation of the IC, but aren't necessary for the rest of the TV, should be eliminated by making an integratable version of such components, or by making a new circuit that can do without the external components. The ever-growing complexity of analogue and mixed-signal ICs, and the drive to reduce the number of pins of the encapsulation, require new test methods. The number of signals that can be observed to see whether the IC is good or not becomes small compared to the total number of signals in the IC. Without countermeasures the test time of IC would rise enormously as a result of this.

Outline of this dissertation

This dissertation describes integrated circuit techniques for one-chip TV systems which focus on lowering the total cost of the application. Three different approaches to cost reduction are explored.

Chapter 3 describes an integrator circuit with a low unity-gain bandwidth. This circuit is applied in a voltage controlled crystal oscillator to minimise the offset on the quadrature outputs. The integrator circuit can be regarded as an integrated alternative to a large external capacitor.

Chapter 4 describes a mixed-signal quadrature demodulator that performs as much as possible of the signal processing in the digital domain, without digitising the input signal. This

demodulator is an example of a subsystem that has been designed to use the signals that are already present in the IC to such an extent, that this subsystem no longer needs its own external components.

Chapter 5 discusses a fast, generic test method for analogue VLSI circuits. This test method reduces the test time of an IC significantly with a only small number of additional components. The test method is non-invasive to the circuits under test. The additional components only monitor the supply current of the circuits, so they have no influence whatsoever on the operation of the IC.

To give some background information on the systems for which the circuits described in this dissertation were developed, a brief description of analogue TV broadcasting systems and TV receivers will be given in the following chapter.

chapter 2

Analogue TV systems

Introduction

There are three principal colour TV broadcasting systems in use around the world: NTSC, PAL and SECAM. Of these broadcasting systems NTSC is the oldest one. The PAL system can be regarded as a refinement of NTSC. The colour rendition of the NTSC system can degrade quite heavily due to distortion in the transmission channel (differential phase errors). PAL was designed to be less sensitive to this. The SECAM system is an alternative to PAL that uses a completely different modulation scheme for the colour information to reach the same goal.

In the following a virtual TV broadcasting system will be described that combines aspects of all the systems that are in use around the world. At the end the most important differences between the various real-life systems will be listed. After the description of the TV broadcasting systems, the signal processing part of a TV set will be described. The information in these sections was taken from [9]-[11].

A virtual TV broadcasting system

A TV signal transmits 25 pictures (or frames) per second. Each frame is built up with 625 lines. A frame is transmitted in two fields of 312.5 lines. This approach has the advantage that although only 25 pictures are transmitted (which is enough for the impression of smooth movement), the picture is refreshed 50 times per second (which, for most people, is enough to eliminate the impression of flicker). This trick is similar to the system used in film projection where 24 frames per second are on the film and each frame is projected twice in rapid succession. There is one crucial difference, however, between film and TV. Whereas the film projects the whole picture twice, TV frames are projected in two fields. A field contains half of the lines of a frame, so two fields combined make up a frame. This has the advantage that the amount of information that has to be transmitted is determined by the amount of information in the picture and not by the repetition rate of the projection device. The technique of transmitting half the number of lines per field is called interlacing (Fig. 6). The bold lines are the visible lines. The thin lines are in the first field, the bold ones in the second field. The dashed lines are the invisible flyback trajectories of the electron beam.

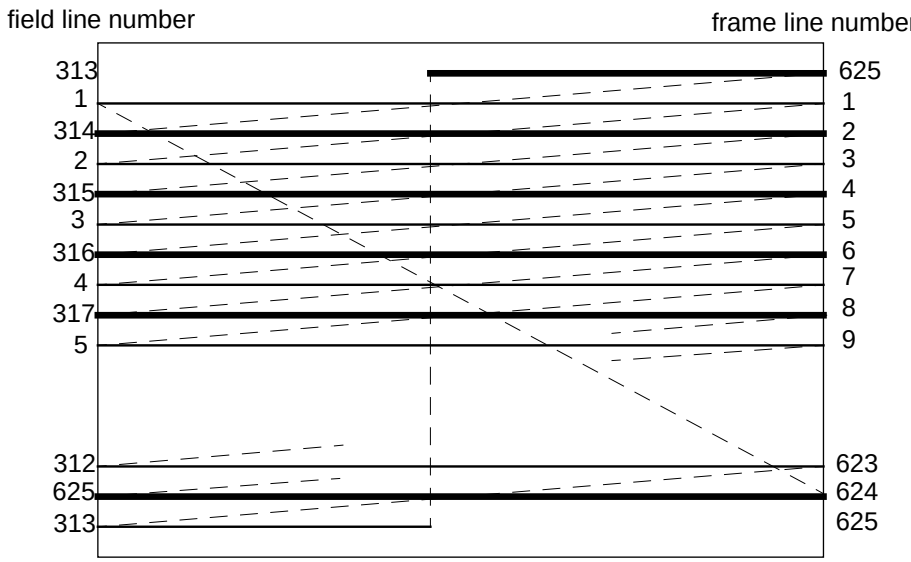


Fig. 6 Line structure of a TV picture.

In the first field all odd lines of the frame are transmitted. In the second field all even lines of the frame are transmitted. The limited resolution of the eye helps in giving the impression of a continuous flow of pictures, even though the light of the two fields of each frame does not originate in the same pixels of the picture tube. Note that the numbers on the left in Fig. 6 are the line numbers in the field (i.e. the order in which they are transmitted). The numbers on the right are the line numbers in the frame (i.e. the number in the complete picture).

Fig. 7 shows the construction of a baseband TV signal. Fig. 7a shows the time domain without sound. The signal shown in Fig. 7a is called a CVBS signal (Composite Video Baseband Signal). Fig. 7b shows the frequency spectrum of a baseband TV signal including the sound.

As mentioned earlier, each TV frame is built up of 625 lines. There are 25 frames per second, so per second 15625 lines are transmitted. This means that each line is 64µs long. During 52µs video information is transmitted. The other 12µs are used to transmit other information that the TV needs to project a good picture. In the TV itself the 12µs are used to move the electron beam in the tube back to the start of the next line. Each line starts with a synchronisation (or sync) pulse. The start of a new field is indicated by a wide sync pulse (dotted sync pulse on the right in Fig. 7a). In the first field (with the odd lines of the frame) the start of the field sync

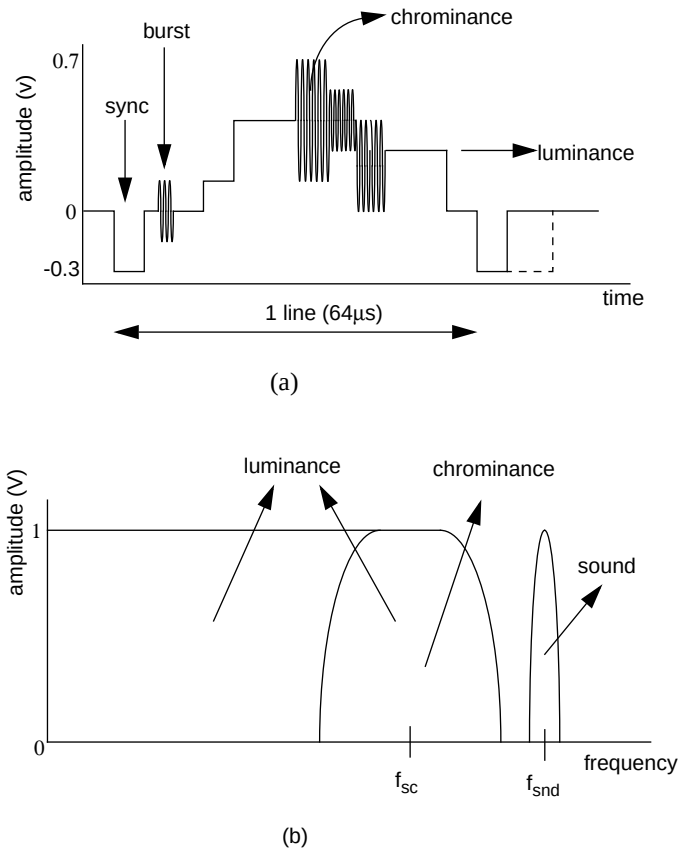


Fig. 7 TV signal in (a) time domain without sound,
(b) frequency domain with sound.

pulse coincides with the line sync pulse. In the second field (even lines) the field sync pulse starts between two line sync pulses.

The colours in a TV picture are made by combining the three primary colours: red (R), green (G), and blue (B). To maintain backwards compatibility with black-and-white TV broadcasting systems, the colour TV signal is not transmitting the R, G and B information, but so-called luminance and chrominance signals. Backwards compatibility was an important boundary condition when colour TV was introduced. This was necessary to make sure that viewers could watch the same TV programmes on both black-and-white TVs and colour TVs, without having to make special channels for colour TV.

The luminance signal carries the information that is also used by black-and-white TVs. It

represents the amount of light in the scene. The chrominance signal carries the information about the tint of the colour and its saturation. The luminance signal is designated by the letter Y. The chrominance signal carries the colour information in the form of two colour difference signals: the difference of the red signal and the luminance (R-Y) and the difference of the blue signal and the luminance (B-Y). The luminance is made at the transmitter side by combining the R, G and B signals:

$$Y = 0.30R + 0.59G + 0.11B \tag{1}$$

By combining the Y, R-Y and B-Y signals in the TV, the original R, G and B signals can be recovered (three equations and three unknowns).

The theory behind luminance and chrominance processing is beyond the scope of this work. A good introduction can be found in [9].

The chrominance information is modulated on a subcarrier f_{sc} that is placed in the upper part of the luminance spectrum. The amplitude of this subcarrier is a measure for the colour saturation, its phase determines the colour tint (also called hue). The subcarrier can carry two different types of information, because the information is quadrature modulated on it (Fig. 8). To be able to reproduce the correct colour tint the TV needs a reference to know what ‘phase zero’ is. The burst, which is transmitted after the sync pulse (see Fig. 7a) contains this information.

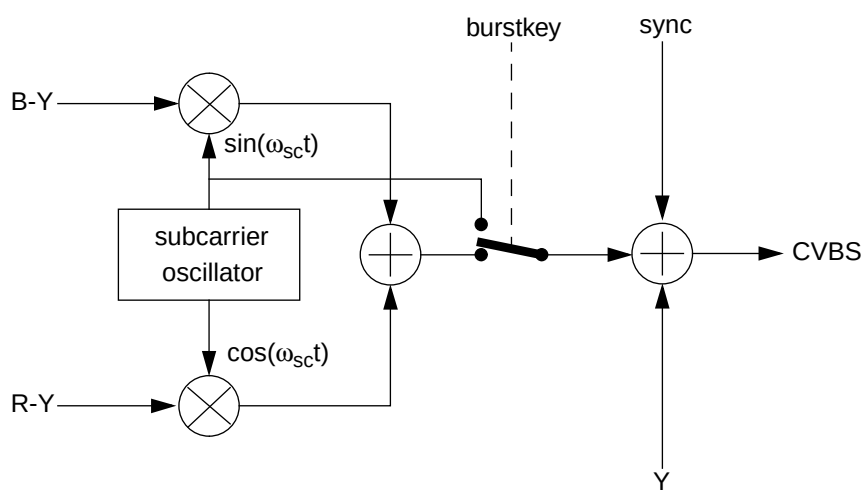


Fig. 8 Generation of the CVBS signal in a TV transmitter.

Fig. 8 shows how the chrominance, burst, luminance, sync are added to form a CVBS signal. This CVBS signal is the signal shown in Fig. 7a.

When inspecting the spectrum of Fig. 7b, it is obvious that the luminance and chrominance share a part of the spectrum. This will inevitably lead to crosstalk. This crosstalk can be seen as the colours running through a striped shirt (cross-colour), or as a band of vertically moving dots between saturated colours (cross-luminance or dot-crawl).

At first glance it may seem strange to let the spectra of luminance and chrominance overlap, but this scheme was selected to keep colour TV signals compatible with black-and-white TV signals. The colour subcarrier frequency was chosen such that the artifacts that arise due to the overlapping spectra are as small as possible.

The sound that accompanies the picture is modulated on a second subcarrier (f_{snd} in Fig. 7b) with a frequency just above the maximum frequency of the luminance spectrum.

For broadcasting of television signals vestigial side band (VSB) modulation is used. This modulation scheme combines the best elements of single side band (SSB) and double side band (DSB) modulation. Straightforward amplitude modulation of a carrier results in a DSB signal. Such a signal has twice the bandwidth of the modulating signal. By suppressing one side band of the DSB signal an SSB signal is obtained. An SSB signal has the same bandwidth as the original signal. However, whereas a DSB signal is easily demodulated in the receiver, this is not true for an SSB signal. A DSB signal can be demodulated by a simple envelope detector. For the demodulation of an SSB signal a more complex demodulator is needed (e.g. a quadrature demodulator). When TV was first introduced, electronic components were expensive. To keep the television receivers simple (and thus cheap) VSB was chosen as the modulation scheme for TV signals. In a VSB signal one sideband is broadcast completely, the other is partially suppressed to save bandwidth. For black-and-white TV signals a simple envelope detector can be used for demodulation. Black-and-white TV signals have most of their energy in the low frequencies, so that the distortion that is the result of this simple way of demodulation is not too annoying. Colour TV signals require more sophisticated demodulators, as they do contain many high-frequency components due to the modulation of the colour information

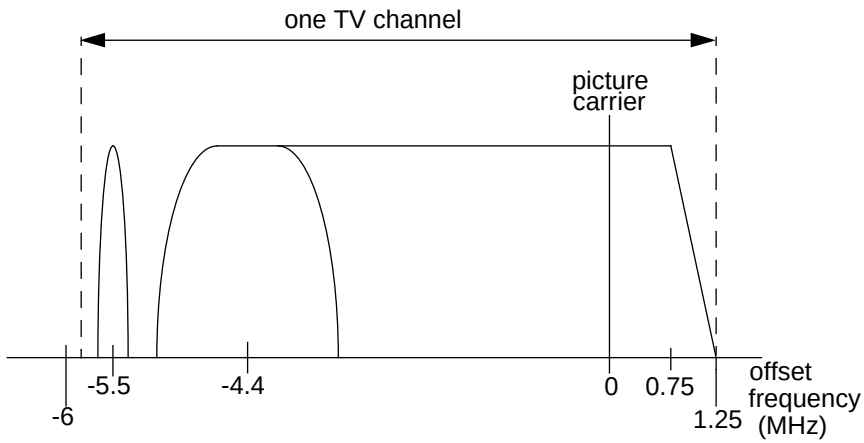


Fig. 9 Broadcast spectrum of a VSB modulated TV signal with respect to the picture carrier.

on a subcarrier. Fig. 9 shows the spectrum of a VSB modulated PAL TV signal.

As the low-frequency components of a VSB signal are effectively broadcast in DSB mode and the high-frequency components in SSB mode, a filter with a so-called Nyquist slope is used in front of the demodulator to get a flat amplitude response of the output signal (Fig. 10). Note that the lower side band is broadcast completely, and the upper side band partly.

Fig. 11 shows the well-known EBU colour bar (European Broadcasting Union), a test signal that is widely used to get a quick impression of the performance of a TV broadcasting

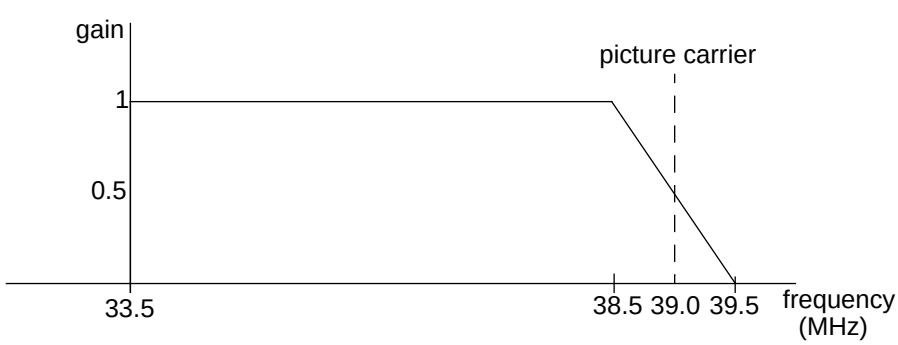


Fig. 10 Idealised transfer of the input filter of the VSB demodulator.

chain [11]. This signal will come back in the measurement sections of the circuits that will be discussed in the following chapters. The colour difference signals in this colour bar are called U and V, with U = (B-Y)/2.03 and V = (R-Y)/1.14.

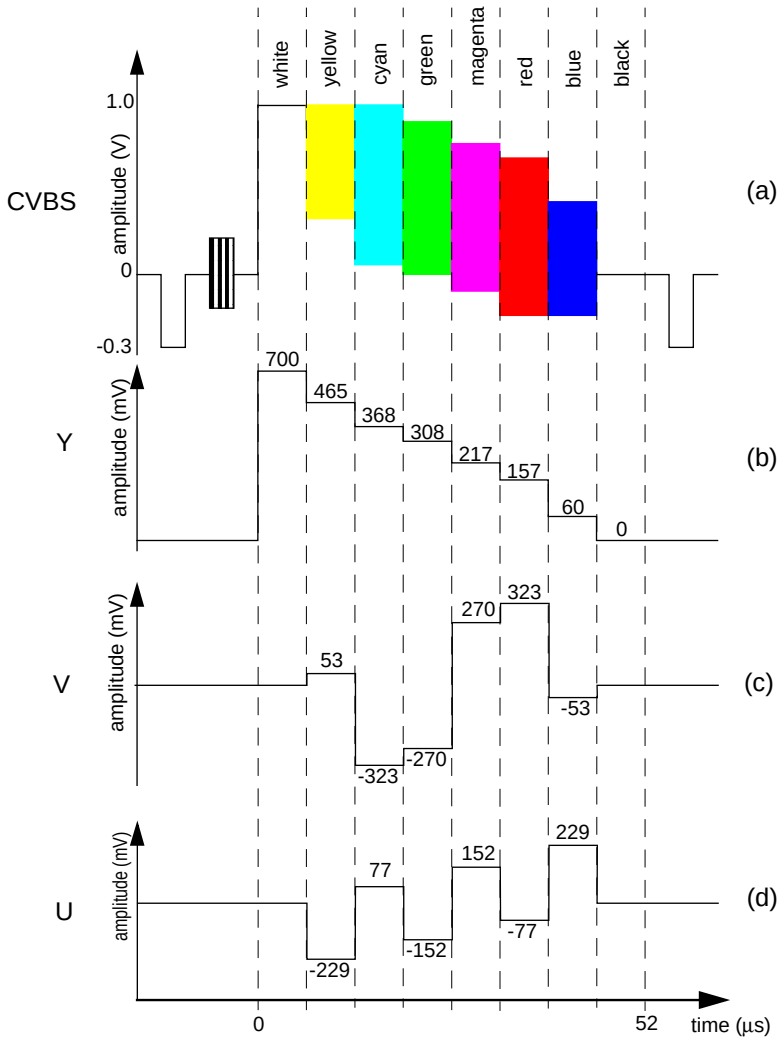


Fig. 11 PAL EBU colour bar: (a) CVBS, (b) luminance, (c) V, (d) U.

Television set

Fig. 12 shows the block diagram of a straightforward analogue colour TV. Through the antenna the input signal enters the tuner. The tuner converts the input signal from the input frequency that can be anywhere in the range from 50 to 900MHz to a 39MHz intermediate frequency (IF). The bandwidth of the incoming TV signal is 6.25MHz, and the TV channels are spaced 7MHz apart. The exact bandwidth and channel separation for terrestrial broadcast signals vary from country to country. Cable networks sometimes deliberately use a different channel spacing to prevent interference problems. Extremely complicated filters would be needed in the tuner if the channel separation were made with one tunable band-pass filter. With the superheterodyne approach the band-pass filter in the tuner can be wider: the input signal is converted to 39MHz and here the selectivity is made by one fixed band-pass filter with the response shown in Fig. 10.

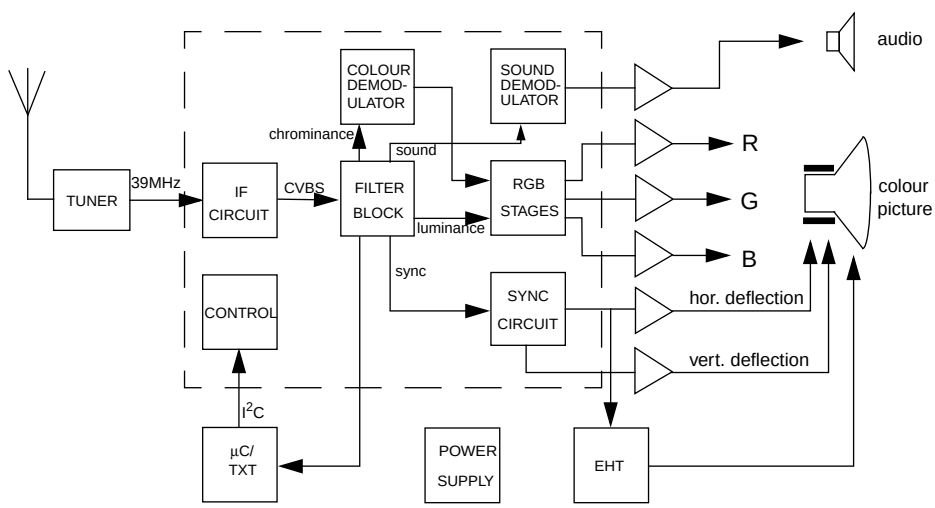


Fig. 12 Block diagram of a basic TV.

The IF circuit converts the signal coming from the tuner to a baseband CVBS signal. The output signal of the IF circuit is the signal shown in Fig. 7. The CVBS signal is split into its component parts in the filter block. The sound signal is fed to a sound demodulator, whose output signal drives the loudspeaker after power amplification. The chrominance signal goes to the colour demodulator that outputs the colour difference signals. The luminance and colour difference signal are combined in the RGB stages. These stages drive the Red, Green and Blue guns of the picture tube. The synchronisation signal is fed to the sync circuit that comprises a PLL to recover the starting points of the lines. The vertical sync signal is usually recovered

with the aid of a digital counting circuit. The sync pulses themselves are not used directly, to increase noise immunity of the TV. Without these circuits the pictures will show jagged vertical edges and roll vertically, even with relatively low levels of noise.

The power supply unit is a switched mode circuit. Sometimes the line frequency of the TV is used as the switching frequency. This has the advantage that there is no risk of interference of the power supply and the deflection. Another possibility is to use a free-running frequency. This has the advantage that it is easier to make the circuit insensitive to mains- and load variations.

The acceleration voltage (EHT: Extremely High Tension, about 30kV) that is needed in the picture tube is usually generated by a circuit that uses the flyback voltage of the horizontal deflection coil.

A signal that has not been mentioned in the foregoing is the (digital) teletext signal (TXT). This signal is transmitted in the lines directly after the vertical sync pulse. These line are not carrying video information, because it takes some time to move the electron beam back to the starting point of the next field. So, although the 625 lines per field as shown in Fig. 6 are transmitted, the first 25 lines in each field are not displayed. The TXT signal is also filtered out of the output signal of the IF circuit and fed to a microprocessor for processing. This processor is also used to control all internal functions of the TV.

As mentioned earlier, a transmitted TV picture is built up of 50 fields per second. Some people don't experience this as a stable, but as a flickering picture. In so-called 100Hz (or scan-conversion) TVs each field is stored in a memory and displayed twice in rapid succession. By increasing the repetition rate of the picture by a factor of two like this, the flickering effect can be made invisible.

Differences between the TV broadcasting systems

The system described above is not an actual TV broadcasting system. PAL, NTSC and SECAM have a number of differences, the most important of which are listed in Table 2. The list only summarises the most important differences.

The SECAM colour information is frequency modulated on two different subcarriers. Each line the subcarrier switches to the other frequency. The reference phase of the colour burst of PAL switches between two values: -45^{o} and $+45^{o}$. Each line the phase changes to the other value. There also two variants of PAL with colour subcarrier frequencies of 3.575611MHz and 3.582056MHz.

All broadcasting systems also have small differences from country to country. Especially the IF modulation has a lot of variants [10].

	NTSC	PAL	SECAM
field frequency	60Hz	50Hz	50Hz
number of lines/frame	525	625	625
colour subcarrier (burst) frequency	3.579545MHz	4.433619MHz	4.25 MHz 4.406MHz
burst reference phase	0^o	$+/-45^o$	n.a.
sound subcarrier frequency	4.5MHz	5.5MHz	6.0MHz
IF frequency	45.75MHz	38.9MHz	38.9MHz

Table 2 Differences between the most commonly used versions of NTSC, PAL and SECAM.

Differential phase errors

As mentioned earlier, NTSC signals are sensitive to differential phase errors of the transmission channel. This means that the phase of the signals changes slightly as a function of the signal amplitude. As the colour tint is coded in the phase of the modulated colour subcarrier, this results in a wrong colour on the screen. Therefore NTSC television have a so-called hue control button that allows the viewer to adjust the colours. As the viewer does not normally have measurement equipment at hand to find the optimum setting, setting the hue amounts to adjusting the colours to his/her taste. Adjusting the hue is done in the TV set by demodulating the quadrature modulated colour subcarrier with $\sin(\omega_{sc}t+\phi_{hue})$ and $\cos(\omega_{sc}t+\phi_{hue})$, instead of $\sin(\omega_{sc}t)$ and $\cos(\omega_{sc}t)$.

PAL and SECAM TVs do not have a hue control button as these were designed to be insensitive to differential phase errors. PAL accomplishes this by a slight modification of the modulation scheme (with respect to NTSC), SECAM by using frequency modulation (FM) instead of quadrature amplitude modulation for the chrominance signal [9].

Television ICs

The market of TV ICs is divided in three segments: low-end, mid-range, and high-end. The low-end and mid-range ICs are used in 50/60Hz TVs, the high-end ICs are used in 100Hz TVs only.

For the lowest end of the market two ICs, an analogue signal processor and a microcontrol-

ler are put in one package, a so-called multi-chip package (MCP). Fig. 13 shows such a package. This construction has the advantage that both the (analogue) signal processor and the (digital) microcontroller can be made in a process that is optimal for these functions. This brings considerable cost savings to the manufacturer of these ICs. For the TV set maker it is advantageous, because he has to handle only one component. On top of that the printed circuit board will be smaller and simpler.

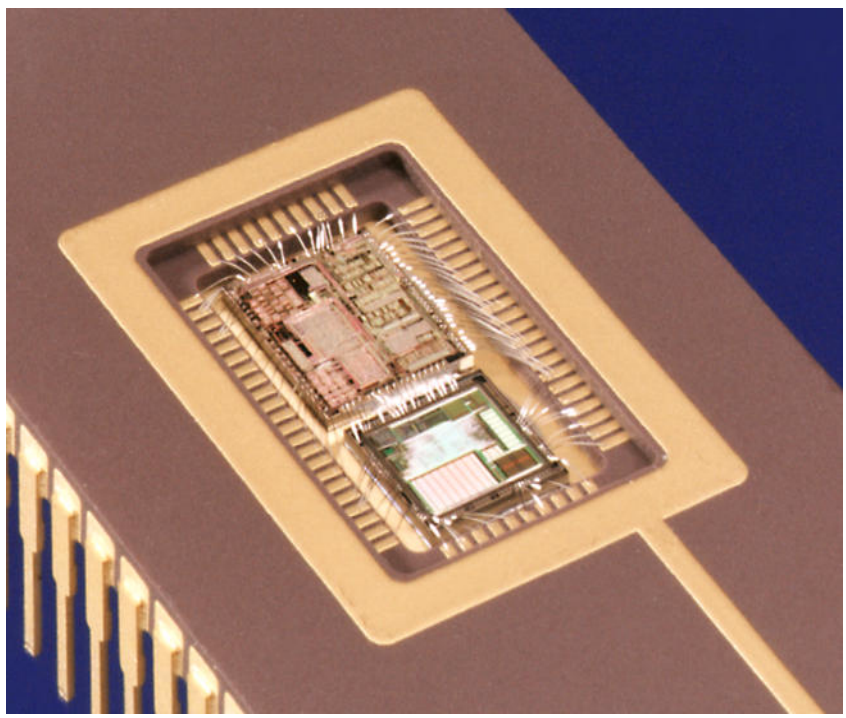


Fig. 13 MCP with analogue TV processor and digital microcontroller for low-end applications.

Fig. 14 shows a mid-end analogue signal processing IC for 50Hz TV. As there is no need to digitise the video signal in a 50Hz TV, all signal processing in such a TV is usually done in the analogue domain. In a 100Hz TV the signal does have to be digitised, because it must be stored in a memory. Depending on the architecture of the TV the signal is digitised for the memory only, or (a part of) the signal processing is done digitally as well.

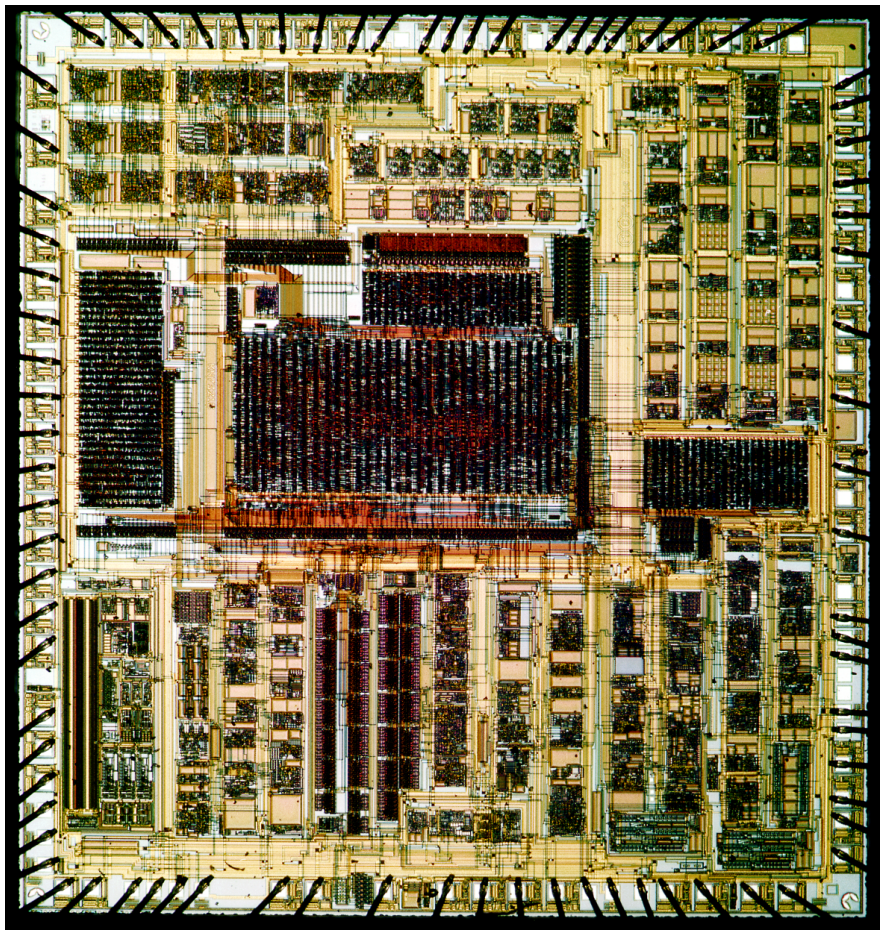


Fig. 14 TV processor IC for mid-range applications.

The processor shown in Fig. 14 contains all functions that are drawn within the dashed rectangle in Fig. 12. So this IC contains all signal processing functions (except the tuner, the microcontroller and the power stages) which are needed in a TV. The IC can be characterised as a system-on-silicon, with an analogue data path and a digital control path. All signal processing functions are performed by analogue circuits, whereas everything around the signal path is digital if possible. One of the reasons for that is that the IC has 25 adjustments and some 70 switches. If each of these adjustments and switches had to controlled via its own pin on the IC, that would require nearly 100 pins. That's why the IC is controlled by an I^2C bus [12]. This two-wire bus feeds all the adjustment and switching commands to the IC. This saves

a lot of hardware and makes the IC easily software controllable. Instead of 25 potentiometers the IC has 25 6-bit DACs to control all adjustments. The adjustments are for the adjustments of external components, like the picture tube, and to adjust user settings, like sound volume. All circuits in the IC are kept within their specified range by internal, automatic calibration circuits.

The IC of Fig. 14 is made in a BiCMOS process with a minimum line width of 0.6µm. It contains over 60,000 components on 27mm^2. The analogue circuits are made up of 18,000 components. The supply voltage is 8V and the total current consumption is about 140mA. More than 95% of this current is drawn by the analogue circuits. The digital circuits are predominantly low-frequency control circuits and consequently don't draw a lot of current.

In [13] one of this IC's forebears is described.

chapter 3

Integrator with a low unity-gain frequency

Introduction

In many IC applications there is a need for circuits with a low bandwidth. These circuits are needed for e.g. stabilisation of control loops and/or suppression of high-frequency signal components. This chapter describes a technique for making continuous-time low-unity-gain-frequency integrators. The long time-constants that are needed in such integrators are challenging to make in an IC, as the maximum size of integrated capacitors is in the pF range.

Integrators with low unity-gain frequencies have been described in e.g. [14]-[16]. However, these circuits operate at extremely low currents. The circuit in [16] operates at a bias current of only 300pA. Very small bias currents make circuits susceptible to leakage currents that may arise when processing problems occur in a foundry. Leakage is not normally a problem, but if an IC is susceptible to it, this can lead to low yield, or worse, scrapping of complete batches. But, as leakage increases with temperature, the leakage may well not be detected by the test program in the test factory. If an IC with a relatively high leakage current escapes detection by the test program, it may cause a failure of the system in which it is used. A way to prevent ICs with a high leakage current from escaping detection is to test at a high temperature instead of at room temperature. This is possible but costly, so if there is no absolute need for it, it should be avoided.

As leakage currents can lead to high costs, a research topic was defined to make an integrator with a low unity-gain frequency that has a very low sensitivity to leakage currents. To make the circuit insensitive to leakage currents, the bias currents were chosen well above the leakage current level. As this research was not aimed at a particular application, the outcome was going to be a solution in search of a problem.

The boundary conditions for the integrator were set as follows: total capacitance equal to 20pF (i.e. two anti-parallel connected capacitors of 10pF) and minimum bias currents in the transistors of the order of 1μA. With this lower limit on the bias current, the current level in the circuit is far above the level of the leakage currents in the process. A number of circuits with a low unity-gain frequency are proposed in which the effects of parasitics are addressed one by one to increase the DC gain of the integrator.

The design technique for the integrator circuit was verified in a voltage-controlled crystal quadrature oscillator, wherein it must keep the offset of two series-connected integrators at bay. From the proposed circuits one is adapted to fit the requirements of the oscillator.

Scope of this work

This work concentrates on continuous-time integrators for systems in which a clock is not available or undesirable (e.g. to prevent crosstalk of the clock frequency to the rest of the system). Discrete-time techniques like switched-capacitors [17] and switched-currents [18] have not been considered.

Continuous-time integrators

ideal integrator

Fig. 15 shows an ideal continuous-time integrator. The unity-gain corner frequency of this ideal circuit is:

$$\omega_{GB} = \frac{g_m}{C} \tag{2}$$

The DC gain of this ideal circuit is infinite.

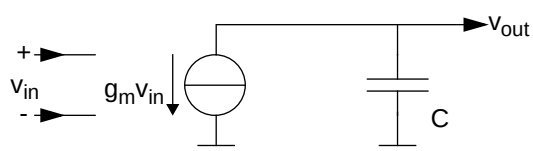


Fig. 15 Ideal integrator.

practical integrator

Practical continuous-time integrators can never have an infinite DC gain. There will always be (parasitic) impedances in the circuit that limit the DC gain. This can be e.g. a finite output resistance of the currents source, or a leakage in the capacitor. Fig. 16 shows the equivalent circuit of a practical integrator. The unity-gain corner frequency of this circuit is $\omega_{GB} = g_m/C$ (so

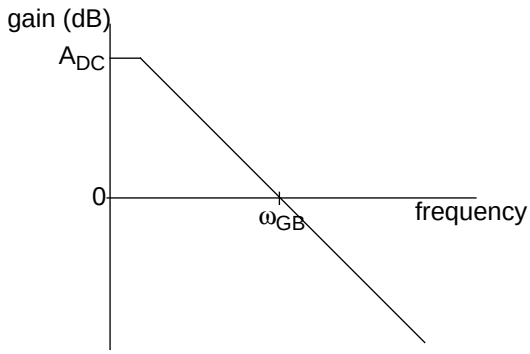


Fig. 17 Amplitude transfer characteristic of a practical integrator.

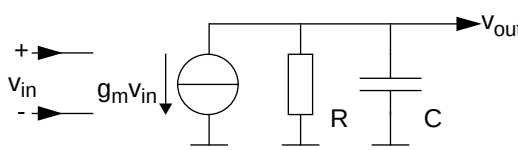


Fig. 16 Integrator with finite DC gain.

equal to that of an ideal integrator), the DC gain is:

$$A_{DC} = g_m R \tag{3}$$

Fig. 17 shows the amplitude transfer characteristic of a practical integrator.

Circuits for continuous-time integrators

From the above it follows that in order to obtain a lower unity-gain frequency, either g_m must be decreased or the capacitance must be increased. In the following some circuit techniques that can be used for integrators with a low unity-gain frequency are discussed.

Miller effect

A practical upper limit to the value of a capacitor in an IC is about 100pF. One way to get

round this is to electronically boost the value of a capacitor. A technique that is widely used to electronically boost the value of a capacitor is the Miller effect [19]. Fig. 18a shows a circuit that makes use of the Miller effect. The value of the capacitor is electronically enlarged by placing it in the feedback loop of an amplifier. This technique is widely used to stabilise amplifiers. The amplifier in Fig. 18 is then one of the stages of the amplifier that has to be stabilised. In Fig. 18b the effective value of the capacitor seen from the input is $C_{eff} = (1+A_M)C$. By making the gain A_M of the amplifier high it is easy to make extremely high effective values of the capacitor.

If the capacitor of an integrator is replaced by a capacitor that is boosted with the Miller effect, the unity-gain frequency will not change: both the apparent capacitance and the DC gain are increased by the same amount, so the gain-bandwidth product (which is identical to the unity-gain frequency) will remain the same. When the Miller effect is used to stabilise an amplifier, the capacitor is placed across one of the amplifying stages that is already present. So in such an application the capacitor value is boosted, but the total gain of the system is not increased.

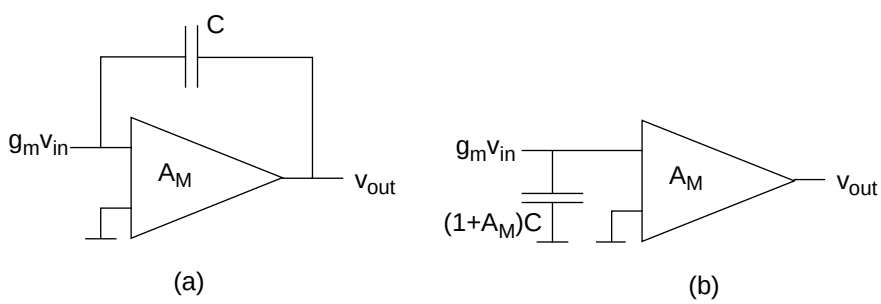


Fig. 18 Basic configuration of a circuit using the Miller effect (a) and its equivalent circuit (b).

active RC integrators

If the capacitor of an ideal integrator is replaced by a capacitor in the feedback loop of an amplifier the current source can be replaced by a resistor (Fig. 19). The input voltage is converted into a current as the resistor is connected to virtual ground. So the transconductance in this circuit is simply $g_m = 1/R_{int}$ [20].

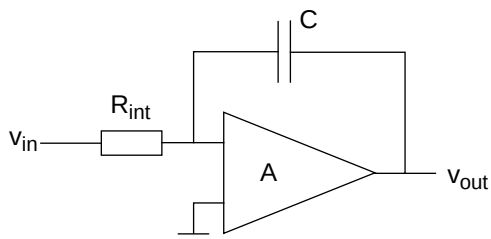


Fig. 19 Active RC integrator.

A low unity-gain frequency can be obtained with the circuit of Fig. 19 by increasing R_{int} to a very high value (for a given capacitance C). Like capacitors, resistors also have a practical upper limit. In a 0.6μm BiCMOS process [21] a resistor of more than 1MΩ is impractically large. Instead of resistors, MOS transistors can be used in the circuit of Fig. 19 [22]. A circuit with MOS transistors instead of resistors is shown in Fig. 20. This circuit is balanced to get rid of the non-linearity of the MOS transistors. A control voltage V_c is applied to the gates of the transistors to tune the circuit to the desired unity-gain frequency.

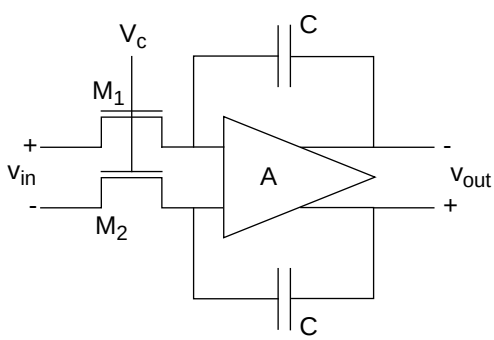


Fig. 20 Balanced integrator circuit with MOS transistors used in their linear region.

A disadvantage of the circuit of Fig. 20 is that the MOS transistors must be very long and/or have a low gate-source voltage to obtain a low transconductance value. This means that the maximum input voltage is rather limited. A way to get round this is to use the configuration of Fig. 21 [23]. Due to the cross coupling, the difference of the conductance of M_1 and M_3

(and their counterparts) determines the unity-gain frequency. Two different control voltages are used to control the conductances of the MOS transistors. So the resulting conductance can be low even with a moderate conductance in the MOS transistors. In [23] this circuit is used to improve the linearity with respect to that of the circuit of Fig. 20.

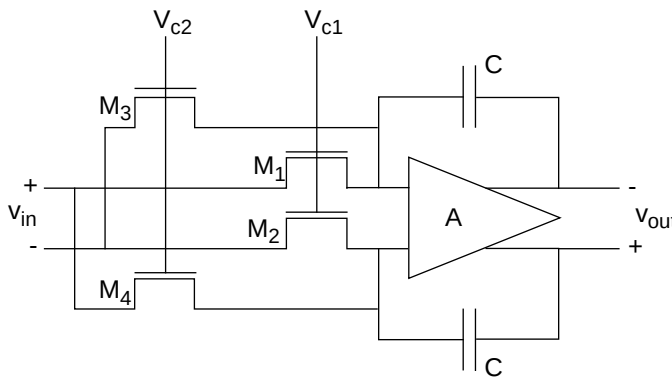


Fig. 21 Balanced integrator circuit with cross-coupled MOS transistors to reduce the transconductance.

transconductance-capacitance integrators

Fig. 22 shows a circuit in which the transconductor is a bipolar transistor.
The transconductance of the transistor is

$$g_m = \frac{1}{r_e} = \frac{qI_E}{kT} \tag{4}$$

In this equation, I_E is the bias current that flows through the transistor. So, to obtain a low

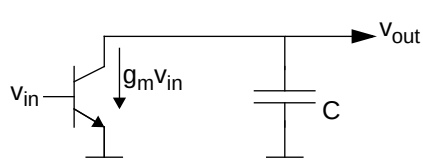


Fig. 22 Integrator with bipolar transistor as transconductor.

transconductance the bias current must be low.

Emitter degeneration can be used to make the transconductance of the circuit of Fig. 22 lower. Fig. 23 shows a balanced circuit in which emitter degeneration is applied. Although a low transconductance can now be obtained with a (relatively) high bias current, the circuit does have some drawbacks. A large resistor (or an equivalent circuit) is needed, and if the circuit is biased with a current that is far bigger than the maximum signal current that flows through the resistor, the modulation depth is very low. This is generally not good for the signal-to-noise ratio.

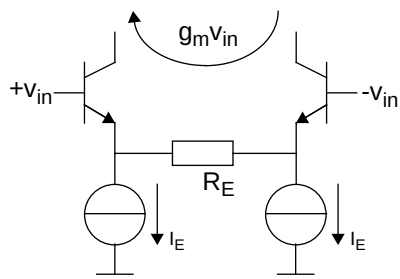


Fig. 23 Emitter degenerated transconductance amplifier.

A differential pair of MOS transistors has limitations similar to that of a bipolar transistor. But, with the same bias current the transconductance of a MOS transistor is always lower.

Making a low unity-gain frequency

With all the circuits described above it is challenging to make a really low unity-gain frequency. The circuit with the cross-coupled MOS transistors (Fig. 21) is limited by the mismatch of the MOS transistors. Circuits with transconductors are limited by the lowest bias current that can be used, without running into trouble with leakage currents.

In the following a circuit technique will be explored to alleviate the latter problem.

Low unity-gain frequencies and leakage currents

Transconductor-C integrators for very low frequencies usually operate at an extremely low current level. Examples of these are the circuits described in [14]-[16]. In [14] and [15] a MOS current mirror with a large attenuation is used to charge a capacitor. In [16] a bipolar current mirror with a very large attenuation drives a Miller integrator. The collector current in the output transistor of the current mirror in the latter circuit is just 300pA. The reason why these cir-

cuits operate at such low bias currents lies in the fact that the maximum value that an integrated capacitor can have is of the order of 100pF. The very low current is needed to make the low transconductance, which is needed to make an integrator with a low unity-gain frequency.

The absolute minimum current level at which a circuit with bipolar transistors can operate, in an IC with only perfect p-n junctions, is determined by the saturation[1] current of the (reverse biased) base-substrate diode of the lateral PNP transistors. The saturation current (due to minority carriers) depends on the doping profile of the base-substrate junction, the transistor dimensions and the temperature [24]. Typically this current will be below 1nA (at 125^{o}C) in a 0.6µm BiCMOS process [25]. However, due to imperfections in the p-n junctions (e.g. dislocations in the monocrystalline silicon) extra current may flow in the base-substrate diode. This current is due to so-called Shockley-Hall-Read (SHR) recombination [26]. This extra current with respect to the saturation current is called leakage current or I_{SHR} in this chapter.

If the impedance of the source that drives the transistor is very high I_S and I_{SHR} flow into the base and are amplified by the current gain factor α_e of the transistor (Fig. 24). If there are processing problems in the foundry (e.g. impurities at the surface that cause many dangling bonds: the shaded areas at the top-right and top-left of the NWELL in Fig. 24a), the value of I_{SHR} can be significantly higher than I_S. However, experience shows that if processing problems occur, in the majority of cases they cause collector currents below 10nA (at 125^{o}C) in minimum-size transistors in a 0.6µm BiCMOS process [25].

The leakage current of NPNs is generally much smaller than the leakage current of PNPs.

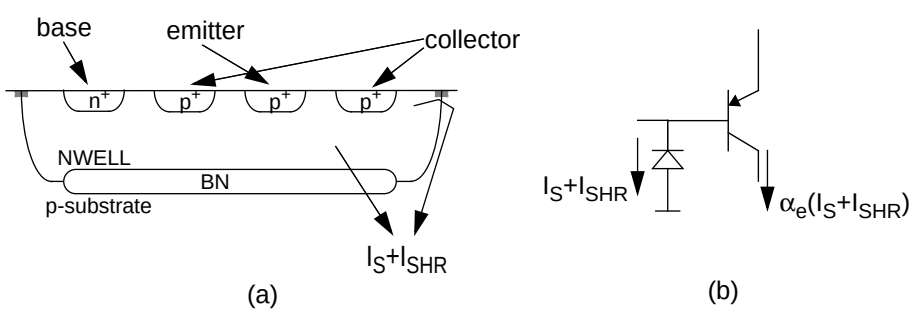


Fig. 24 (a) I_S and I_{SHR} flow from the base to the substrate. (b) I_s and I_{SHR} are amplified just like any other input current.

1. The term saturation current refers to the current in a reverse biased diode in this section. It does **not** refer to the current in a bipolar transistor that is driven into saturation. It also does **not** refer to the current in an MOS transistor driven with a very high gate-source voltage.

The I_S+I_{SHR} of an NPN originates in the collector-base junction and is amplified by the current gain of the NPN, just like in the case of the PNP shown in Fig. 24. If the bias current of the NPNs is delivered by PNPs, the PNPs' leakage current determines the minimum bias current of the whole circuit.

The minimum operating current of MOS transistors is mainly determined by their sub-threshold characteristic [27]. For minimum-size transistors in processes with very short channel length (<1µm) the leakage current can be well within the nA range (at 125°C) [28]. If the channel is made long enough the saturation current of the drain-to-well diode will become dominant in an ideal MOS transistor. Unfortunately processing wafers in a foundry is not always ideal. One of the many critical process steps is the field V_T implant (shaded area in Fig. 25). If something goes wrong with this implant the threshold voltage of the parasitic MOS transistor between the e.g. the drain and the substrate may become so low that a leakage current flows (I_{lkg} in Fig. 25). There are more effects that can cause leakage in an MOS transistor, but experience shows that in the majority of cases the total leakage current is below 5nA (at 125°C) for minimum-size transistors in a 0.6µm BiCMOS process [29].

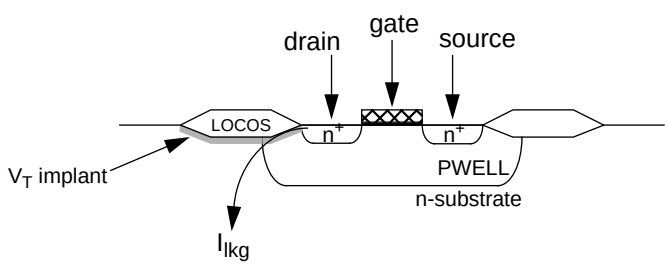


Fig. 25 Leakage current from the drain of an NMOS transistor to the substrate due to a wrong V_T implant.

Integrator with g_m reduction

A compact and simple way to reduce the transconductance of an arbitrary transconductor is shown in Fig. 26. The current is attenuated by the current gain factor, α_e, of a bipolar transistor [30][1]. For clarity Fig. 26 only shows the signal diagram. The bias components will be added at a later stage of the design process.

There are two ways in which the operation of the circuit can be understood. Seen from

1. In the late sixties/early seventies the basic idea of Fig. 26, to use the base of the transistor as the output node, was used in some circuit designs. Despite an extensive search of the literature no references from that (or any other) period could be found.

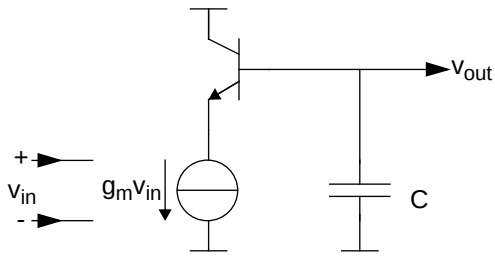


Fig. 26 Reducing the transconductance by current attenuation.

capacitor the transconductance is reduced by the current gain of the transistor. Seen from the source the capacitor is increased by the current attenuation factor of the transistor.

The unity-gain corner frequency of the circuit is:

$$\omega_{GB} = \frac{g_m}{\alpha_e C} \tag{5}$$

Assuming the current source output impedance is infinite, the DC gain is determined by the transconductance and the (parasitic) collector-emitter resistance of the transistor. This resistance is called the output resistance of the transistor in the design of current sources. As the collector is not the output in this circuit, the term collector-emitter resistance will be used to avoid confusion. The collector-emitter resistance r_{ce} of a transistor is dependent upon its Early voltage V_{EA} and its bias current I_C:

$$r_{ce} = \frac{V_{EA}}{I_C} \tag{6}$$

So the DC gain of the circuit is:

$$A_{DC} = \frac{g_m V_{EA}}{I_C} \tag{7}$$

This equation suggests that the DC gain of this circuit is higher when the bias current decreases. However, this depends on the type of transconductor that is used. E.g. a non-degenerated differential pair of bipolar transistors has a g_m that is proportional to the bias current. With such a transconductor the DC gain is independent of the bias current.

The DC gain of the circuit of Fig. 26 is equal to the DC gain of a circuit in which the collector of a bipolar transistor drives the capacitance (Fig. 22). However, the unity-gain fre-

quency of the circuit of Fig. 22 is a factor of α_e lower than the unity-gain frequency of the circuit of Fig. 26. Another way of putting this is to say that the circuit of Fig. 26 can be biased at an α_e higher current level to obtain the same unity-gain frequency.

Comparison with the Miller-effect circuit

One way of looking at the circuit of Fig. 26 is to see it as a capacitance booster. This is a function that the Miller-effect circuit of Fig. 18 also performs. As a consequence both circuits share many characteristics. There is, however, one big difference between the circuits. If the Miller-effect circuit is added to a system, the unity-gain frequency is determined by the physical value of the capacitor, not by the boosted value. This is due to the fact that all input current flows through the capacitor. If the circuit of Fig. 26 is added to a system, the unity-gain frequency is determined by the boosted capacitor value, not its physical value. This is due to the fact that only a part of the input current flows through the capacitor.

After the work presented in this chapter was finished, a circuit was proposed that uses the Miller effect, but in which the unity-gain frequency is determined by the boosted value instead of the physical value [31]. This is achieved by measuring the current to the capacitor and then feeding a part of this current to ground instead of through the capacitor.

Circuit implementation

The first step in moving from the prototype to a real circuit is to change the prototype into a balanced circuit (Fig. 27). Balanced circuits have a number of well-known advantages: suppression of even order harmonic distortion, robustness against substrate crosstalk. Also, it is easier to bias the circuit if it is balanced instead of single-ended.

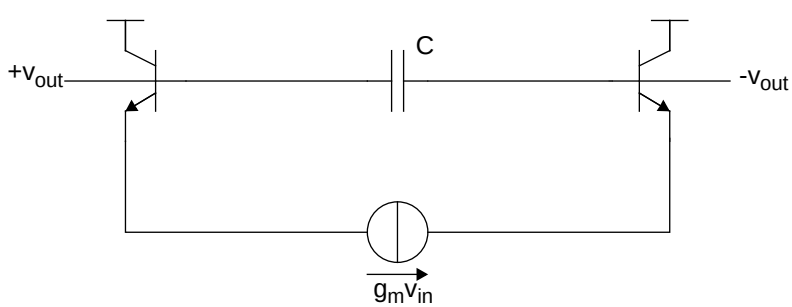


Fig. 27 Balancing the circuit.

In the following, all components of the circuit will be drawn, but only the components of one half of the circuit will be described. The analyses for these components are also true for their counterparts in the other half of the circuit. The only thing to remember, when calculating e.g. an impedance level or a time-constant, is to multiply (or divide) the result by two to get the correct answer for the balanced circuit. The equations below all have this factor of two already taken into account.

Up to now the signal path of the circuit has been described. The bias components will now be added. For the biasing part of the circuit the same criteria with respect to leakage hold true as for the signal processing part. Therefore the bias current that is fed to the base of the current attenuating transistors should also be flowing from a base. For a correct biasing this current must flow from the base of a transistor that is the complementary type of the transistor that is used for the signal attenuation. In the circuit diagrams shown so far NPN transistors are used in the signal path. This means PNP transistors have to be used in the bias circuitry[1]. Fig. 28 shows the basic biasing scheme. In the following circuit diagrams the components that have been added or changed with respect to the previous diagram will be shaded. Fig. 29 shows how the common-mode currents of the circuit of Fig. 28 are generated. A PMOS transistor pair T_4

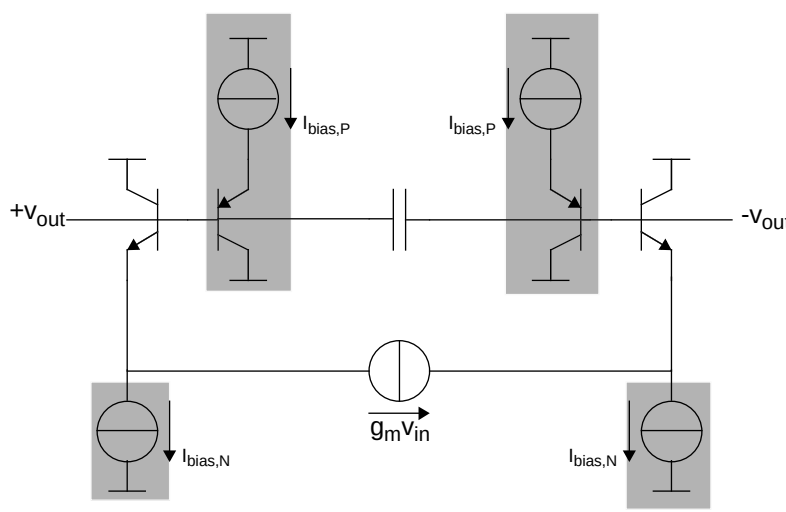


Fig. 28 Basic bias circuitry.

1. In this circuit, as in all electronic circuits, the N-components (i.e. NPN and NMOS) and P-components (i.e. PNP and PMOS) can be interchanged at will in the signal path. This will not affect the function of the circuit (though the specification will be affected due to the difference in parameters of both types of components), but only the bias conditions.

senses the voltage across the capacitor. The gate terminals of MOS components are used to sense the capacitor voltage as they have an extremely high-ohmic input resistance and don't suffer from leakage currents. The voltage on the common source node is the (level-shifted) common-mode voltage of the capacitor. This voltage is used to generate the input current of a current mirror that outputs the common-mode currents to the PNPs (T_3) that feed the bias currents to the signal attenuating transistors.

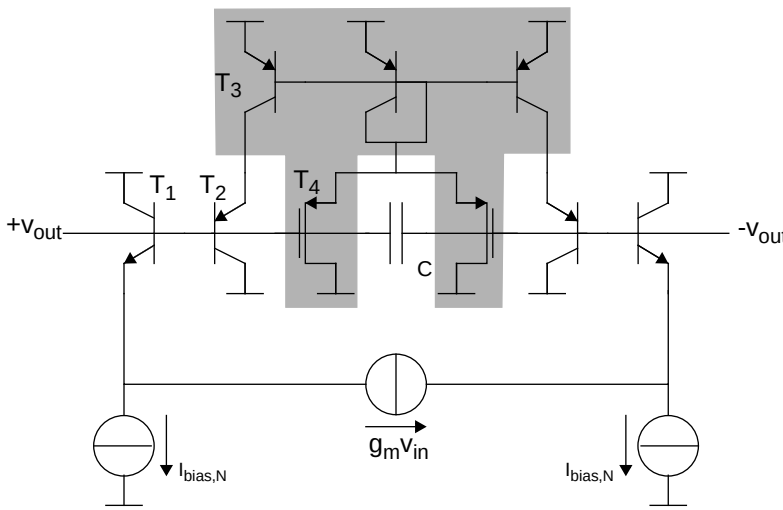


Fig. 29 The common-mode control circuit added.

influence of the bias components on the DC gain

The addition of the bias components does not affect the unity-gain frequency. The DC gain of the circuit, on the other hand, is reduced due to the bias components. The circuit has three parasitic resistive components that limit the DC gain. These parasitics are the collector-emitter resistances of T_1, T_2 and T_3. The DC gain of the complete circuit after the addition of the bias components has become:

$$A_{DC} = 2g_m\left(r_{ce1} \| \left(\frac{\alpha_{eP}}{\alpha_{eN}}(r_{ce2} \| r_{ce3})\right)\right) \tag{8}$$

Where α_{eN} and α_{eP} are the current gain factors of the NPN and PNP, respectively. If the NPNs are identical and the PNPs as well, an alternative way of writing equation 8 is:

$$A_{DC} = \frac{2g_m}{I_{C1}}\left(V_{EAN} \parallel \frac{V_{EAP}}{2}\right) \tag{9}$$

where V_{EAN} and V_{EAP} are the Early voltage of the NPN and PNP, respectively.

An observation that can be made in equation 9 is that the current gain of neither the NPN nor the PNP is a determining factor for the DC gain.

Suppose the input current is delivered by a non-degenerated differential pair of ideal bipolar transistors with a tail current of 2µA, so g_m = 20µS (i.e. 1/(50kΩ)). Then, with a circuit made in a 0.6µm BiCMOS process [21] (Table 3) and using a 20pF capacitor, the unity-gain frequency f_{GB} = 1.2kHz and the DC gain A_{DC} = 54dB.

α_{eN}	130 (10nA<I_C<100µA)
α_{eP}	35 (10nA<I_C<10µA)
V_{EAN}	60V (V_{CB}=0V)
V_{EAP}	30V (V_{CB}=0V)
poly-poly capacitance	1600pF/mm^2

Table 3 Parameters of the 0.6µm BiCMOS process [21] (room temperature).

Simulation results

To check the calculation a simulation was run on the circuit of Fig. 29. The capacitor in the circuit has a value of 20pF, but is in fact an anti-parallel connection of two poly-poly 10pF capacitors. This is to keep the circuit well-balanced: both terminals of the total capacitor have the same bottom-plate-to-substrate capacitance. In the simulation the transconductor is an ideal differential pair of bipolar transistors. The tail current of this pair was varied to check its influence on the unity-gain frequency and the DC gain. Fig. 30 shows the results.

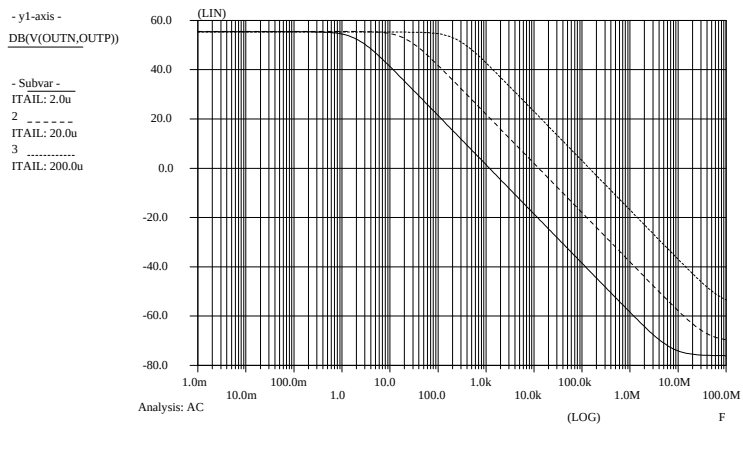


Fig. 30 Simulated transfer of the circuit of Fig. 29 for three different bias currents.

As expected Fig. 30 shows that the influence of the bias current on the DC gain is very low, while the unity-gain frequency varies nearly linearly with the tail current.

Common-mode loop

The circuit has the desired low unity-gain frequency and a high DC gain, but this can only be exploited if the whole circuit is stable. As the circuit contains a common-mode control loop, it is important to make sure that this loop is always stable. When analysing the circuit it is easy to see that the common-mode loop has one dominant pole located on the gate node of T_4. On the gate node the impedance is very high as only bases and the gate are connected to it. The other nodes in the loop are connected to emitters and will therefore have a far lower impedance. On the gate of T_4 there is also a (relatively) large capacitance to ground, mainly due to the bottom-plate parasitic of capacitor C. As the capacitor is connected across the differential output node of the circuit, it will not influence the stability of the common-mode loop. Only its parasitics to ground, which are of the order of 10 per cent of the capacitor itself, will influence the stability. In case the circuit would prove to have stability problems with the common-mode loop, capacitor C might be (partly) split up in two series capacitors (instead of two parallel capacitors), with the central node connected to ground. Fig. 31 shows that the stability of the common-mode loop of Fig. 29 is good enough with the two parallel capacitors for both high and low bias currents.

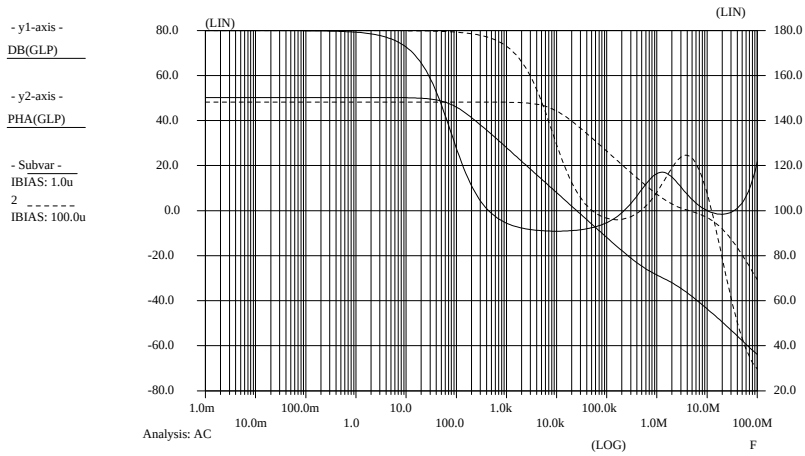


Fig. 31 Simulated Bode plot of the open-loop behaviour of the common-mode loop.

Noise performance

The basic operating principle of the presented circuit is attenuation of the input signal. Because of this it is to be expected that its signal-to-noise ratio is not its strongest feature. In a worst case scenario one might fear a deterioration of the signal-to-noise ratio of a factor equal to the current attenuation factor. The circuit of Fig. 29 (without the capacitor) can be regarded as an active load resistor of the transconductor. In appendix A it is simulated that the circuit of Fig. 29 generates 29dB more noise than an equivalent passive load resistor. Although this is substantially lower than the current attenuation factor (i.e. 130, or 42dB), it is certainly too high to call the circuit low-noise.

Increasing the DC gain of the integrator

To increase the DC gain of the integrator to a value which is as high as possible, the influence of the three collector-emitter resistances in equation 8 must be eliminated.

elimination of the influence of the collector-emitter resistance of T_3

Starting with the easiest one: T_3. This current source's output impedance can be increased by either emitter degeneration or cascoding. Cascoding is preferred, as the current in T_3 is very small. This implies that very high resistor values are needed for emitter degeneration to have

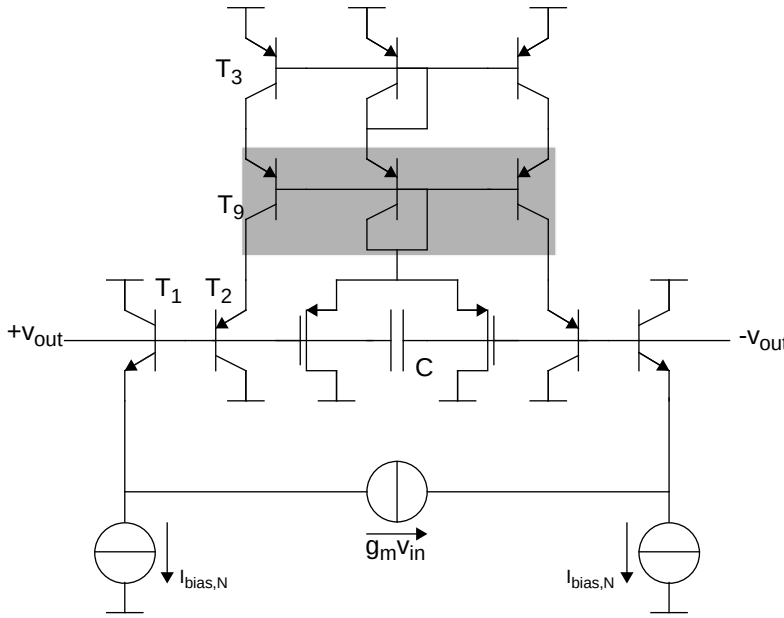


Fig. 32 Cascoding the current sources.

any effect. Fig. 32 shows the circuit diagram.

elimination of the influence of the collector-emitter resistance of T_2

Next the influence of T_2 will be addressed. Eliminating the influence of the Early effect always implies that some way must be found to keep the collector-emitter voltage of the transistor, that is suffering from it, constant. Looking at Fig. 32 an elegant solution for the elimination of the influence of the Early effect of T_2 is to see T_1 as an emitter follower between the output and the input of the circuit. By connecting the collector of T_2 to the emitter of T_1, the collector-emitter voltage of T_2 is kept constant (Fig. 33). As the collector current of T_2 is now delivered by the bias current source that also biases T_1, the bias current in T_1 will be lowered somewhat. If the bias current $I_{bias,N}$ remains the same, the lower bias current through T_1 will lead to an extra increase of the DC gain.

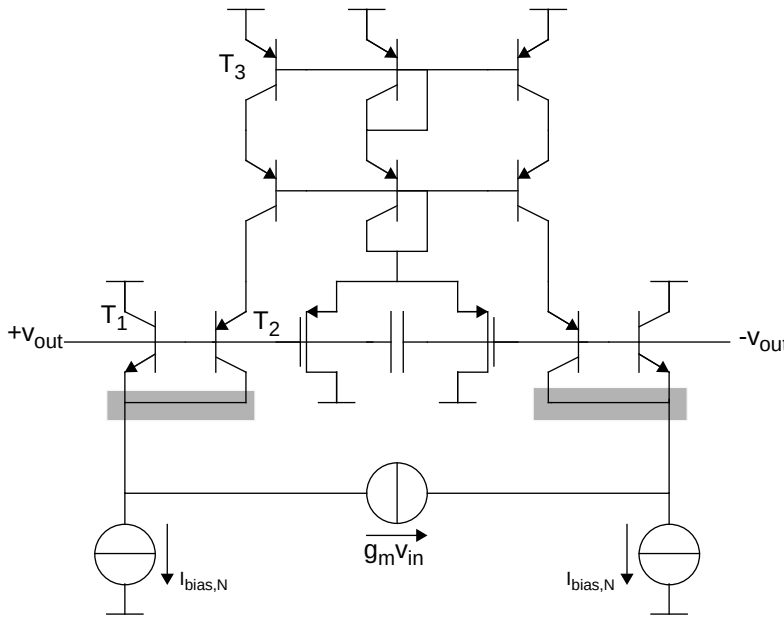


Fig. 33 Eliminating the influence of the collector-emitter resistance of T_2.

elimination of the influence of the collector-emitter resistance of T_1

It may seem attractive to eliminate the influence of the Early effect of T_1 in a fashion similar to that of T_2 as shown in Fig. 34a. However, here the trick doesn't work. The reason for that is that the input current has no closed path in which it can flow, except through the capacitor. Neither the loop with T_1 and T_2, nor the DC current sources can take up the signal current.

An effective way to eliminate the influence of the Early effect of T_1 is shown in Fig. 34b. In this circuit T_6 keeps the collector-emitter voltage of T_1 constant by bootstrapping it. T_6 is not a cascoding transistor, because its base is not connected to (signal) ground, but to the emitter of T_2, which carries the output signal itself. There is still some signal current flowing through T_2 in this circuit, but because it is now only the base current of T_6 its influence on the DC gain is negligible compared to the elimination of the influence of r_{ce1}.

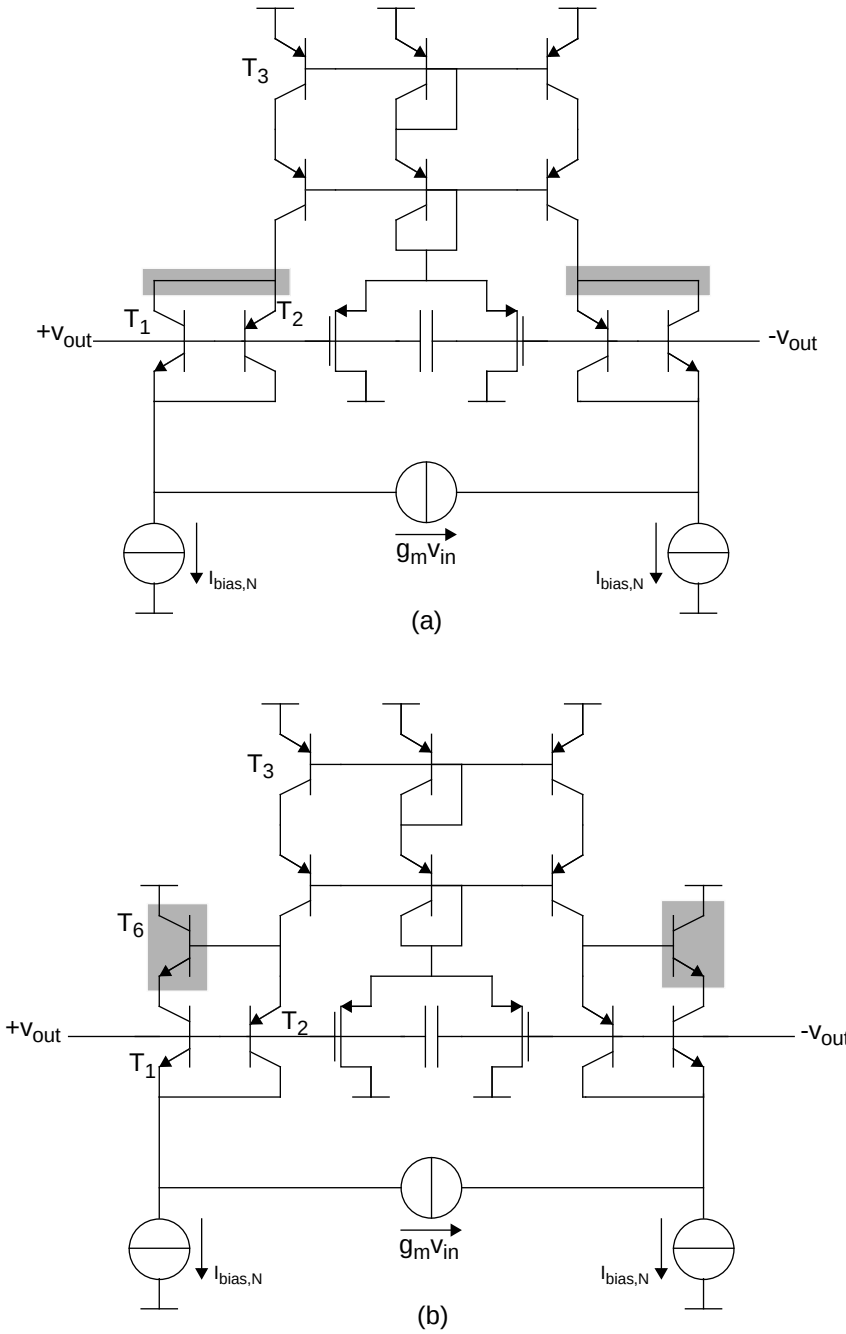


Fig. 34 Incorrect way (a) and correct way (b) to eliminate the influence of the collector-emitter resistance of T_1.

Simulation results

Table 4 lists the DC gain of the circuits discussed above. The transconductor is the same as in the previous simulation. The tail current was set to 2µA.

circuit	DC gain
Fig. 29	55dB
Fig. 32	61dB
Fig. 33	72dB
Fig. 34b	86dB

Table 4 Simulated DC gain of the circuits described above.

Verification of the integrator design

The design technique for the integrator described above was verified in a one-pin voltage controlled crystal oscillator (VCXO). This oscillator is an existing design [32], whose performance is good, but which would need an external capacitor (or an impractically large integrated capacitor and/or resistor) to stabilise an internal DC control loop. The offset cancellation circuit has to cancel the offset of two series-connected (high-frequency) integrators. To make sure the overall loop will not oscillate, the offset cancellation circuit must have a very low unity-gain frequency.

In the following section the oscillator design will be briefly discussed. The oscillator is part of the colour demodulator (see chapter 2). It oscillates at the colour subcarrier frequency.

The oscillator design

Fig. 35 shows the block diagram of the oscillator. The oscillator is a one-pin voltage controlled crystal oscillator. This means only one pin of the crystal is connected to the oscillator, the other pin is connected to ground.

Many one-pin crystal oscillators designs e.g. [33] produce square wave output signals of a fixed frequency. An example of an application of such oscillators is the generation of a stable system clock in VLSI systems. The application in which this oscillator is used, however, requires sinusoidal output signals and a slightly variable frequency. The reason why there is a need for frequency control is that the oscillator is part of a PLL, so it must be able to tune to the incoming frequency (see also the description of the analogue PAL/NTSC colour demodulator in chapter 4). The reason why the oscillator must produce a sine and a cosine is that the

system in which it is used needs quadrature signals whose phase can be varied with respect to the input signal. By adding the sine and cosine with different weight factors it is easy to change the phase. The phase shifting circuit is not part of the oscillator. The phase shifting circuit performs the hue control in case of NTSC reception (see chapter 2).

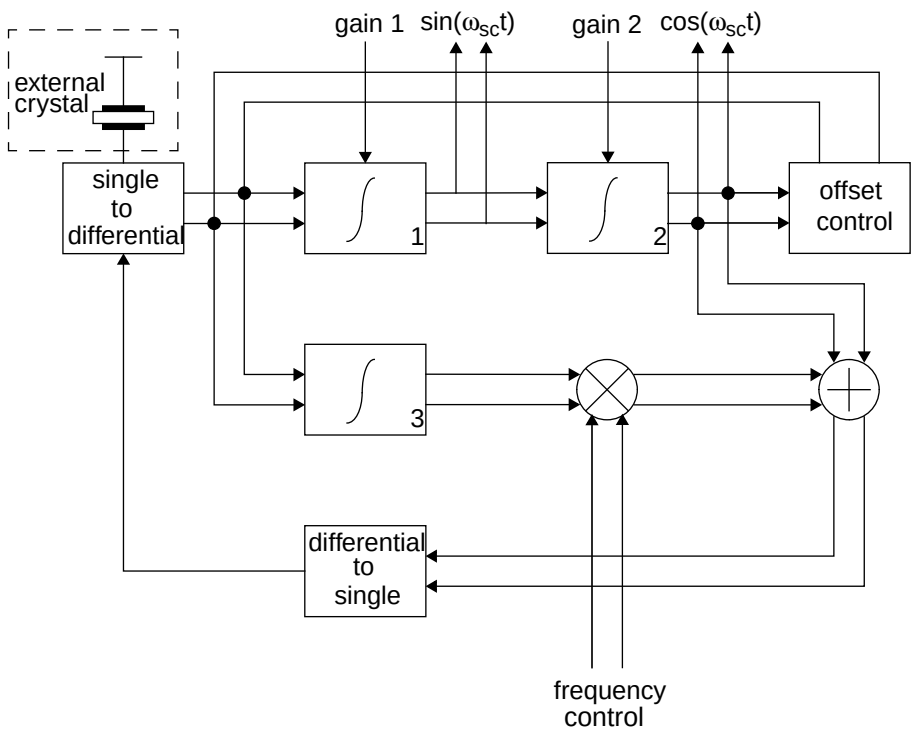


Fig. 35 Block diagram of the voltage controlled crystal oscillator.

Internally all oscillator signals are differential. As only one pin of the crystal is connected to the oscillator, the signal is fed to the crystal by a differential-to-single converter and taken from the crystal by a single-to-differential converter. The output signal of the single-to-differential converter is fed to two integrators (1 and 3). Integrator 1 is connected to another integrator (2), integrator 3 to a multiplier. The output of integrator 2 and the multiplier are added and fed back to the crystal through the differential-to-single converter. If the signal on the frequency control input is changed, the amount of the output signal of integrator 3 that is added to the output signal of integrator 2 changes. This causes a change of the phase of the output signal of the adder. As a result of this, the oscillator will move to a slightly different oscillation fre-

quency, as the conditions for oscillation must be maintained.

All three integrators have a twofold job: phase shifting to allow detuning of the crystal and suppression of harmonics of the crystal to guarantee oscillation at the correct frequency. The two series-connected integrators provide the quadrature output signals of the oscillator. These connect to the multipliers that perform the quadrature demodulation of PAL and NTSC signals.

The oscillator has three control inputs. One (differential) input controls the oscillation frequency (terminal “frequency control” in Fig. 35). The two other inputs control the gains of the two series-connected integrators (terminals “gain 1” and “gain 2” in Fig. 35). As there is only one frequency present in the oscillator (the crystal frequency), the gain control circuits to which integrators 1 and 2 are connected, will automatically adjust them to have a gain of one at this frequency.

The oscillator generates both a sine and a cosine output signal. The differential output amplitudes are $500mV_{pp}$.

Offset in the oscillator

Fig. 36 illustrates why the output signals of the oscillator must have a very low offset. The outputs of the VCXO are connected to two multipliers. The output signals of these two multipliers are the demodulated PAL/NTSC colour difference signals. Offset on the input of the multipliers causes a direct feedthrough of the colour carrier frequency (ω_{sc}) to the outputs. In Fig. 36 the sine output signal of the oscillator is assumed offset-free, while the cosine output signal has an offset u_{os}. In the offset-free sine path, the output of the multiplier only contains the low-frequency demodulated signal and a signal at two times the colour carrier, that can be eliminated by a low-pass filter at the output of the multiplier (not drawn in Fig. 36). Due to the offset, the output signal of the cosine path also contains a term with the incoming modulated signal itself.

maximum allowable offset on the output signals of the oscillator

The maximum offset that is allowed in the system is determined by the maximally allowable amount of residual carrier in the output signal. According to the system specification the residual carrier on the output must be smaller than $5mV_{pp}$ [34]. The carrier is attenuated by a factor of ten (worst case) in the third order low-pass filter and buffer amplifier which follow the multiplier (these are not shown in Fig. 36). The residual carrier might be eliminated by a higher order low-pass filter, but this would cost extra area and increase the group delay of the filter. Extra group delay in the colour difference paths must be compensated in the luminance path (by yet another filter) to make sure that the luminance and colour difference signals arrive

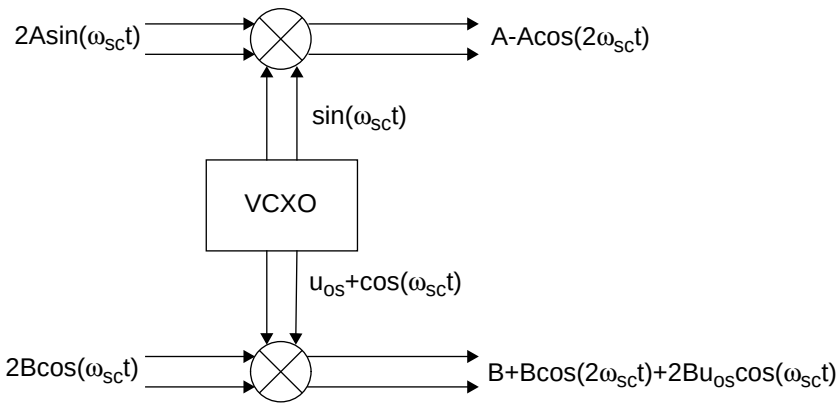


Fig. 36 Effect of offset in the oscillator output signals in a simplified colour demodulator.

synchronously at the stage where they are converted to RGB signals.

Offset on both the input signal and the oscillator signal are allowed an equal contribution to the residual carrier on the output. This implies that the amplitude of the term $2Bu_{os}\cos(\omega t)$, which is caused by offset on the oscillator signal, must be lower than $2.5mV_{pp}$ (i.e. maximum residual carrier amplitude divided by two) for the maximum input signal. The maximum input signal is $660mV_{pp}$, so the peak amplitude $2B = 0.33$. From this it follows that the maximum allowable offset on the oscillator outputs is $u_{os} < 7.5mV$.

The single-to-differential converter

Crystal oscillators can be made to oscillate at either the parallel or series resonant frequency of the crystal. A full explanation of these oscillation modes is beyond the scope of this work. Please refer to [35]. The specification of the oscillator demands that it oscillates at the series resonant frequency of the crystal [32].

The fact that the oscillator must oscillate at the series resonant frequency of the crystal has a major implication for the design. Due to it, it is not possible to keep the offset in the oscillator below the specified value by good design of the oscillation loop, because the oscillation loop has no DC transfer path. The main oscillation loop in the oscillator, which is formed around the two series-connected integrators, is not closed differentially. It is closed through a differential-to-single and a single-to-differential converter. This is a consequence of the fact that the oscillator must be a one-pin oscillator.

Fig. 37 shows the circuit diagram of single-to-differential converter. The input signal v_{in} is the sinusoidal signal from the output of the differential-to-single converter. T_1 passes the full input signal amplitude on to the base of T_2. However, the signal amplitude at the base of T_3 is very low, as the impedance of the crystal is very low at its series resonant frequency. This configuration forces the crystal to oscillate at its series resonant frequency.

As the base of both T_2 and T_3 are driven from the emitter of T_1, there is no DC transfer from v_{in} to i_{out}. If the base of T_2 were connected to a signal ground, instead of the emitter of T_1, there would be a DC transfer, but then the crystal would resonate at its parallel resonant frequency (the frequency at which the impedance of the crystal is very high).

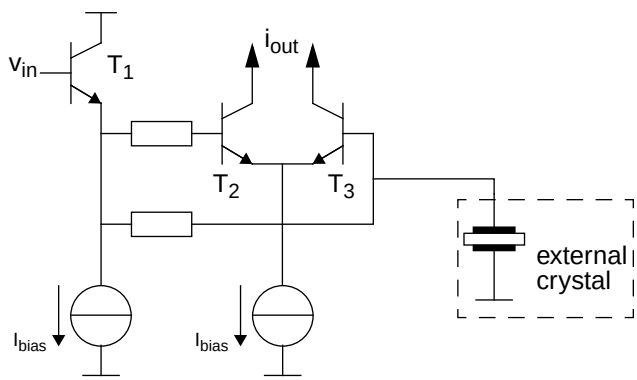


Fig. 37 Single-to-differential converter.

Eliminating the offset in the oscillator

As there is no DC transfer through the differential-to-single and single-to-differential converters, it is not possible to keep the DC offset in the main oscillation loop small through the feedback of the loop itself. It is necessary to have some form of offset cancellation, because the integrators have a DC gain of about 30, so the two integrators is series have a gain of nearly 1000. So even the smallest offset in the single-to-differential converter or integrator 1 (Fig. 35) would cause a very big offset at the output of integrator 3. Therefore the output of integrator 3 is sensed by an offset cancelling circuit. This circuit must comprise a low-pass filter, to get rid of the oscillation frequency (3.6MHz or 4.4MHz). The remaining DC component is fed back to the input of the first integrator. This way the loop will have a low offset on all integrator outputs. But, the low-pass filter adds a third pole in the loop with the two integrators. The oscilla-

tion loop must follow the oscillation produced by the crystal and not oscillate on its own. So, to safeguard stability, the unity-gain frequency of the offset cancelling circuit must be very low. Its unity-gain frequency must be well below:

$$f_{GB} < \frac{f_{osc}}{loopgain} \tag{10}$$

If this condition is met, the system will have 6dB/octave slope at the frequency where the gain is one. The two-integrator-plus-offset-cancellation-circuit loop then behaves like a first order system, so it is inherently stable.

The time-constant of the two integrators in the offset cancelling loop is controlled by a circuit that keeps the gain of these integrators exactly one at the oscillation frequency. If the control circuit is starting up the unity-gain frequency can be a factor of two lower than during normal operation, which is 2MHz worst case [32]. The offset control loop must, of course, also be stable in this situation. The above means that the cut-off frequency of the low-pass filter must be well below 2kHz. If the offset control circuit itself has a DC gain of more than one, its gain-bandwidth product must be less than 2kHz.

The oscillator is embedded in a family of analogue signal processing ICs that do not all have a clock. Because of fear of interference from a clock to the analogue circuits, it was decided to use a continuous-time (i.e. clockless) offset cancellation circuit. Without this boundary condition e.g. a switched-capacitor circuit might have been used. The oscillator frequency itself could be the clock frequency for such a circuit.

The IC family is made in a 1µm BiCMOS process [36]. The most important process parameters, for the minimum-size transistors, are listed in Table 5.

α_{eN}	150 (10nA<I_C<300µA)
α_{eP}	60 (10nA<I_C<1µA)
V_{EAN}	40V (V_{CB}=0V)
V_{EAP}	25V (V_{CB}=0V)
poly-metal capacitance	1100pF/mm^2

Table 5 Parameters of the 1µm BiCMOS process [36] (room temperature).

Making a cut-off frequency of 2kHz with a 10pF capacitor requires an 8MΩ resistor. This is a very high value for an IC. Therefore it was decided to use the circuit described above to make the offset control. The circuit of Fig. 29 will be used as a starting point.

The offset cancellation circuit

Fig. 38 shows the offset cancellation circuit that was derived from the circuit in Fig. 29. The part that is identical to Fig. 29 is within the shaded rectangle.

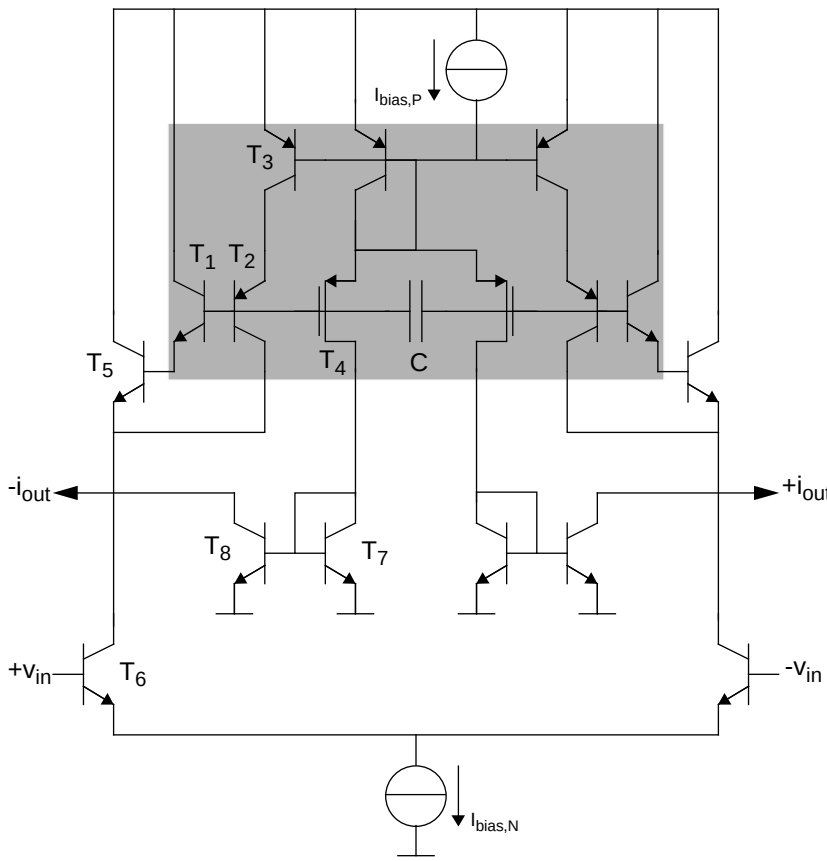


Fig. 38 Offset cancellation circuit.

the input stage of the offset cancellation circuit

The output voltage of integrator 2 (Fig. 35) is converted to a current by a differential pair (T_6). According the spec derived above, the offset must be lower than 7.5mV. With both bipolar and MOS transistors this is attainable. However, as the offset of bipolar transistors can easily be much lower than this value, while with MOS transistors this value can only be attained

with a careful design/layout, bipolar transistors were selected for the input stage.

The linear input range of the input amplifier is lower than the maximum input voltage ($500mV_{pp}$). This is not a problem for the function of this circuit as only the DC content of the input signal is important. To make sure the system is always stable, the following calculations use the worst case value of the transconductance.

the unity-gain frequency of the offset cancellation circuit

The oscillator has an NPN bias rail to which a number of current sources of 200µA are connected. Using a tail current of 200µA in the input stage (i.e. $g_m = 2mS$) a unity-gain frequency of $f_{GB} = 2kHz$ requires a capacitor of 1061pF in the circuit of Fig. 29. This value is too large for practical purposes. However, if a Darlington configuration is used, a capacitor of only 7pF is needed. The bias current in T_1 is 0.7µA in this circuit, so it is still very much higher than the leakage current level.

In the layout the capacitor is split up in two anti-parallel capacitors, so that the circuit stays well-balanced. When the layout was made both capacitors were enlarged to 6pF (giving a total of 12pF) as there was some room left in the layout. This way the stability of the loop will be extra robust against process spreads.

DC gain of the offset cancellation circuit

With the input amplifier and the darlington pair connected to the capacitor the DC gain of the circuit becomes:

$$A_{DC} = \frac{1}{r_{e6}}\left(\left(\frac{\alpha_{eP}}{\alpha_{eN}^2} r_{ce3}\right) \parallel \left(\frac{r_{ce1}}{\alpha_{eN}} \parallel (r_{ce5} \parallel r_{ce6})\right)\right) \tag{11}$$

This equation can be simplified by realising that the current through T_5 and T_6 is the same, so their collector-emitter resistances are the same. On top of that the current in T_1 is α_{eN} times lower than the current in T_5. So its collector-emitter resistance will be α_{eN} times higher. With this input equation 11 can be rewritten as:

$$A_{DC} = \frac{1}{r_{e6}}\left(\left(\frac{\alpha_{eP}}{\alpha_{eN}^2} r_{ce3}\right) \parallel \left(\frac{1}{3} r_{ce5}\right)\right) \tag{12}$$

Or alternatively in large signal quantities:

$$A_{DC} = \frac{1}{r_{e6} I_{C6}}\left(V_{EAP} \parallel \left(\frac{V_{EAN}}{3}\right)\right) \tag{13}$$

Or:

$$A_{DC} = \frac{V_{EAP} \parallel \frac{V_{EAN}}{3}}{\frac{kT}{q}} \tag{14}$$

So the DC gain of the offset cancellation circuit is A_{DC} = 345 (51dB).

the output stage of the offset cancellation circuit

The voltage on the capacitor must be converted to a differential current that can be added to the current of the differential amplifier that acts as the single-to-differential converter. As the common-mode DC voltage on the capacitor can vary quite a lot with temperature and process spreads, the current is fed to the output of the single-to-differential converter by a current mirror (T_7 and T_8) that is connected to the ground rail. This way the DC voltages in the offset control circuit and the oscillator can never cause saturation of the bipolar transistors. The voltage on the capacitor is sensed by a PMOS differential pair (T_4). This differential pair also acts as the input stage of the common-mode feedback loop. Bipolar transistors cannot be used for this function, because they would lower the impedance on the time-constant-making nodes.

The single-to-differential converter of the crystal oscillator is a differential pair of bipolar transistors with a tail current of 100µA. The tail bias current in the PMOS differential pair (T_4) was chosen 10µA. With this current value the DC bias at the output of the single-to-differential converter is only marginally upset. But, as the load resistance of the single-to-differential converter is 4kΩ, the offset control circuit can compensate for an input offset voltage on the first integrator up to +/-40mV ($I_{tail,PMOS}$*R_{load}). Offset on the input of the differential pair that makes up the single-to-differential converter would have to amount to 5mV, before the current in the PMOS transistors is too small to compensate for it. A differential pair of identical bipolar transistors will seldom show more than 2mV offset [36]. The single-to-differential converter has no circuit connected to its inputs that can aggravate its own offset (Fig. 37).

The PMOS differential pair (T_4) that senses the voltage on the capacitor, is the same pair that is used for the common-mode control circuit. But, as the common-mode control circuit generates only a small current in the PMOS transistors (less than 1µA), an extra 10µA current source ($I_{bias,P}$) connects to their sources. The gain in the offset compensating loop is more than 100dB. This is more than sufficient to get a small offset.

The capacitor value calculated before was calculated with nominal process parameters and for one temperature. Process and temperature variations cause a lot of spread on the parameters in the circuit. The gain of the transistors can spread by a factor of 1.5, the capacitor value by a factor of 1.3, the currents by a factor of 1.3. To create more than enough phase and gain

margin for even the very worst case scenario, the gain of the buffer with T_4, T_7, and T_8 and the load resistors of the single-to-differential converter was set to 0.1.

Simulation results

Fig. 39 shows the simulated transfer of the offset control circuit from the input of the voltage-to-current converter (T_6) to the output of the current mirrors (T_7 and T_8), with a 4kΩ load. Fig. 40 shows the open loop response of the two-integrators-plus-offset-control-circuit in the complete oscillator. Fig. 40 shows that the phase margin of the offset control loop is 65^o. This is more than enough to ensure stability under all circumstances. It can also be seen that the gain margin of the circuit is 92dB. This staggering gain margin is caused by the fact that the offset control circuit has an (unintentional) zero near the frequency where the integrators have their pole. This zero is caused by the fact that for high frequencies the current will flow through the base-emitter capacitance of T_1, so the attenuation of the intrinsic transistor is bypassed. But, even if this zero were not present the gain margin would be very high. The bold dashed line drawn in Fig. 40 is the phase response in absence of the zero. Even with this phase response the gain margin is in excess of 20dB.

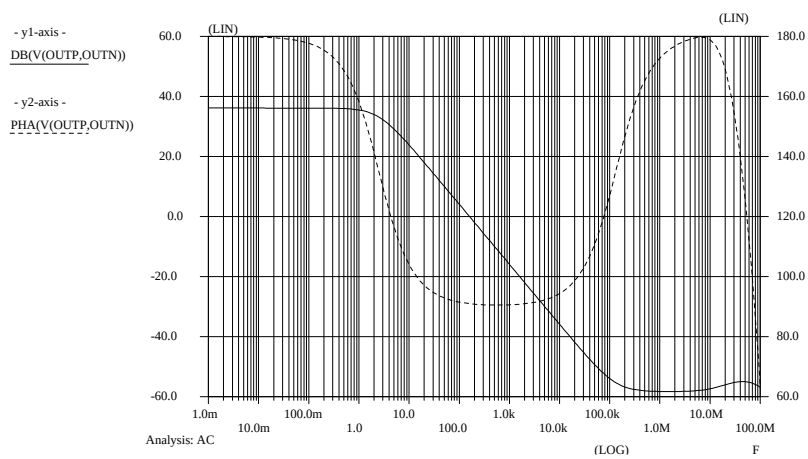


Fig. 39 Simulated open loop transfer of the offset cancellation circuit.

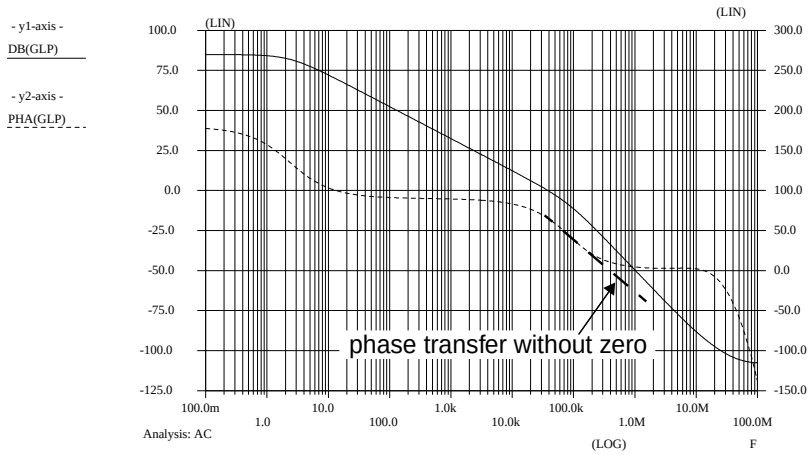
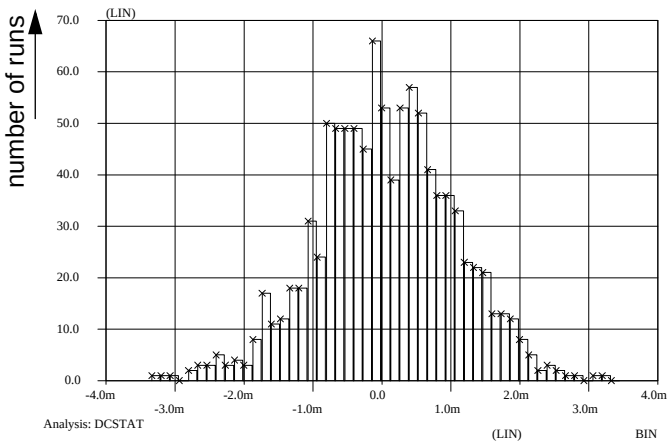
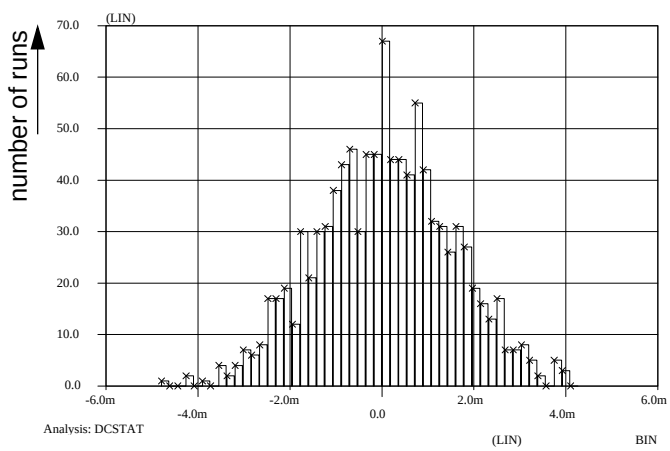


Fig. 40 Bode plots of loop with two integrators and offset control circuit.

The above simulations show that the circuit is always stable, but give no indication about the circuit's primary function: keep the offset at the outputs of the oscillator low. To check this, a statistical simulation was run. In this simulation all parameters are varied statistically according to the actual spread that is found in the waferfab that runs this process [36]. This statistical data includes mismatch performance of the process. Without this it would, of course, be impossible to find the expected offset in the circuit. Fig. 41 shows the offset voltage distribution for both (90^o phase shifted) outputs of the oscillator. For both outputs the offset stays below 5mV, even for worst case ICs. This well below the specified value of 7.5mV.



(a)



(b)

Fig. 41 Monte Carlo simulation (1000 runs) of the offset voltage distribution of (a) first integrator, (b) second integrator.

To check whether the circuit can easily eliminate the offset, or whether in some ICs it is only just capable of feeding enough offset correction current to the output of the single-to-differential converter, the modulation depth of the current through T_8 and its counterpart was observed. The modulation depth is 1 when all current flows through T_8. The modulation depth is -1 when all current is flowing is through T_8's counterpart. If the modulation depth

approaches 1 or -1, the circuit clips and can no longer cancel the offset voltage. As can be seen in Fig. 42, even in the very worst ICs the modulation depth stays below 0.7.

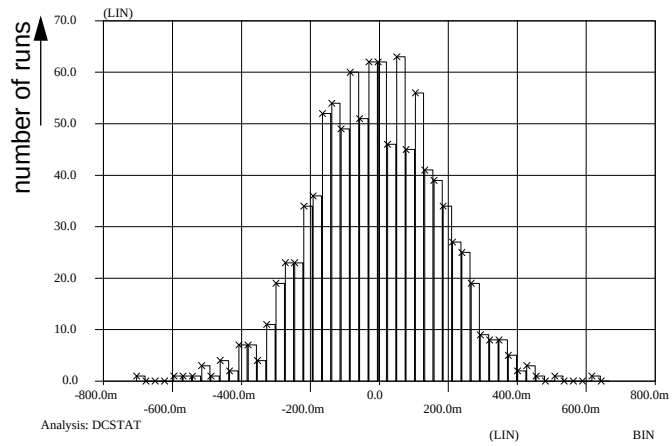


Fig. 42 Monte Carlo simulation (1000 runs) of the modulation depth in the output current mirror of offset control circuit.

The oscillator including offset cancellation circuit

Fig. 43 and Fig. 44 show the circuit diagram of the crystal oscillator, including the offset control circuit. The circuit parts as shown in the block diagram are indicated. The bias circuit on the left-hand side of Fig. 43 generates both DC currents and DC voltages. The DC bias voltages are generated to make the oscillator robust against supply voltage variations.

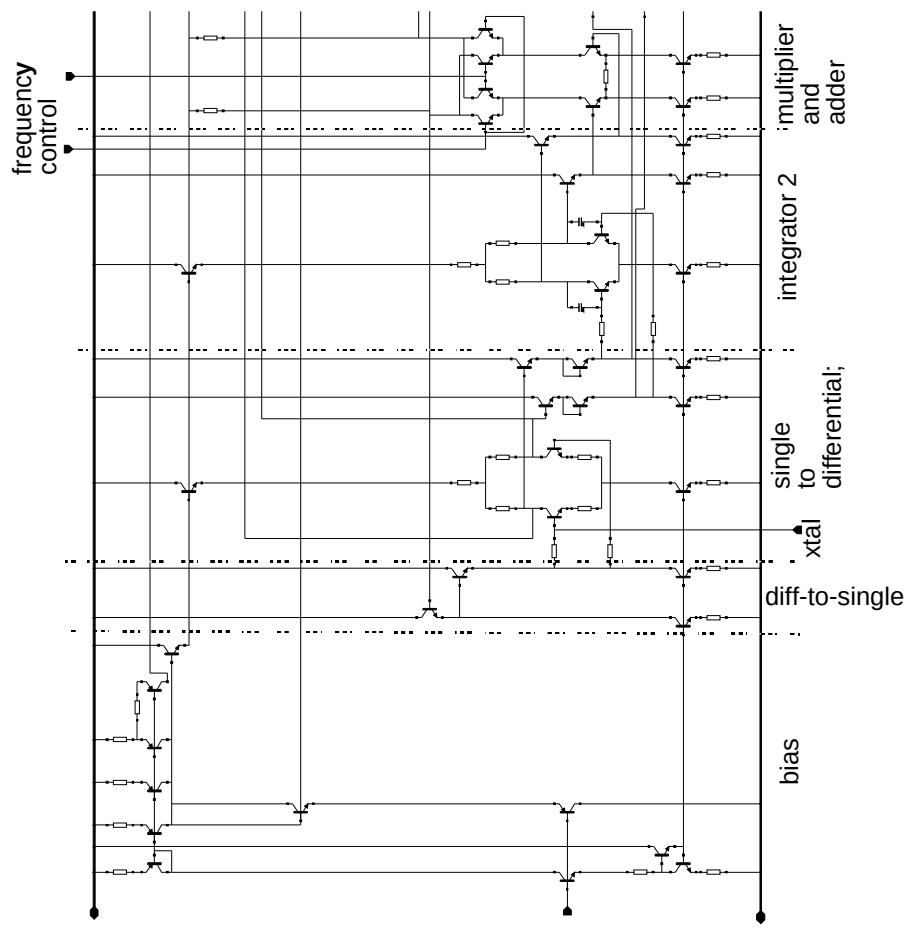


Fig. 43 Circuit diagram of the crystal oscillator with offset cancellation (part 1).

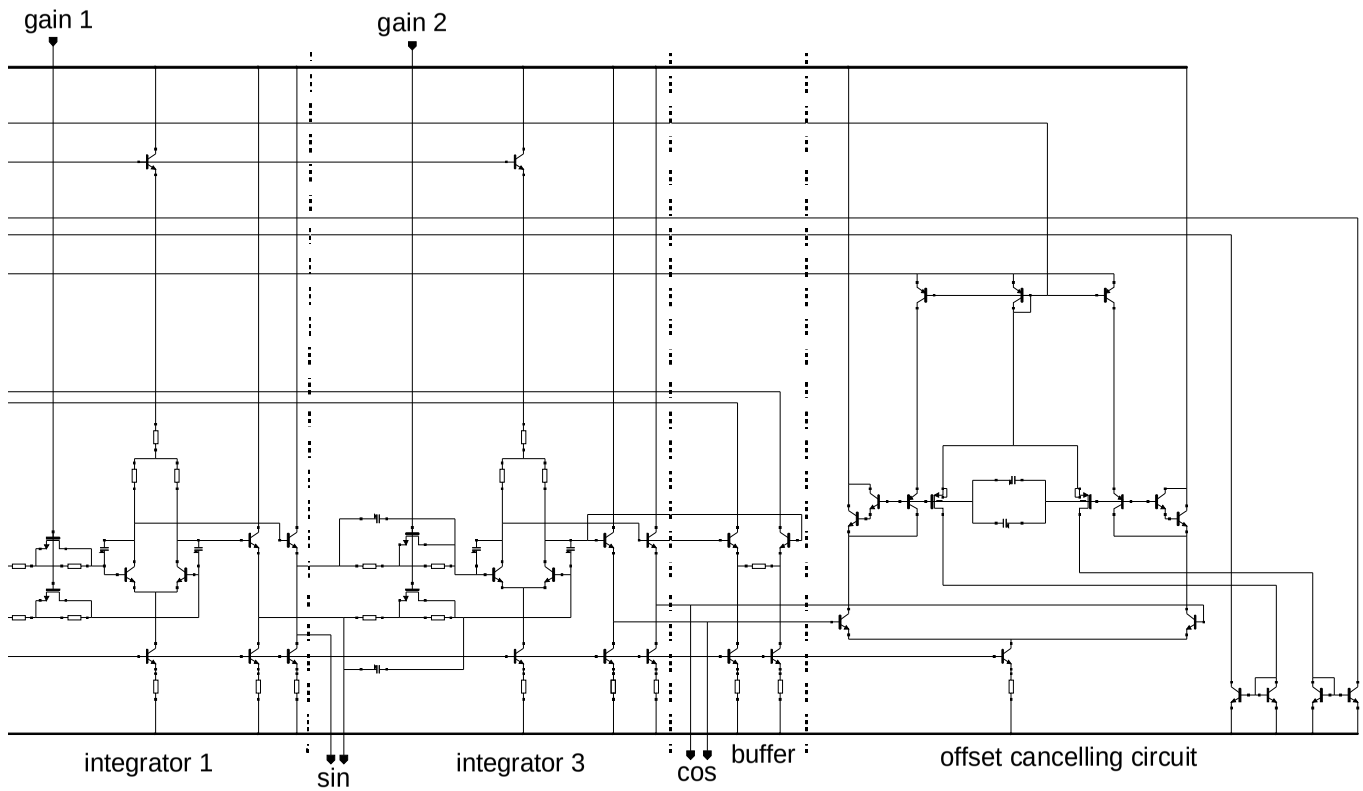


Fig. 44 Circuit diagram of the crystal oscillator with offset cancellation (part 2).

Measurement results

To test the performance of the oscillator with the offset cancelling circuit, it was entered into a one-chip TV processor IC [34]. This IC is made in a 1µm BiCMOS process [36]. Fig. 45 shows a photograph of the crystal oscillator, including the offset cancellation circuit. The area indicated in Fig. 45 is approximately 0.02mm^2.

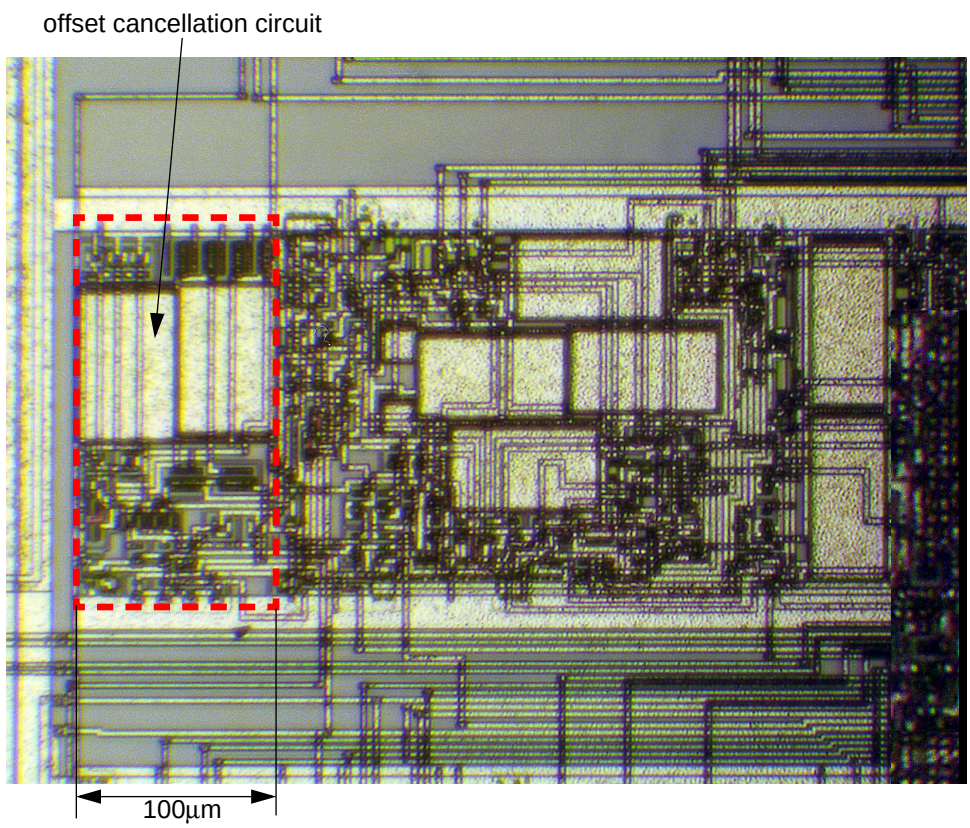


Fig. 45 Photograph of the crystal oscillator with offset cancellation.

Fig. 46 shows an oscillogram of the subcarrier output. It is not a perfect sine as there is a soft clipping differential-to-single converter between the sine output of the oscillator and the pin on which this signal is measured. The oscillogram does show, however, that the oscillator produces a stable oscillation.

Fig. 47 shows the -(R-Y) and -(B-Y) output signals with an EBU colour bar input signal

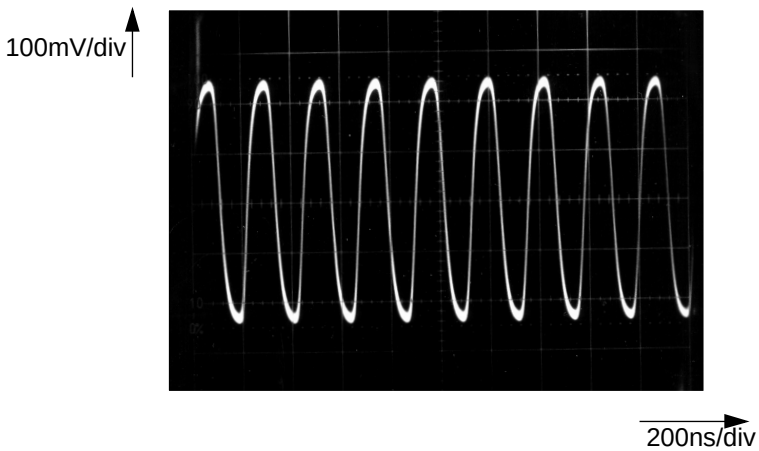


Fig. 46 Subcarrier on the reference output.

(see chapter 2): the output signals of the quadrature demodulator for the chrominance signal after these have passed through a third order low-pass filter. The photograph shows that the traces of the -(R-Y) and -(B-Y) signals are thin and not covered with “grass”. This indicates that there is not much subcarrier breakthrough to these outputs.

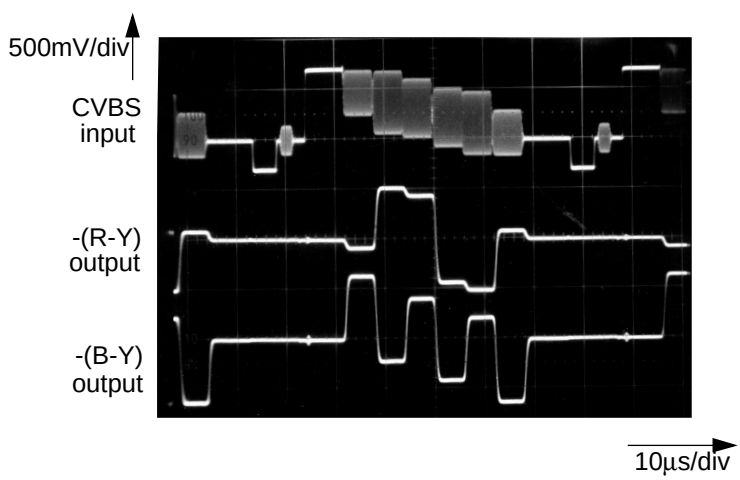


Fig. 47 Colour difference outputs with an EBU colour bar input.

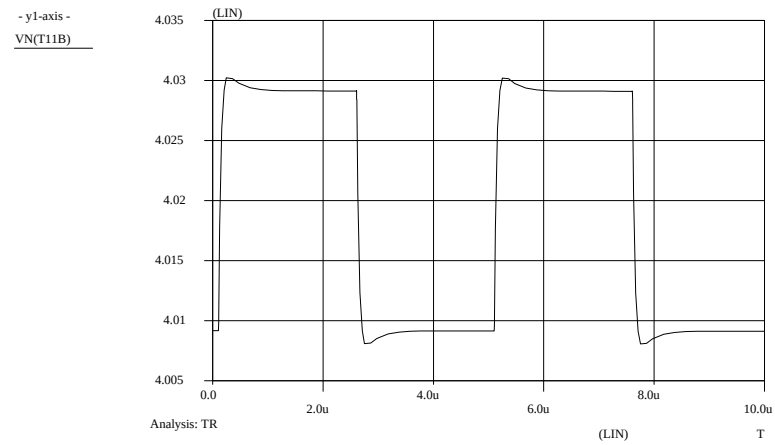
In 20 samples from four different batches the residual subcarrier amplitude was measured on the colour difference outputs. The average residual subcarrier amplitude on the -(R-Y) output is 1.4mV$_{pp}$ with a spread (1σ) of 0.5mV$_{pp}$. The average residual subcarrier on the -(B-Y) output is 1.3mV$_{pp}$ with a spread of 0.8mV$_{pp}$. So, the spec of 5mV$_{pp}$ is met for ICs within a 4σ spread.

The subcarrier breakthrough measurement gives a clear indication that the offset on the oscillator output is well within spec. As there are a number of other effects that influence the subcarrier breakthrough, the offset is most certainly within spec. However, the subcarrier breakthrough is an indirect measurement. Therefore the offset was measured directly at the outputs of the oscillator in four samples. As the oscillator output is not available as a differential signal, this required probing in the IC. The average offset for these four samples was 0.5mV on the sine output and on the 1.5mV on the cosine output. For both outputs the worst case offset that was measured differed less than 1mV from the average offset.

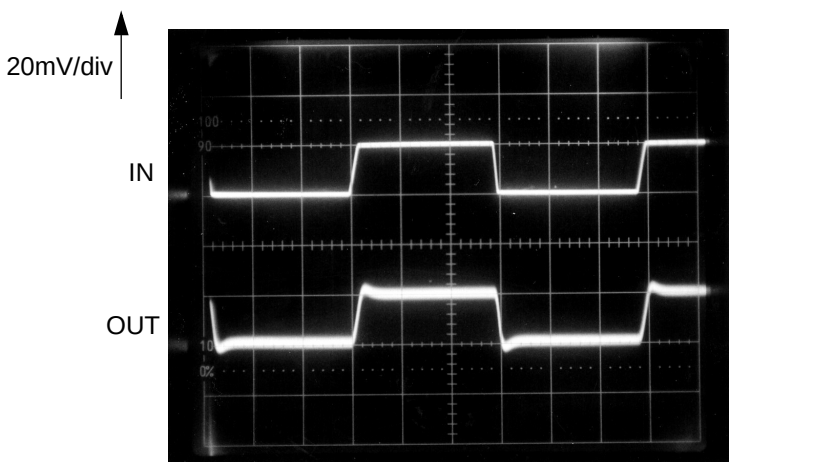
The fact that the low-unity-gain-frequency integrator circuit is part of the oscillator means that it is hard to measure its properties directly. Therefore a measurement was done to show that the design objective of the circuit was met. The design objective was to give a first order response to the two-integrator-plus-offset-control-circuit loop. Fig. 48 shows the response of the oscillator when the crystal is taken out and a step input signal is applied to the input of the single-to-differential converter. The output signal is the output signal of the differential-to-single converter. For this experiment the gain control of the integrators was set such, that their unity-gain frequency was minimum (Fig. 35). As stated earlier, this represents the worst case condition that can occur when the circuit is starting up. The frequency control input was set such, that the multiplier at the output of integrator number 2 was set to zero gain. By setting the controls like this the measurement path is limited to the two-integrator-plus-offset-control circuit part of the oscillator.

From Fig. 48 it can be concluded that the design objective is met. The response to the step shows a small overshoot, but there is no sign of ringing or oscillation, which would indicate that circuit is near the limit of stability.

The overall system of which the oscillator is a part has a signal-to-noise ratio of more than 52dB. It is not the oscillator, but an active filter, that is the limiting factor of the signal-to-noise ratio.



(a)



(b)

Fig. 48 Step response of the two-integrator-plus-offset-control-circuit loop.
(a) simulation, (b) measurement.

Conclusions

A line of low-unity-gain-frequency integrator circuits has been proposed. The current level in these integrators is chosen such that the level is far above the leakage current level. As the unity-gain frequency is dependent on the bias current, a lower unity-gain frequency can be made in processes with lower leakage current levels, by lowering the bias current. The proposed circuits have a number of properties which are similar to circuits using the Miller effect. There are, however, two marked differences. First, the unity-gain frequency of the new circuits is related to the simulated value of the capacitor instead of its physical value. Secondly, as the new circuits are based on current attenuation, their noise behaviour is relatively poor.

The proposed circuit technique has been successfully applied in a voltage controlled crystal oscillator to stabilise a DC control loop.

chapter 4

Mixed-signal narrow-band quadrature PLL-demodulator with programmable centre frequency

Introduction

The signal processing circuit that sets a colour TV apart from a black-and-white one is the colour demodulator (also called colour decoder). This circuit demodulates the colour information that is modulated on a subcarrier to the baseband (see chapter 2). A colour decoder regarded as a system in its own right, can be described as a narrow-band quadrature PLL-demodulator with programmable centre frequency.

To obtain the very high accuracy of the free-running frequency that is needed for the demodulation of PAL and NTSC signals, the oscillator in the PLL is usually a crystal oscillator [38]. For a TV that can be used all over the world, four different crystals are necessary. Apart from the crystals of the colour decoder, most TVs also have one crystal to generate the clock for the microcontroller and the teletext decoder. Crystals are expensive components, so the number of crystals in a TV should be as low as possible to keep the cost down.

This chapter describes a mixed-signal colour demodulator circuit that is built around a PLL that does not need crystals to generate the colour subcarrier frequencies. The topology of the mixed-signal demodulator is based upon the topology of the analogue system. The desired colour subcarriers are generated by a digital frequency synthesiser that uses the same clock frequency (24MHz) as the microcontroller that is also present in the overall system [39]. This means that four of the five crystals can be eliminated from the system.

The external loop filter of the traditional colour decoder's PLL is replaced by an integrated digital loop filter. Despite the fact that a large part of the PLL is made with digital circuits, the input signal is not digitised. The link between the analogue and the digital domain is a 1-bit sigma-delta converter that only has to convert the phase error signal, which is a quasi- DC signal. The signal path of the demodulator is completely analogue. As the colour decoder is part of a bigger system which also has a completely analogue signal path, this approach has the advantage that there is no need for a high-performance ADC in the signal path. Such a circuit would require a considerable amount of silicon area.

The colour decoder part of a TV

The colour demodulator in the block diagram of the basic TV receiver in chapter 2, actually consists of two separate colour demodulators. One is used to demodulate PAL and NTSC signals, while the other demodulates SECAM signals. Two separate colour demodulators are used because of the very different requirements of the transmission standards. Fig. 49 shows a high-level block diagram of the system around these two demodulators. First the CVBS input signal is split into the luminance signal Y and the chrominance signal C in a filter block. The chrominance signal is subsequently demodulated to obtain the colour difference signals (R-Y and B-Y). After post processing the resulting U and V signals are combined with the luminance signal to obtain the RGB signals for the output stages of the TV.

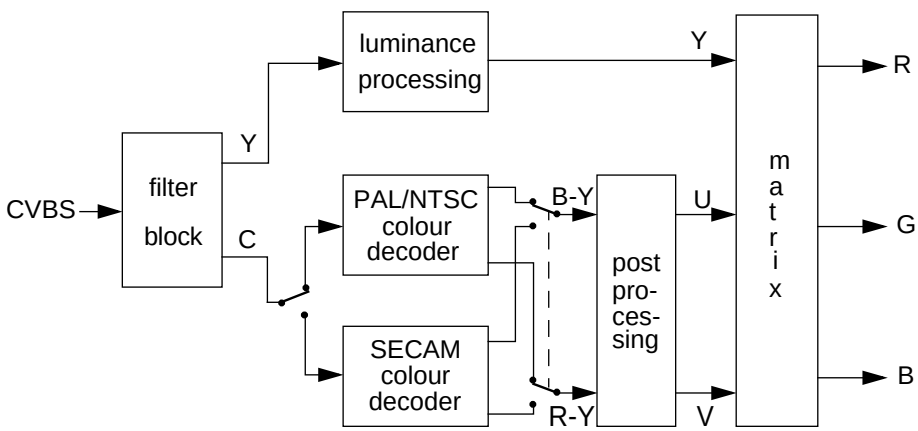


Fig. 49 Block diagram of the video processing part of a TV.

Differences between the PAL/NTSC and the SECAM colour decoder

The colour decoders for both PAL/NTSC and SECAM are built around PLLs. The characteristics of the two PLLs, however, are very different due to the differences between PAL/NTSC and SECAM.

The chrominance signal of the SECAM system is frequency modulated on two different carriers. In this system the PLL locks to the incoming signal not only during the burst time, but also during the active part of the video line. Consequently, the PLL for SECAM must have a wide bandwidth (ca. 1MHz) because it must follow the modulated carrier during the whole line time. The PLL for PAL and NTSC must have a narrow bandwidth (ca. 700Hz) because it

must lock to a stable reference frequency during the burst time. During the rest of the line time the PLL for the PAL and NTSC systems is not closed, so its oscillator produces a stable frequency for the QAM demodulation process.

If the bandwidth of the PAL/NTSC PLL were wide, there would be a significant risk of false-locking due to the fact that the PLL is a closed loop during only a part of the line-time. This can cause the PLL to lock to a multiple of the line frequency instead of the colour subcarrier. If there were only this requirement, a bandwidth of half the line frequency (i.e. 7.8kHz) would be the maximum allowable bandwidth. However, there are four different subcarrier frequencies in use around the world. The harmonics of the line frequency of one system can be just a few hundred Hertz away from the colour subcarrier frequency of another. With a large lock-in range the PLL may lock to a multiple of the line frequency of one system, making the PLL's lock detector (which is usually called colour killer in TV applications) think it has locked to the colour carrier of another. This is a highly undesirable situation as it makes automatic detection of the colour system being received impossible. Therefore the lock-in range of the PLL must be limited to about 700Hz.

Traditional analogue PAL/NTSC colour demodulator

The traditional way of making a PAL/NTSC colour demodulator is shown in Fig. 50. The

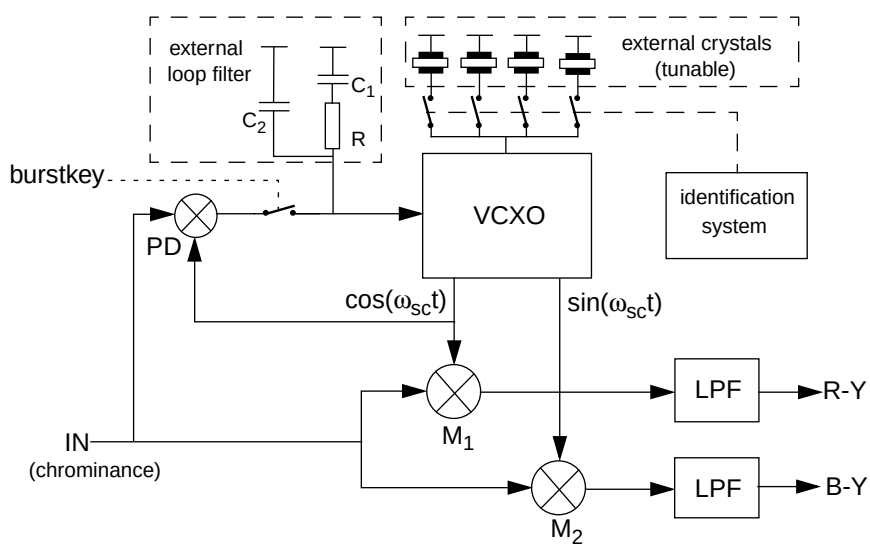


Fig. 50 Traditional analogue PAL/NTSC colour demodulator.

core of the demodulator is a PLL with a quadrature voltage-controlled crystal oscillator (VCXO) [40]. A VCXO is used because then, thanks to the very low frequency tolerance of crystals, the absolute frequency accuracy of the PLL is very high, so that the risk of false locking is minimal. The cosine output of the VCXO is connected to a multiplier that multiplies the cosine signal with the incoming signal. The output of this multiplier (or phase detector, PD) is connected to the (external) loop filter during the burst time (controlled by the burstkey signal). The output of the phase detector is low-pass filtered and fed to the frequency control input of the VCXO. The quadrature outputs of the VCXO also drive two multipliers (M_1 and M_2) that demodulate the chrominance signal. After low-pass filtering the outputs of the multipliers, the colour difference signals are available for further processing.

Fig. 51 shows the waveforms of a number of signals in the PAL/NTSC demodulator. The VCXO produces a sine wave. This sine wave is connected to one input of the demodulating multipliers. The gain from this input to the output of the multiplier is so high that it effectively multiplies the signal on the other input with a square wave. In other words: the chrominance signal is rectified in the demodulator, not linearly multiplied. This implies that only the phase accuracy of the oscillator signal is important, its amplitude accuracy is irrelevant.

The transfer characteristic of the analogue colour decoder PLL is derived in appendix B.

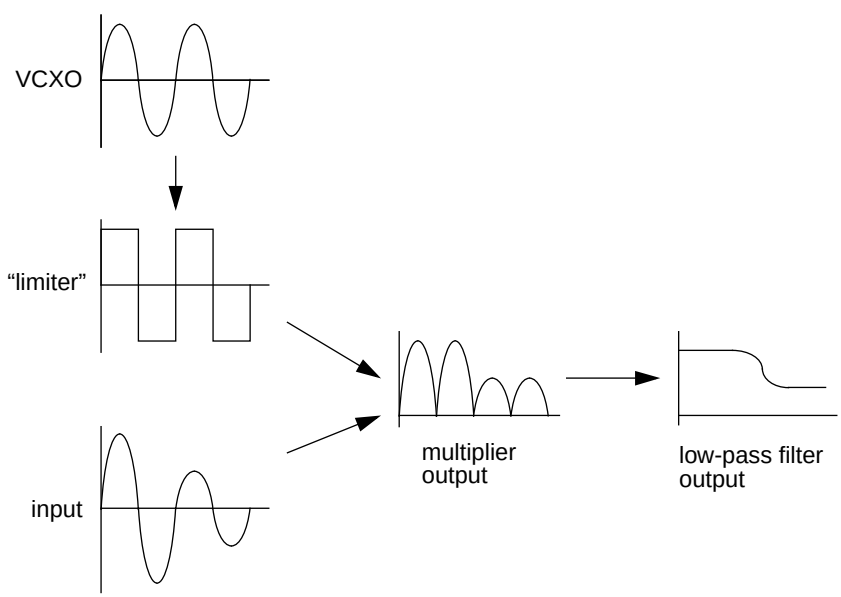


Fig. 51 Signals in the analogue demodulator (time domain).

The PLL has two modes of operation:

1) Tracking mode.
   In this mode the PLL is locked to the input frequency and follows it. The bandwidth of the loop is lower in this mode than in the acquisition mode to increase noise immunity. It may not be too low because that would cause problems when the phase input signal changes quickly. This is a phenomenon that is important when the signal is supplied by a video recorder, as will be explained later.

2) Acquisition mode.
   In this mode the PLL tries to lock to the incoming signal. The phase detector gain is increased in this mode to increase the acquisition range. A PLL locks to a signal within the acquisition range with a phase transient. As the acquisition range is always smaller than the tracking range for a second- or higher-order loop [40], the gain of the loop must be increased to guarantee the PLL can lock to all frequencies in its tracking range with just a phase transient. This will reduce the time the PLL needs to lock to an incoming signal, especially if there is a lot of noise on the input signal.

PAL H/2 ripple

The loop filter of the colour decoder shown in Fig. 50 has one component more than the loop filter of the standard design of [40]. Capacitor C_2 is an extra component that must suppress the so-called H/2 ripple of PAL signals. The phase of the PAL burst signal changes between -45^o and $+45^o$ from line to line. The PLL will try to follow the phase change from line to line. This causes a phase error which has the same value in successive lines, but opposite signs. PAL was designed to reduce the effect of static phase errors, i.e. errors with the same value and the same sign in successive lines. The phase change from line to line cannot be compensated by the PAL system. As a result of the phase jump from line to line a (small) colour fault will arise. As the maximum phase change from line to line is rather small in a PAL demodulator without C_2 (no more than a few degrees), the colour fault is hardly noticeable. If C_2 is added to the loop filter the phase change from line to line is strongly reduced, thereby virtually eliminating the colour fault.

Another reason for adding C_2 to the loop filter is the fact that TV test pictures contain so-called anti-PAL signals. PAL was designed to be insensitive to differential phase shift. If the coding of the PAL signal is deliberately inverted, a normal PAL receiver will increase, instead of eliminate, the phase error. Originally these signals were used to adjust PAL decoders. Nowadays colour decoders do not need adjustment any more. But the anti-PAL signal is still part of TV test pictures. If C_2 is not present in the loop filter these anti-PAL signals will show up as

coloured instead of grey patches. People who do not know the background of this colouration tend to think that a TV that shows these colours is inferior [41].

Fig. 52 shows the output signal of the traditional analogue colour demodulator with a PAL input signal. The shape of the colour difference signals in two successive lines is nearly, but not quite, identical. The difference is so small that it is hardly visible in Fig. 52.

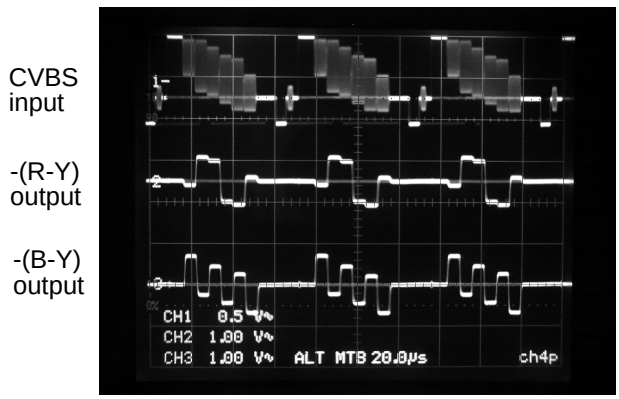


Fig. 52 Colour difference output signals of the traditional analogue colour decoder with a PAL input signal.

dynamic behaviour of the PLL in the colour decoder

The simulation of the step reponse to a 90^o phase jump of the system is shown in Fig. 53. TV signals from a transmitter will not normally have phase jumps on the colour carrier, but video cassette recorders (VCRs) can have a phase jump just before the start of the vertical blanking period, due to the way the TV signals are written to and read from the tape. A video recorder has two heads that write the video signal on the tape during recording and read it back during playback. The heads are active during alternate fields. The phase jump occurs due to the so-called head take-over [42]. This takes place just before the start of a new field. In the tracking mode the phase error must be less than 5^o at the start of the active video lines of the next field to make sure it is not noticeable. This implies the phase error should be less than 5^o after 2ms. In the acquisition mode the phase error is not relevant, as the output signal of the PLL is not displayed then. Only the stability of the PLL is important in this case. As can be seen in Fig. 53 (and Fig. 54) the PLL is stable. But, the step response does show ringing in the acquisition mode. This ringing (which does not occur in a true second-order PLL [40]) is a result of

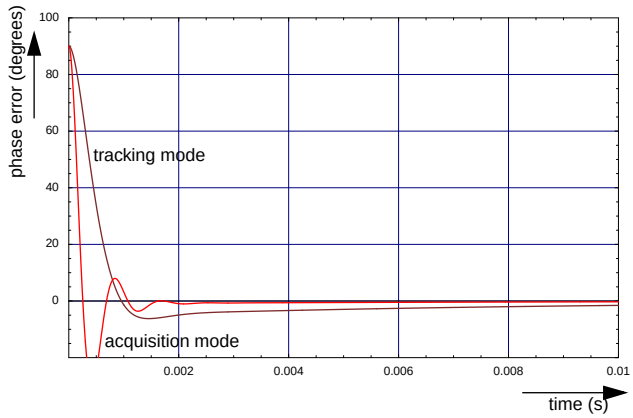


Fig. 53 Step response to a 90^{o} phase jump of the analogue colour decoder PLL.

the addition of C_2 to the loop filter.

simulation of the open-loop response

The open-loop transfer characteristics of the analogue PLL for the two modes of operation are shown in Fig. 54. In the acquisition mode the phase detector gain is increased by a factor of five. From these characteristics it can be concluded that C_2 has a negative influence on the stability of the PLL, especially in the acquisition mode. In the acquisition mode the influence of capacitor C_2 reduces the phase margin of the PLL to 37^{o}.

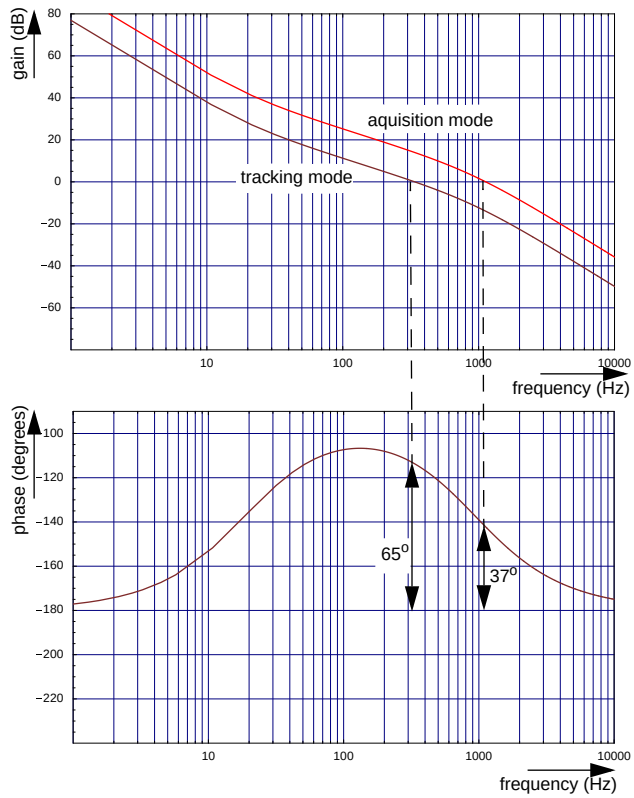


Fig. 54 Open-loop transfer characteristics of the analogue colour decoder PLL.

specification of the PLL in the analogue colour decoder

The most important specification points of the analogue colour decoder PLL are summarised in Table 6 [43]. The names behind the centre frequencies are the names of the standards that use these frequencies.

centre frequency	3.579545MHz (NTSC-M) 3.575611MHz (PAL-M) 3.582056MHz (PAL-N) 4.433619MHz (PAL-B,G)
acquisition/tracking range	+/-700Hz
natural frequency	550rad/s (tracking mode) 1128rad/s (acquisition mode)
damping	2.25 (tracking mode) 5.0 (acquisition mode)

Table 6 Important specification points of the analogue colour demodulator.

Requirements on the new colour decoder

The colour decoder PLL described above is a very reliable and robust system, but has a severe non-technical drawback: total system cost. In the world four different frequencies are in use for the colour subcarrier. Each of these frequencies requires its own crystal. As these crystals must be cut such that it is possible to detune them slightly from their nominal frequencies, they are more expensive than 'normal' crystals. Therefore a colour decoder based on a PLL with only one crystal, preferably a non-tunable one, would bring significant cost savings. If the new decoder can run on a fixed-frequency crystal this also means it can run on the system clock, if it is part of a larger system. In the latter case the colour decoder PLL turns into a no-crystal PLL. If the external loop filter can also be integrated the cost saving will be even higher.

The requirements can be listed as follows, ordered by importance.

1) Circuit behaviour identical to the analogue decoder (or better).
   The analogue system performs well enough, only its cost is too high.

2) Eliminate the need for tunable crystals.
   The tunable crystals are the most important cost factors of the analogue system. The system to which the colour decoder must be added has a clock frequency of 24MHz available. If possible, this frequency should be used. For the new system to be economically viable the extra silicon cost of the new colour decoder must be below the cost of the external crystals.

3) Do not digitise the input signal.
   The colour decoder is part of an analogue signal processing system. If only one

circuit in the signal processing chain is digital this means an anti-aliasing filter, ADC, DAC and reconstruction filter will be necessary to connect the colour decoder to the rest of the system. This overhead is important as it increases the cost of the new colour decoder, making it harder to compete with the analogue decoder.

4) Integrate the external loop filter.
   The cost of the external components is not high, but eliminating the loop filter does release a pin of the IC. In signal processing ICs pins tend to be very precious, as on the one hand many pins are required to provide maximum flexibility, whereas on the other hand the number of pins must be kept to a minimum for cost reasons.

5) Avoid critical analogue components and subcircuits.
   This is a “nice-to-have” requirement, that will make the integration of the new circuit in a bigger system easier.

Towards a new design

As the most important requirement on the new system is that the loop transfer must be as close as possible to the transfer of the analogue system, no circuit topologies have been pursued that are very much deviating from the topology of the analogue system. This means that all kinds of frequency synthesisers, based on harmonic mixing [44], or based on techniques such as pulse rate multipliers, swallow counting or sidestep programming [45], [46] were rejected without further consideration.

Alternative PLL configurations for the colour decoder

In this section a number of alternative PLL configurations, that might be used as the core of the colour decoder, are evaluated.

PLL with matched oscillators

A PLL with a transfer function that is exactly identical to that of the PLL in the traditional demodulator and that keeps the output frequency within a predetermined window, with the use of a fixed reference frequency, is shown in Fig. 55. The oscillator in this PLL is a fully integrated relaxation oscillator. This system has been successfully applied [47]. In this system a master oscillator locks to the reference frequency generated by the reference oscillator. A slave oscillator is connected to the same frequency control voltage as the master oscillator. However,

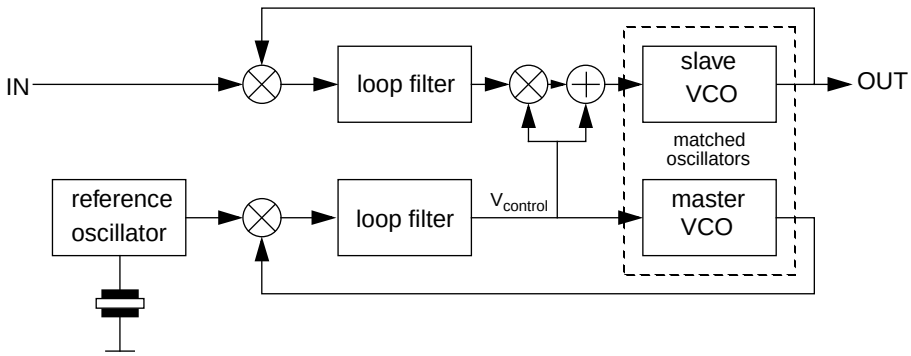


Fig. 55 PLL with matched oscillators.

this voltage is multiplied by a factor of α (with $-\alpha_{max} \leq \alpha \leq \alpha_{max}$). This allows the slave oscillator to freely move in a range $(1-\alpha_{max})*f_{master} < f_{slave} < (1+\alpha_{max})*f_{master}$.

Although this is a reliable system, it cannot be used for our purpose: the frequency accuracy of this system is limited by the matching properties of the oscillators. This accuracy is of the order of one per cent of the centre frequency. This means that the acquisition range must be at least a few per cent of the centre frequency to make sure the PLL can lock, even in the case of maximum mismatch. As an acquisition range of about one hundredth of one per cent of the centre frequency is required (see Table 6), it is obvious this solution is not viable.

analogue PLL with digital frequency watch-dog

Fig. 56 shows an analogue PLL in which the free-running frequency is guarded by a frequency watch-dog [48]. This system has been successfully applied in radio ICs [49].

As in the PLL with matched oscillators, the oscillator in this PLL is a relaxation oscillator. The absolute frequency accuracy of the oscillator is maintained by the digital frequency watch-dog. Each time the oscillator frequency moves outside the acquisition/tracking window the watch-dog forces it back to this window.

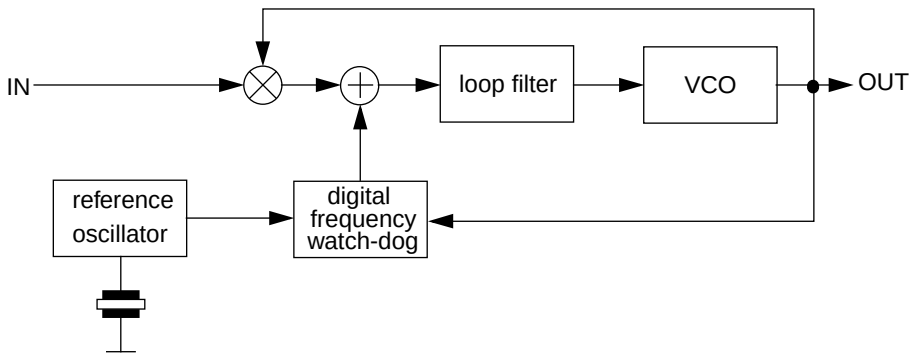


Fig. 56 Analogue PLL with digital frequency watch-dog.

Experiments with this type of system showed a high susceptibility to crosstalk from the digital to the analogue circuits. This was partly due to the fact that the sensitivity of the integrated VCO is of the order of 1MHz/V, instead of 1kHz/V as for the VCXO in the analogue system. Also the fact that the PLL is closed only during the burst time played a role. In the radio application the PLL is permanently closed.

Due to the susceptibility to crosstalk encountered in the experiments, this system was abandoned in favour of the system that will be described in the rest of this chapter. However, there is no doubt in the author's mind that this kind of system can also make a good colour decoder PLL.

replacing analogue by digital circuitry

The most important target for the new colour decoder PLL is that it must have a response as close as possible to the analogue system. Combining this with the 'nice-to-have' requirement (to have as much of the PLL digital as is possible while keeping the number of sensitive analogue circuits down to a minimum), leads to a topology that replaces as much as possible of the analogue circuitry by digital equivalents. But, when doing this, no ADC for the input signal should be introduced (requirement 3). Fig. 57 shows the resulting topology.

The VCO has been replaced by a discrete-time oscillator (DTO) [50]. Here a brief description of the DTO is given, a full explanation of the DTO and its properties is given on page 94. A DTO is an oscillator that is composed of a register and an adder (Fig. 68). On each active clock edge the number in the register of the DTO is incremented by a certain amount. This

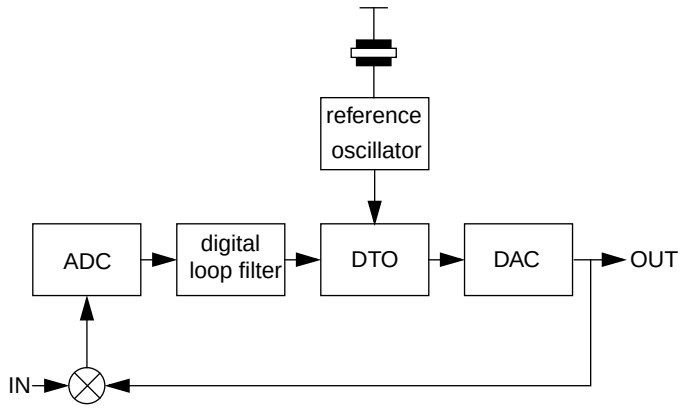


Fig. 57 Straightforward mixed-signal PLL.

increment can be regarded as a phase increment. When the phase has been incremented by 360^{o} (i.e. when the register overflows) a new cycle of the output signal starts. By varying either the clock frequency of the register, or the input word of the adder, the output frequency of the DTO can be varied.

The output signal of the DTO is DA converted and fed to the phase detector. The output signal of the phase detector is digitised before it enters the digital loop filter. This ADC can be far simpler than an ADC that has to convert the input signal: it only has to convert the phase error signal, which is a quasi-DC signal.

Although the PLL of Fig. 57 fulfils a number of the requirements, it does not produce a response which is close to the analogue PLL's response. A comparison of Fig. 51 and Fig. 58 shows why. The analogue system relies on an accurate timing of the zero-crossing of the oscillator to demodulate the input signal by means of rectification (Fig. 51). As a DTO can only change its output level at an active clock edge, and as the clock has no relation to the input signal, the zero-crossings of the output of the DTO have a very high timing jitter with respect to the zero-crossings of the input signal. This results in a heavily distorted output signal of the demodulator.

In principle there are two ways to cure the problems of the straightforward mixed-signal PLL of Fig. 57: either in the time- or in the frequency-domain. In the time-domain solution the zero crossing of the DTO is shifted to the desired time-point. In the frequency solution the spectra of the signals in the system are shaped such that the system performs its desired function. Both ways will explored in the following.

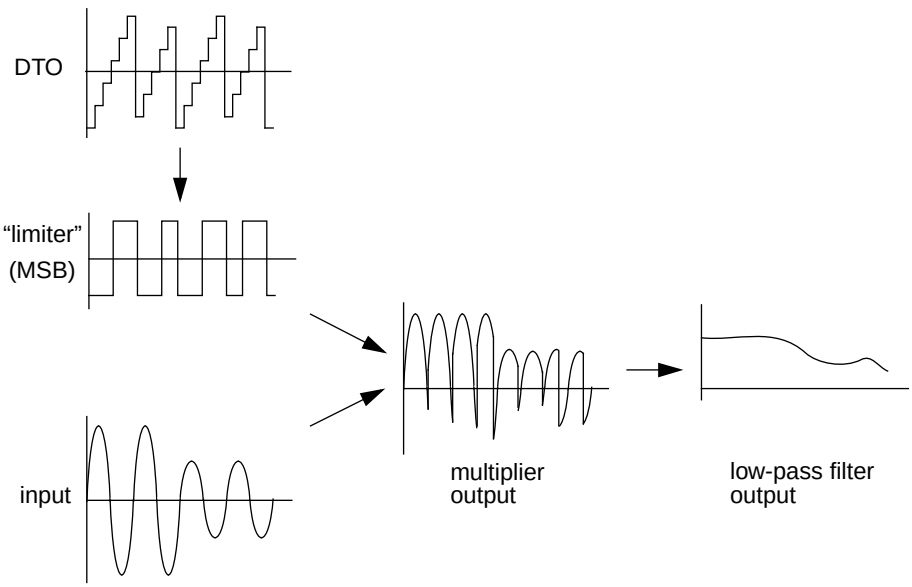


Fig. 58 Signals in mixed-signal demodulator (time domain).

time-domain solution to the DTO jitter

In the time-domain solution (Fig. 59) the correct position of the zero-crossing is retrieved by looking at the value of the DTO just before and just after the zero-crossing. As the value in the DTO rises linearly with time, it is easy to calculate how much time the ideal zero-crossing occurs after the last clock edge before the zero-crossing of the DTO. The exact position of the zero-crossing with respect to the last active clock edge is (Fig. 60):

$$\Delta t = \left| \frac{M_{t-1}}{K} \right| T_{clk} \tag{15}$$

In this equation Δt is the time between the last active clock edge and time at which the DTO would have its zero-crossing, if it were a continuous-time circuit. The DTO counts from -2^{N-1} to $2^{N-1}-1$. The number in the register of the DTO just before the zero-crossing is M_{t-1}. The number with which the DTO is incremented each clock cycle is K, and the clock period is T_{clk}. By using the absolute value of the factor with which T_{clk} is multiplied, Δt will be greater than zero for both positive and negative going zero-crossings.

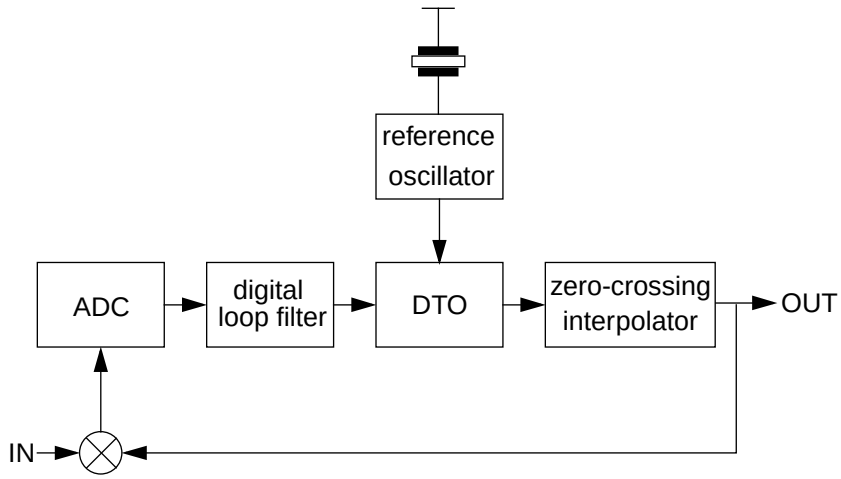


Fig. 59 Mixed-signal PLL with exact timing of the zero-crossing of the output signal.

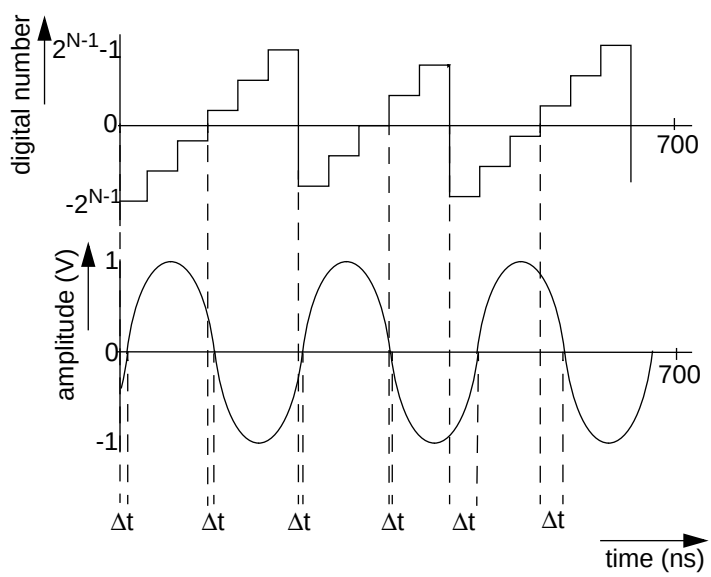


Fig. 60 Difference in timing of the zero-crossing of the DTO output and the desired sine for correct demodulation.

The peak value of Δt is equal to one clock period. So by choosing T_{clk} low enough (i.e. by choosing the clock frequency high enough), the jitter on the zero-crossings can be made arbitrarily small. For the maximally allowable jitter a clock frequency of several GHz would be required. As this is far beyond the capabilities of the process in which the colour decoder has to be made, the jitter must removed in another way.

A zero-crossing interpolator circuit can be used to shift the zero-crossing from the clock edge of the DTO to the desired zero-crossing point. Fig. 61 shows an interpolator as proposed in [51]. The circuit is basically a delay locked loop (DLL), with a decoder to select the inverter in the chain whose output has the correct timing to make the rising or falling edge of the total circuit. The inverters are used as variable delay elements in this circuit, not as logic gates. Each edge is determined by another inverter of the chain. So, if the desired zero-crossing is 20% of one clock cycle later than the active clock edge of the DTO, and there are 30 delay inverters in the interpolator, then the output of inverter number 6 is the one that is closest to the actual zero-crossing.

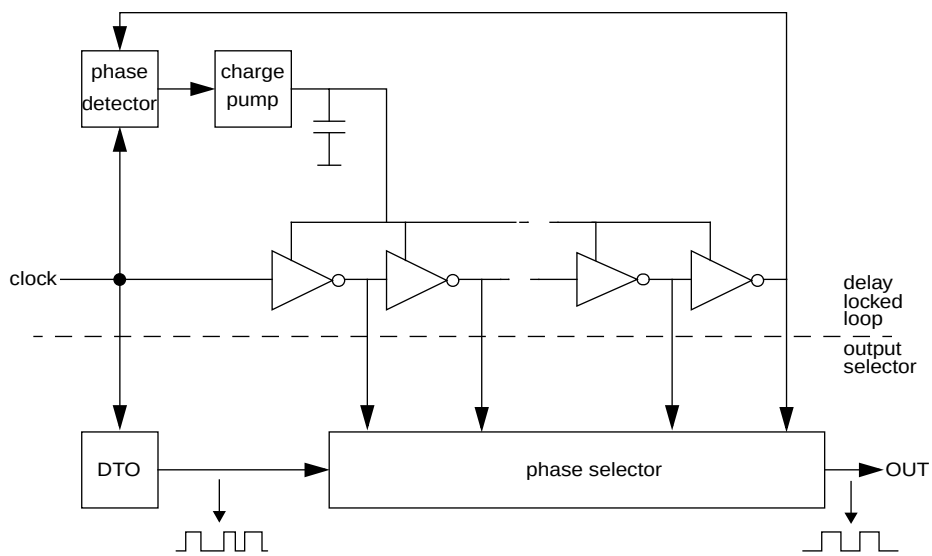


Fig. 61 Block diagram of the zero-crossing interpolator plus the DTO.

In [52] a variation of the above circuit is described. This solution uses a fixed delay, an integrator and a comparator to obtain correctly placed zero-transitions.

In [53] a system is described which also places the zero-crossing at the correct time but which, despite the epithet “all-digital” in the title, actually uses an analogue current-controlled

oscillator in the loop. The analogue control current is generated by a number of binary weighted current sources, which are switched on or off by a digital control word.

frequency-domain solution to the DTO jitter

Fig. 62 shows a frequency-domain alternative to the time-domain solution. The time-jitter problem of the DTO signal can also be considered a problem of its output spectrum. Therefore two band-pass filters have been introduced in the PLL to clean up the spectrum. The digital band-pass filter reduces all the spurious frequencies that are accompanying the desired frequency in the DTO's output spectrum. The analogue band-pass filter eliminates all the clock harmonics and frequencies that may arise due to non-linearity of the DAC.

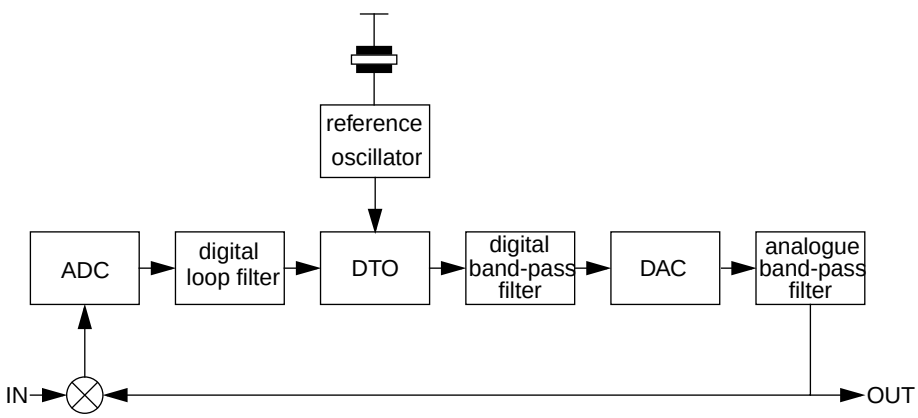


Fig. 62 DTO-based mixed-signal PLL with clean output spectrum.

Fig. 63 shows a circuit that has been presented in [54]. To a large extent the ideas behind the circuit of Fig. 63 are identical to the ideas behind the circuit of Fig. 62, but there are two differences. First, the crystal of the circuit has to be tunable, as the frequency of the DTO is controlled through its clock frequency. This means that the increment of the register in the DTO is always the same value K_{nom}. Secondly, instead of the analogue band-pass filter, an internal PLL is used to clean up the DTO spectrum. This PLL is the kind of sensitive analogue circuit that should be avoided according to requirement 5.

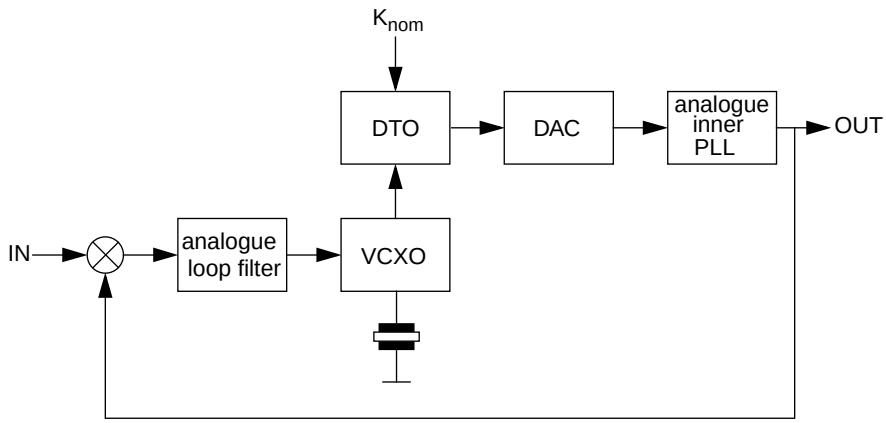


Fig. 63 Mixed-signal PLL [54].

The system presented in Fig. 62 is a generic system. If it is straightforwardly implemented, there are a few practical problems. For a start, the digital band-pass filter is a very large and complex circuit because there are very many frequency components in the DTO spectrum. Many of these components are very close to the carrier frequency, which implies that a very-high-Q filter is needed to clean up the spectrum. A very-high-Q digital filter is not a straightforward design as there is no integer ratio between the clock frequency and the centre frequency of the filter. The adders and multipliers needed in such a digital filter cost a lot of silicon area [55]. Therefore it is better to look at the function of the band-pass filter in a different way. What the band-pass filter should do is to output a pure sine wave when the input signal is a sawtooth. A waveform translator, instead of a band-pass filter, can also perform this function. A waveform translator can be made quite easily by means of a look-up table (LUT). A LUT is nothing more than a ROM, so it is far simpler and far more compact than a high-Q band-pass filter.

If the LUT outputs a sine with a clean spectrum, and the DAC is linear, the analogue band-pass filter really only needs to eliminate the clock frequency and its harmonics from the output signal of the DAC. This means that a low-pass filter can be used instead of the band-pass filter. As a low-pass filter is less complicated than a band-pass filter, this is the preferred solution.

In [56] a system is described that doesn't use a LUT, but converts the sawtooth of the DTO into a triangle and converts the triangle into a sine and cosine by means of non-linear DACs. According to [56] this approach offers power and die area advantages for systems with high

phase and amplitude accuracy. The accuracies needed in the colour decoder system (discussed later in this chapter) are not high enough to exploit these advantages.

Taking all these considerations into account the mixed-signal PLL of Fig. 62 turns into the PLL shown in Fig. 64.

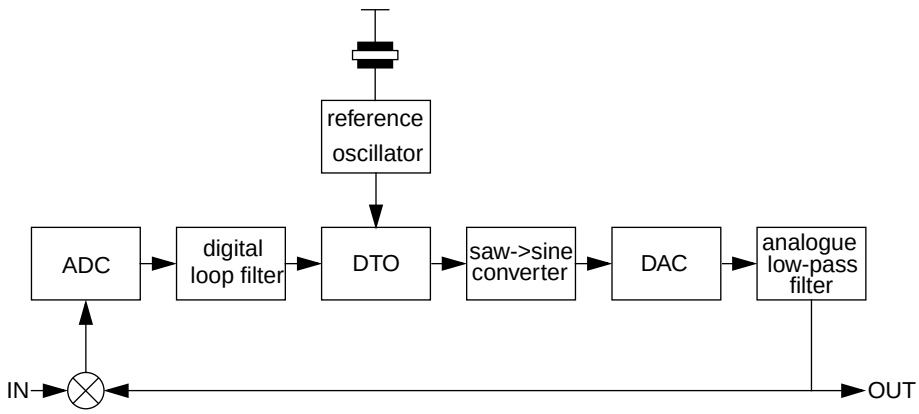


Fig. 64 Cleaning up the DTO spectrum with a waveform translator.

Comparison of the time- and frequency-domain solutions

When comparing the above solutions it can be concluded that the circuits with a zero-crossing interpolator can undoubtedly make a good PLL for this application, but the interpolator is in fact a sensitive analogue circuit; its inverters are not functioning as inverters, but as variable delay cells. This means that substrate interference may adversely affect the performance of the circuit. Therefore the more digital frequency-domain solution of Fig. 64 is preferred. This solution will be worked out in the following.

The complete colour demodulator

Taking the PLL of Fig. 64, a complete mixed-signal colour demodulator as shown in Fig. 65 can be made. In Fig. 65 the combination of DTO and saw-to-sine converter is drawn as a direct digital synthesiser (DDS) [57]. For the ADC a 1-bit sigma-delta converter is chosen. The phase error is a DC signal when the PLL is locked. When the PLL is not in lock the maximum frequency of the phase error signal is two times the lock-in range (i.e. 1400Hz). This occurs when the input signal is at the low end of the acquisition range and the DTO at the upper end

of the acquisition range (or vice versa). In PAL mode there will also be a frequency component at $f_H/2$ (i.e. 7800Hz). As the clock frequency is 24MHz the oversampling ratio is more than 1500. The signal-to-noise ratio of a 1-bit first-order sigma-delta converter with an oversampling ratio of 1000 is more than 80dB [58]. The colour decoder is only one component in the signal processing chain. The signal-to-noise ratio of the total chain must be better than 46dB [59]. The colour decoder should not be the limiting factor of the signal-to-noise ratio of the total chain. Therefore a signal-to-noise ratio of the colour difference signals higher than 52dB (peak-to-peak signal to rms noise) is aimed for. A 1-bit first-order sigma-delta converter with an oversampling ratio of 1500 easily surpasses this requirement.

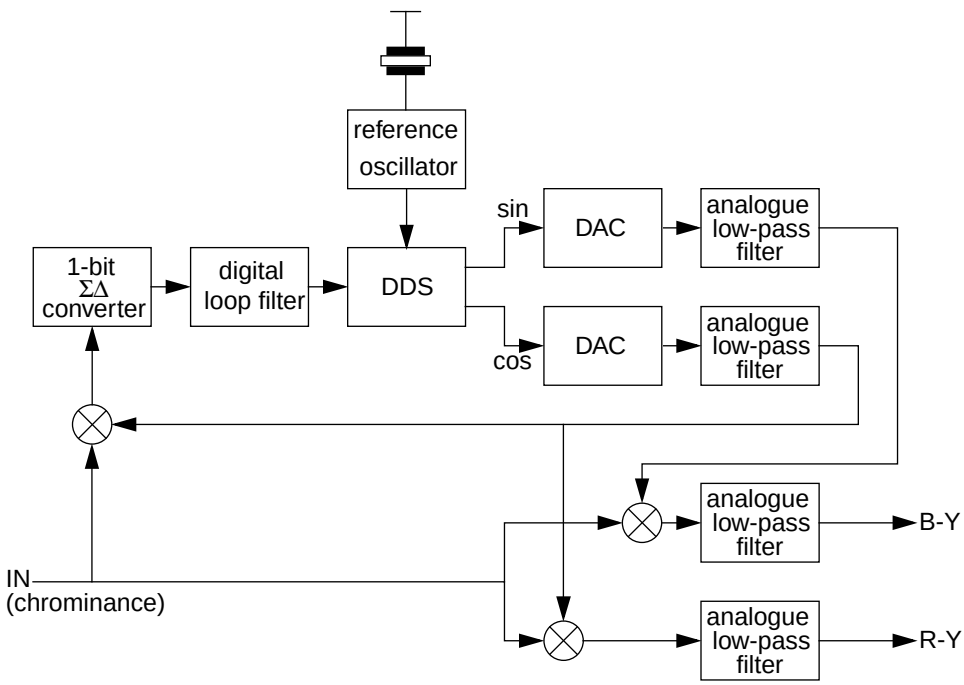


Fig. 65 Colour demodulator comprising the PLL of Fig. 64.

In appendix B a variation of the system of Fig. 65 is described [60]-[62]. In this system (Fig. 66) the low-pass filters at the outputs of the DACs have been eliminated, as their function (removal of the clock harmonics) is also performed by the low-pass filters at the output of the multipliers. The combination of DAC and multiplier is then replaced by a multiplying DAC. These changes are only allowable if the linearity of the multiplying DACs is very good.

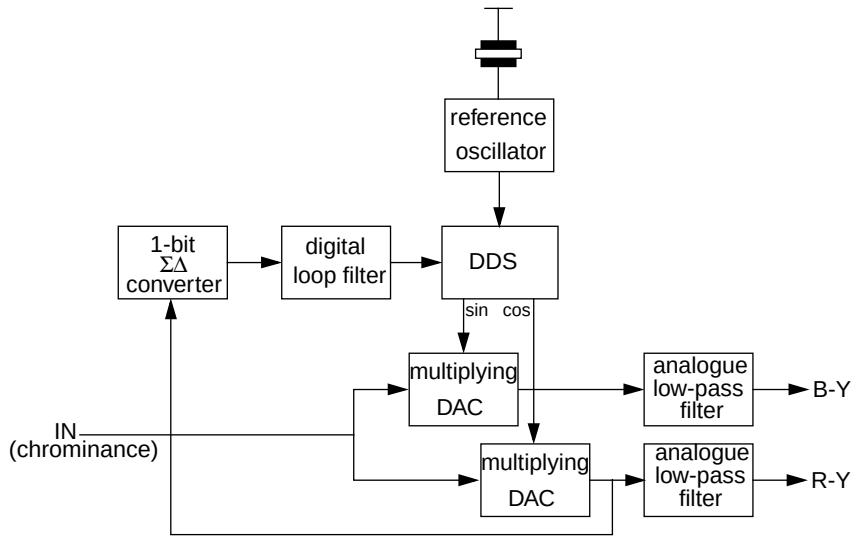


Fig. 66 Simplified colour demodulator.

Comparison of the DAC and MULDAC based systems

Although the performance of the system of Fig. 66 is good enough for standard video signals, the sensitivity to crosstalk of frequencies around the clock frequency (and its harmonics) to the analogue inputs of the multiplying DACs, is a major drawback when integrating the demodulator of Fig. 66 into a larger system. These crosstalk components fold back to the baseband at the analogue outputs of the multiplying DACs, as the digital inputs of the multiplying DACs change their value only at an active clock edge. The linear multipliers in the demodulator of Fig. 65 do not fold crosstalk components of the clock frequency (and its harmonics) back to the baseband. Therefore the demodulator shown in Fig. 65 is the preferred choice for further investigation (see also appendix B).

The component parts of the mixed-signal colour decoder

In the following sections the component parts of the mixed-signal colour decoder will be described one by one.

the direct digital synthesiser

With the direct digital synthesiser each desired subcarrier frequency can be digitally generated from a crystal-stable system clock. The DDS consists of four stages: an input stage, a DTO (or sawtooth generator), a hue control stage and a quadrature output stage. A block diagram is given in Fig. 67. The different stages will be discussed in the following sections. The DTO will be discussed first, as it forms the heart of the new colour decoder.

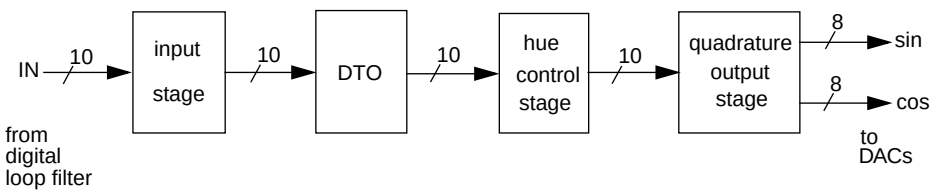


Fig. 67 Block diagram of the direct digital synthesiser.

the DTO

A DTO (Fig. 68) generates a digital sawtooth [50]. The DTO's output signal is shown in Fig. 69. At each rising edge of the clock clk the contents of the N-bits-wide register is increased by a number K. This goes on until the resulting value becomes greater than 2^N-1. When this happens the most significant bit (MSB) of the result is simply discarded and only the remainder is clocked into the register. Starting from this remaining value the process of adding and discarding the MSB if the sum is greater than 2^N-1 is repeated over and over. In this way the circuit of Fig. 68 generates a discrete-time digital sawtooth whose average frequency is:

$$f_{OUT} = \frac{K}{2^N} f_{clk} \tag{16}$$

When regarding the frequency spectrum of this discrete-time sawtooth many spurious components can be observed besides the main frequency component of equation 16. These spurious components are strongly suppressed by converting the discrete-time sawtooth into a sine (and cosine) waveform. This is done by the quadrature output stage. What remains then is a digital sine (and cosine) with a frequency given by equation 16.

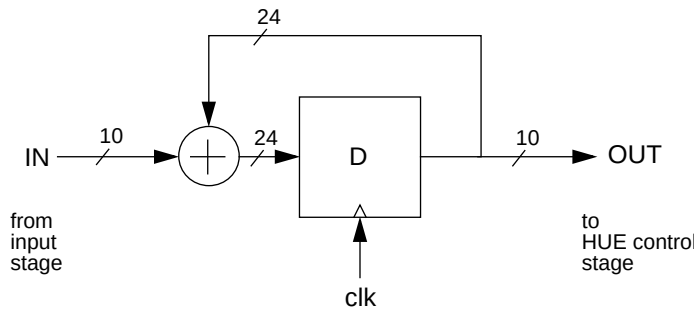


Fig. 68 Discrete Time Oscillator (DTO).

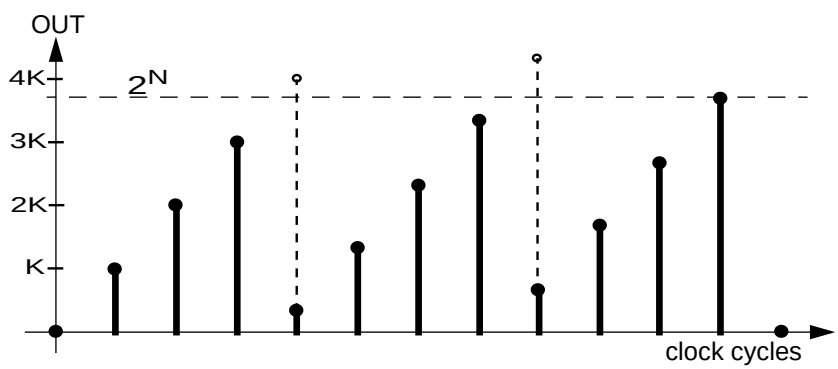


Fig. 69 The number in the DTO's register in successive clock cycles.

From equation 16 two conclusions can be drawn; as N is a fixed number and K is a digital value the frequency stability of f_{out} is directly related to f_{clk}. So when clk is a crystal-stable clock f_{out} also has crystal stability. Another important property that can be seen in equation 16 is the linear relationship between the digital number K and the output frequency f_{out}.

The output frequency of an analogue voltage-controlled oscillator is defined as $f_{out} = K_o v_{in}$. In this equation K_o is the oscillator sensitivity and v_{in} the (analogue) input voltage. Analogous to this the oscillator sensitivity K_o of the circuit of Fig. 68 is defined as:

$$K_o = \frac{2\pi}{2^N} f_{clk} \tag{17}$$

with K_o in [rad/s LSB]. As the DTO is digitally controlled its sensitivity is expressed in rad/s per LSB (Least Significant Bit) instead of per volt. So, the frequency resolution of this type of the DTO is $f_{clk}/2^N$ Hertz per LSB. This means that only discrete frequencies can be produced with intervals of $f_{clk}/2^N$.

phase jitter on the subcarrier

When using the DTO in a colour decoder its limited frequency resolution will cause a systematic frequency deviation in the PLL, as the generator is adjusted only once per TV line (T_H=64µs). It is unlikely that the frequency of the received chrominance signal (the colour bursts) is always exactly equal to one of the discrete frequencies of the DTO. Fig. 70 shows the situation that the received subcarrier frequency f_{sc} is between the frequencies f_k and f_{k+1} of the grid of the DTO. In this situation the PLL will cause the DTO to toggle between the two discrete frequencies f_k and f_{k+1} on either side of the colour subcarrier frequency.

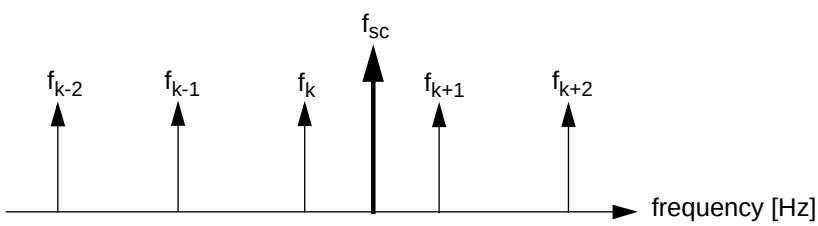


Fig. 70 Frequency grid of the DTO and the colour subcarrier frequency.

At the end of one line interval T_H = 64µs the frequency difference Δf between f_{sc} and f_k (or f_{k+1}) results in a phase difference Δθ (in radians):

$$\Delta\theta = 2\pi\Delta f T_H \tag{18}$$

In a worst case situation the value for Δf approximates $f_{clk}/2^N$: the frequency resolution of the DTO. In this case the peak-to-peak phase deviation is:

$$\Delta\theta = 2\pi\frac{f_{clk}}{2^N}T_H \tag{19}$$

word width of the DTO

With equation 19 a relation is obtained between the internal word width N and the resulting phase deviation. Using this equation the required word width of the DTO can be determined.

The PLL will try to keep the average phase deviation zero. The momentary $\Delta\theta$ is a function of time: $\Delta\theta(t)$. The resulting spurious signal in the colour difference output signals must be more than 55dB down with respect to the video signal to be unnoticeable [63].

Using trigonometry it can be calculated how a phase deviation between the sine and cosine output signals of the DTO and the incoming chrominance signal results in a spurious signal in the demodulated colour difference signals R-Y and B-Y. If the incoming chrominance signal is $\sin(\omega_{sc}t)$, the R-Y output signal is:

$$\sin(\omega_{sc}t)\cos(\omega_{sc}t + \Delta\theta(t)) = 0.5(\sin(2\omega_{sc}t + \Delta\theta(t)) + \sin(\Delta\theta(t))) \qquad (20)$$

The term with $\sin(2\omega_{sc}t)$ is eliminated by the low-pass filter at the output of the colour decoder (Fig. 65). So the spurious signal in the R-Y signal is $\sin(\Delta\theta(t))$. The B-Y signal will also contain a spurious signal of this value. However, this does not affect the signal-to-spurious ratio that is visible on the TV screen: both the signal and the spurious of R-Y and B-Y will be added, so the ratio remains the same.

Table 7 shows the peak-to-peak phase deviation and signal-to-spurious ratio as a function of the DTO word width.

DTO word width	peak-to-peak phase deviation	signal-to-spurious ratio
22	0.13^o	52.7dB
23	0.07^o	58.7dB
24	0.03^o	64.8dB

Table 7 Phase deviation and signal-to-spurious ratio as a function of DTO word width.

From Table 7 it can be concluded that a word width of 23 bits is enough for a 55dB signal-to-spurious ratio. However, as there are more factors contributing to the spurious signal (e.g. rounding errors in the waveform translator and clock jitter), it was decided to use 24 bits in the DTO. This guarantees that the DTO word width will not be the limiting factor in keeping the spurious signal below the level of visibility.

number of bits in the quadrature output stage

The DTO uses a 24-bit word width. If the saw-to-sine converter were addressed with all 24 bits, and would output 24-bit-wide words for the sine and cosine, a giant LUT would be needed. This would also require a very challenging DAC: 24-bit performance at a 24MHz clock frequency. Fortunately the word width of the sine and cosine can be less than 24 bits.

The signal-to-noise ratio (peak-peak for both signal and noise) of a quantised video signal is [50]:

$$SNR = 6.02M + 10\log\left(\frac{f_s}{2f_v}\right) \tag{21}$$

In this equation M is the number of bits, f_s is the sampling frequency (24MHz) and f_v is the bandwidth of the video signal. The bandwidth of the colour difference signals is 1.5MHz. As the colour difference signals are quadrature modulated on a subcarrier, f_v = 3MHz. If M is chosen M = 8, the resulting SNR = 54.2dB. This is somewhat lower than the spec, but the 55dB visibility criterion is based on a single spurious frequency. As the jitter energy is not concentrated in one single spurious frequency, the spurious-free dynamic range (SFDR, which is the parameter of real interest) is better than 55dB (Fig. 73).

In [64] it is demonstrated that for a good performance the resolution at the input of a digital saw-to-sine converter has to be four times higher than the resolution that is required at its output. This means that two bits more are needed at the input of the quadrature output stage than at its output. So, the saw-to-sine converter is addressed with the ten MSBs of the DTO and delivers 8-bit-wide sine and cosine words at its output.

saw-to-sine conversion

The digital sawtooth is converted into a digital sine and cosine waveform using look-up tables (LUT) in which one period of a sine and a cosine have been stored. The sawtooth acts as an address pointer for both tables. Another way of looking at this is to see the value of sawtooth as the phase information of the (co)sine.

Using the properties of sine and cosine, the LUTs can be simplified to reduce the circuit area. As the function y = sin(x) is symmetrical in both x and y direction it should be sufficient to store only one quadrant of this function in the look-up table. Moreover as the function y = cos(x) is simply a 90^o phase shifted version of the sine function, the same look-up table can be used. However, as both functions have to be available at the same time this is not possible without some extra measures. The sine and cosine can be retrieved at the same time by

dividing the stored quadrant into two sectors. The first sector stores the first 45^o of the sine wave, the second sector the second 45^o [65]. Because there is a 90^o phase shift between sine and cosine one of them will take its sample from the first sector, while the other takes its sample from the second sector, and vice versa. They will never need a sample from the same sector. This means that sine and cosine outputs are constantly swapping between the two LUTs that both store one eighth of a full sine wave. Fig. 71 shows the procedure graphically. For each sector it is indicated from which LUT the sine and cosine output must be taken. It is also indicated whether the address that goes to the LUT and the data that comes out of the LUT must be inverted or not to get the correct sine and cosine waveforms.

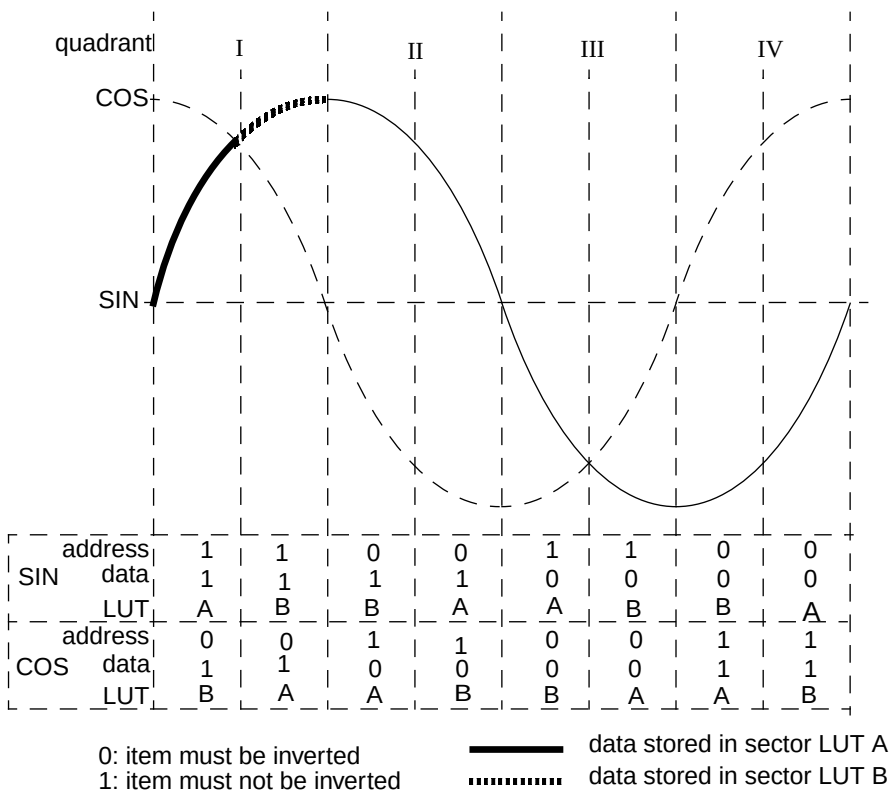


Fig. 71 Breaking the sine and cosine up in quadrants and sectors.

Fig. 72 shows the block diagram of the quadrature output stage. The LUTs are preceded by an inverter circuit that inverts the address data depending on the two MSBs of the address. The output of the LUTs are fed to a switch operated by MSB-1 and MSB-2. This way either LUT

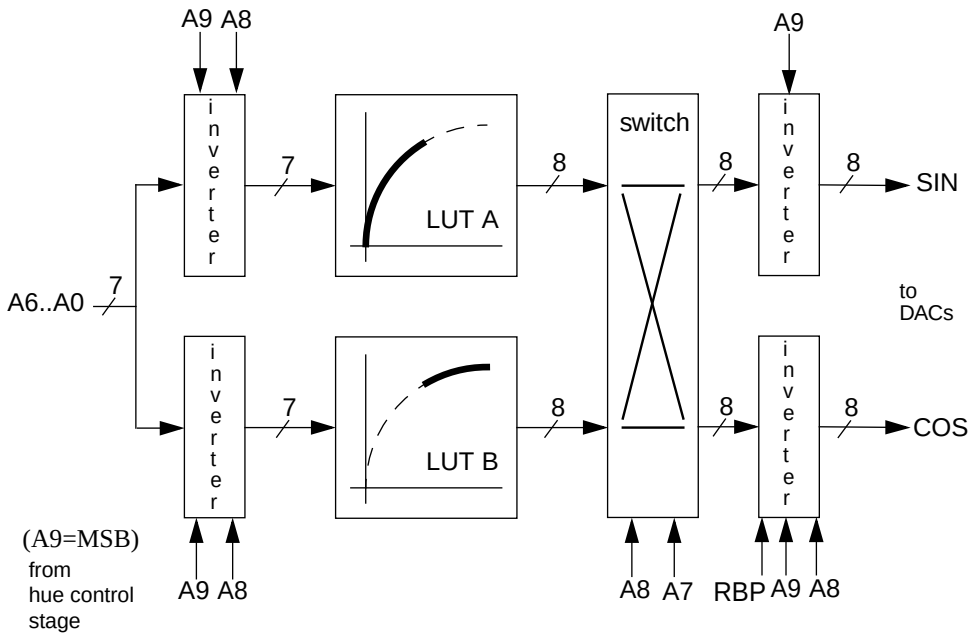


Fig. 72 Quadrature output stage.

can be connected to the sine or cosine output. The correct output data is obtained by inverting the LUT data under the control of the MSB and MSB-1. For the sine output the MSB suffices to do this, for the cosine output the MSB and MSB-1 are combined.

The contents of the look-up tables were calculated according to:

$$y = round\left(127\sin\left(2\pi\frac{1+2x}{2048}\right)\right) \tag{22}$$

As only one quadrant is stored in the combined LUTs, disturbing effects at the edges of the quadrant have to be avoided. Therefore as an operand ((1+2x)/2048) is used instead of (x/1024), with x = 0,1,...,255. This gives seamless transitions between the different quadrants.

In the actual implementation of this circuit combinational logic instead of a “real” ROM appeared to be more efficient in silicon area. This is due to the high address decoding overhead in the ROM compared to the small memory size.

phase alternation for PAL

When receiving a chrominance signal according to the PAL standard, the phase of the cosine output of the quadrature output stage has to be alternated between 0^o and 180^o with half the line frequency. To control this the signal RBP is fed to the inverting circuit of the cosine stage (Fig. 72). However, the cosine output only has to be alternated during the active video interval of each line. Therefore RBP is only active outside the burstkey time.

simulation of the spectra of the DTO and quadrature output stage

To verify the calculations, a simulation of a DDS with a 24 bits DTO and a 1024 x 8 bits sine ROM table was run. The output spectra of the DTO and the sine output of the complete DDS are shown in Fig. 73. From these figures it can be concluded that the spurious-free dynamic range (SFDR) is more than the required 55dB.

Table 8 summarises the specification of the direct digital synthesiser:

clock frequency	24MHz
DTO word width	24 bits
frequency resolution	1.43Hz/LSB
oscillator sensitivity K_o	9.0rad/LSB
sine/cosine word width	8 bits
SFDR	>55dB

Table 8 Specification of the direct digital synthesiser.

the HUE control stage

The hue control stage is placed between the DTO and quadrature output stage (Fig. 67). With the hue control a phase offset can be forced between the internally generated quadrature signals and the incoming colour burst. In this manner colour phase errors caused during transmission of an NTSC chrominance signal can be compensated (see chapter 2).

Hue control in the DDS is obtained by adding the digital hue control word to the output of the DTO. The sawtooth signal represents the phase of the quadrature signals sine and cosine. The hue control word is a variable phase offset that is added to the sawtooth during the colour bursts. During the active video part of each TV line, the hue control word is not added to the sawtooth. As the PLL locks to burst with the offset, while demodulation takes place without

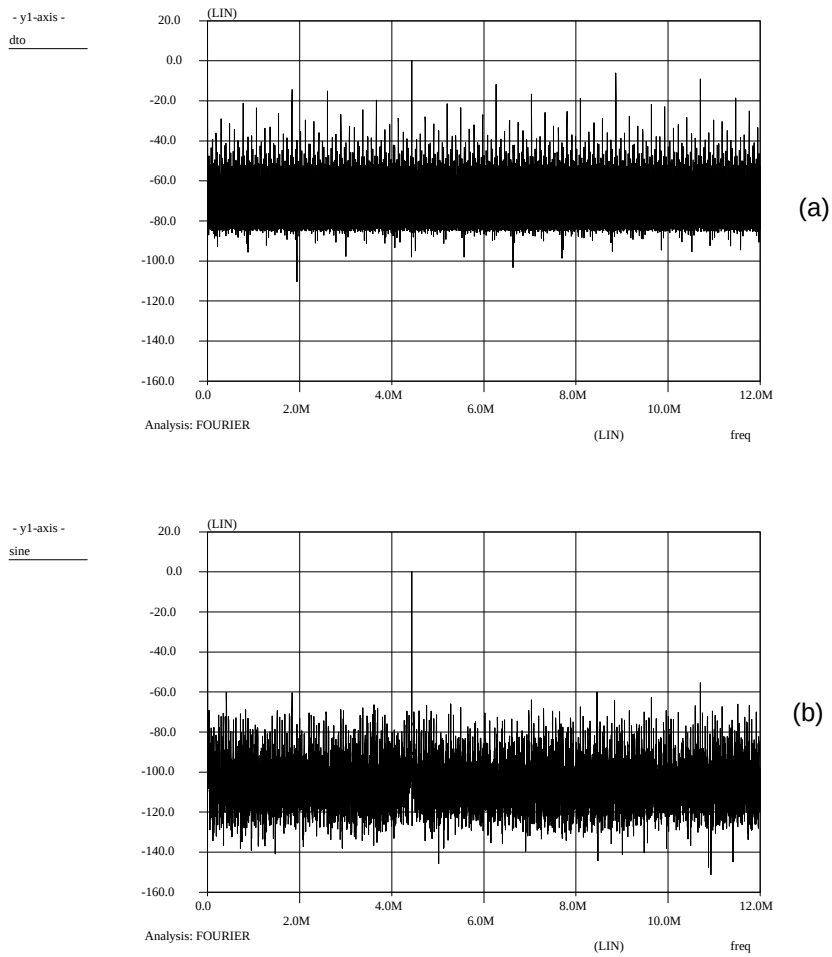


Fig. 73 Simulated spectrum at the output of
(a) the DTO and (b) the waveform translator.

this offset, the demodulation angle can be varied by adjusting the hue control word.

With the hue control word the phase offset must be controlled between -45^o and +45^o [43]. As the output signal of the DTO is ten bits wide, one period (360^o) of the sawtooth corresponds with 1024 different values. The required hue control range of 90^o corresponds to one quarter of a period. The maximum weight of the hue control word should therefore be 1024/4 = 256, so the hue control word must be eight bits wide.

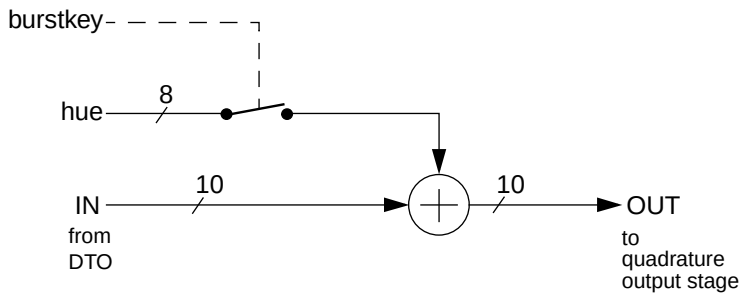


Fig. 74 Hue control stage.

Fig. 74 shows the block diagram of the hue control stage.

the input stage of the DDS

The DDS is adjusted to the desired subcarrier frequency by setting the input value K_{nom} of the DTO. This is done in the input stage of the DDS. The four values for K_{nom} for the four different colour carrier frequencies are listed in Table 9.

TV system	subcarrier	K_{nom}
NTSC-M	3.579545MHz	2502283
PAL-M	3.575611MHz	2499534
PAL-N	3.582056MHz	2504039
PAL-B,G,I	4.433619MHz	3099324

Table 9 K_{nom} values for the various TV systems.

In the input stage the selected 22-bit input value of K_{nom} is selected by a four-input multiplexer and added to the output signal of the digital loop filter (Fig. 75). The loop filter output fine-tunes the DDS for synchronisation to the received colour bursts. The specified tuning range of the DDS is +/-700Hz around the nominal subcarrier frequency. As the resolution of the DTO is 1.43Hz/LSB this corresponds to +/-490LSB. The output word width of the loop filter is therefore limited to ten bits.

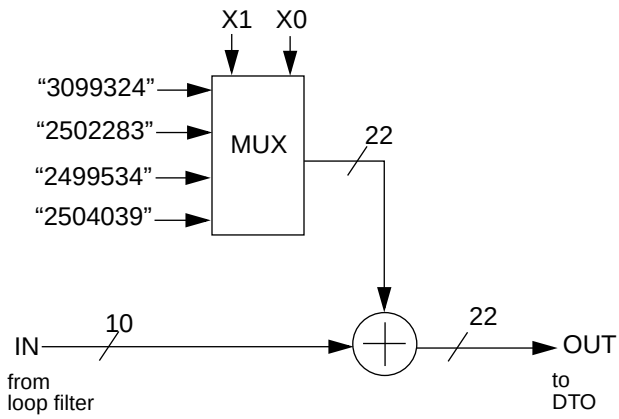


Fig. 75 Input stage of the DDS.

The digital loop filter requirements

After the output signal of the phase detector has been digitised by a sigma-delta modulator, the bitstream is processed by the digital loop filter (Fig. 65). Starting from the open-loop frequency characteristic of the analogue colour decoder PLL, six functions can be distinguished for the digital loop filter:

1) act as integrator for a (theoretically) infinite open-loop gain at DC to obtain a zero steady-state phase error (equivalent to C_1 of the analogue loop filter).

2) introduce a zero in the phase characteristic (equivalent to R of the analogue loop filter).

3) suppress the burst swing in the PAL mode (equivalent to C_2 of the analogue loop filter).

4) act as decimation filter for the conversion of the 24MHz bitstream from the sigma-delta modulator into low-pass filtered two’s complement digital words with the required resolution and a lower sampling frequency.

5) provide the colour decoder PLL with enhanced loop gain in the acquisition mode. In the analogue colour decoder the acquisition mode is switched on by increasing the gain of the phase detector. In this mixed-signal PLL the gain is increased in the loop filter.

6) limit the tuning range of the direct digital synthesiser to about +/-700Hz by limiting the output signal of the digital loop filter.

The loop filter configuration

The block diagram of the loop filter for the colour decoder PLL is shown in Fig. 76. In the first block the integrator and the decimation filter are combined to fulfil requirements 1 and 4. The PAL averager takes care of suppression of the PAL $f_H/2$ burst swing (requirement 3). The differentiator introduces a zero in the transfer characteristic (requirement 2). The tuning range of the DDS is restricted by the frequency limiter (requirement 6). Requirement 5 is met by switching the gain of the integrator/decimation filter under control of the colour killer.

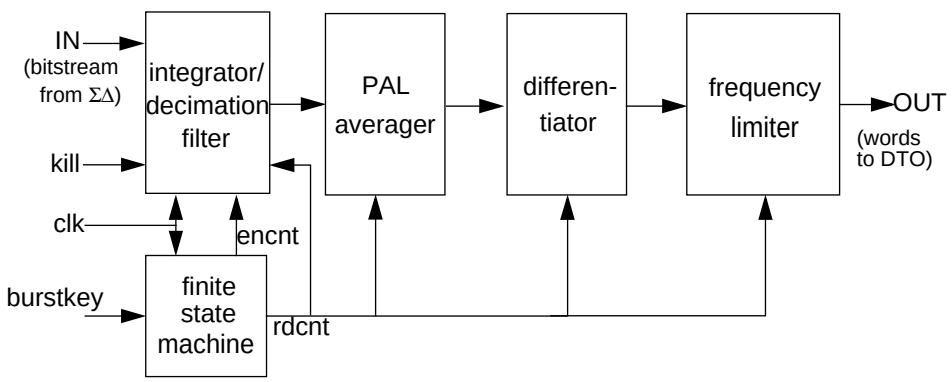


Fig. 76 Block diagram of the digital loop filter.

The combination of integrator and decimation filter is implemented by an up/down counter followed by a down-sample register (Fig. 77).

The first function of the up/down counter is to integrate the phase error. The bitstream controls the direction of the counting process; a digital ‘1’ increases the counter contents with 1LSB and a ‘0’ decreases the counter with 1LSB. As the counter is never reset, the low-frequency phase error coded in the bitstream is integrated in the counter.

A finite state machine (FSM) derives the encnt (enable counter) signal for the up/down counter from the burstkey pulse. The burstkey is a pulse that is high when the burst is present on the input signal. The reason why burstkey itself cannot be used will be discussed later. The finite state machine also generates the rdcnt (read counter) signal. This signal becomes active at the end of the encnt pulse. On this pulse all registers in the loop filter read the data on their inputs.

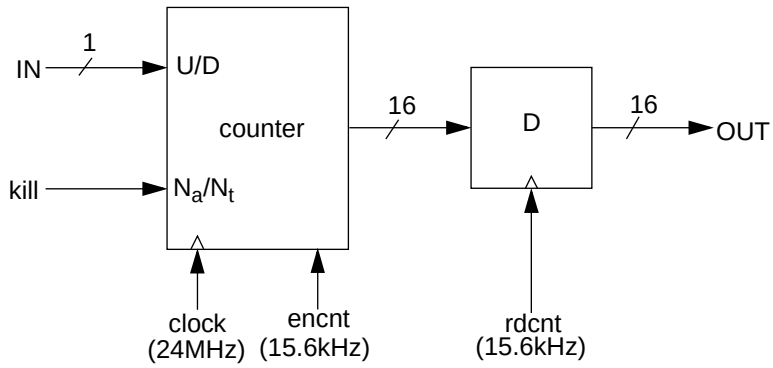


Fig. 77 Construction of integrator/decimation filter.

The kill control signal switches the step size of the counter between a low value (N_t) for the tracking mode and a high value (N_a) for the acquisition mode. In the test IC N_t can be either 2 or 4 and N_a can be either 8 or 16. This is for test purposes only, as the parameters of the analogue and digital systems can only be exactly identical be choosing awkward step sizes (see appendix D). In a final IC implementation the values for N_a and N_t will be chosen that give the most optimal overall system performance.

Apart from the integrating function, the up/down counter has a second function as a prefilter for the down-sampling process. The 24MHz single-bit bitstream is converted into digital words by the up/down counter and the quantisation noise in the bitstream is thus low-pass filtered. Fig. 78 shows how the bitstream of a first-order 1-bit sigma-delta modulator is integrated and low-pass filtered by the up/down counter. Fig. 78a is the spectrum at the input of the up/down counter. This is the spectrum of the bitstream coming from the sigma-delta converter. The analogue input signal of the converter is a 1kHz sine wave. Fig. 78b shows that the quantisation noise in the bitstream (which is mostly located at higher frequencies due to the noise shaping effect of the sigma-delta converter) is strongly suppressed by the up/down counter. A dynamic range well above 52dB (peak-to-peak signal to rms noise) is achieved with this configuration.

The signal at double the subcarrier frequency ($2f_{sc}$) that is also present at the output of the phase detector need not be filtered before digitisation by the sigma-delta converter. It will be coded into the bitstream and will be suppressed by the integrating action of the up/down counter.

When choosing a lower sampling frequency for the remaining part of the digital loop filter the maximum output frequency of the useful signal of the phase detector (and the sigma-delta

converter) has to be considered. This maximum is determined by the $f_H/2$ burst swing during PAL reception, which is 7.8kHz. As there are no signal components above 7.8kHz, the line frequency f_H = 15.6kHz was chosen as the sampling frequency of the digital loop filter.

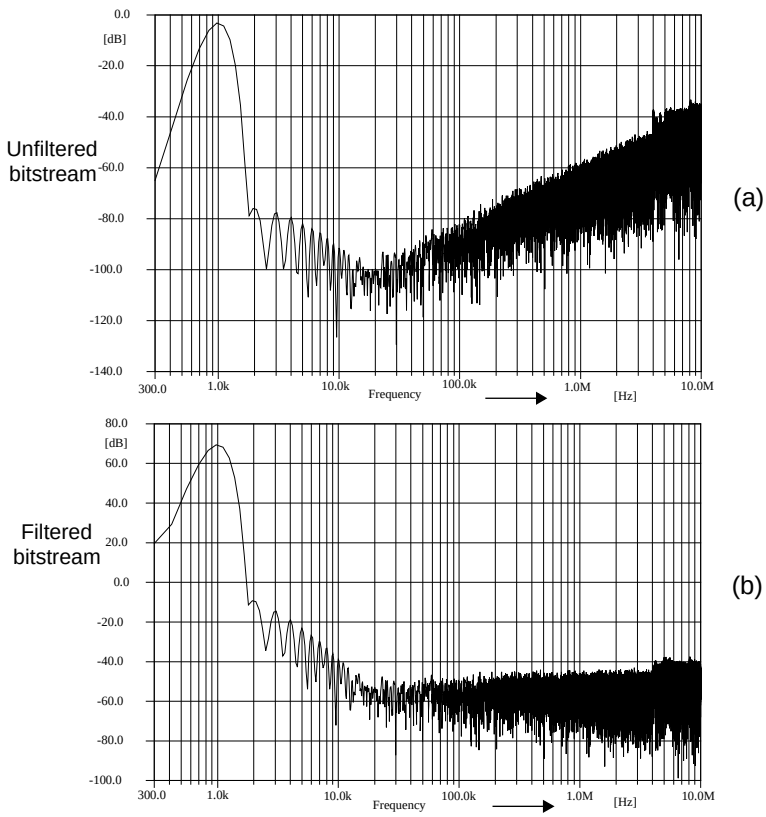


Fig. 78 Simulation of the filtering of the bitstream by the up/down counter: (a) input spectrum, (b) output spectrum.

avoiding quantisation noise due to the burstkeying process

The up/down counter is only activated during the burstkey interval. If the phase error is zero (steady-state situation) the nett result of the counting process can only be zero if the burstkey interval lasts an even number of clock periods. As the burstkey is generated by a circuit that is not using the same clock as the colour decoder, the burstkey itself cannot be used to control the down-sampling process of the up/down counter output. Therefore two timing sig-

nals are generated from the burstkey (Fig. 76 and Fig. 79). The signal encnt determines the time during which the counter is integrating the incoming pulses from the sigma-delta converter. The signal rdcnt is used to down-sample the up/down counter output and as the sampling frequency for the rest of the digital loop filter. Both encnt and rdcnt are derived from the burstkey pulse by a finite state machine. The encnt pulse, used to control the count enable input of the counter, is an internally synchronised version of the burstkey pulse that always contains an even number of periods of the 24MHz clock. Therefore the length of the encnt pulse is prolonged with one clock period if the number is odd (the situation shown in Fig. 79) The finite state machine also generates the rdcnt pulse that acts as a clock for the rest of the digital loop filter. The rdcnt pulse is high for one clock period directly after the end of the encnt pulse (Fig. 79).

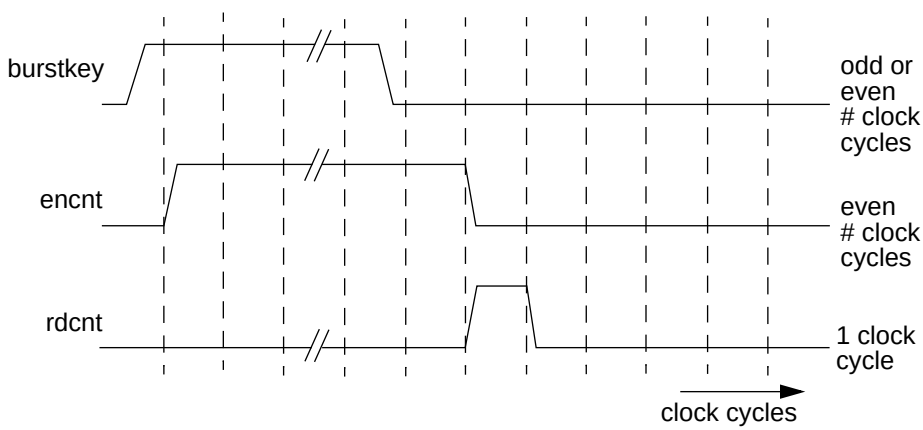


Fig. 79 Timing of the burstkey, encnt and rdcnt signal.

line averaging for PAL

In the analogue colour decoder PLL suppression of the PAL burst swing is obtained by low-pass filtering with an extra capacitor parallel to the loop filter. However, this capacitor gives a low phase margin in the acquisition mode (see Fig. 54). By using a line-to-line averager (Fig. 80) instead of a capacitor-equivalent in the low-pass filter, a better phase margin and a better suppression of the burst swing can be obtained (see appendix D). As two successive samples, with a time separation of one line time, are added in the averager, the gain for DC signals is two and the gain for signals having half the line frequency is zero. So the PAL burst swing, which has a frequency of $f_H/2$, is fully suppressed.

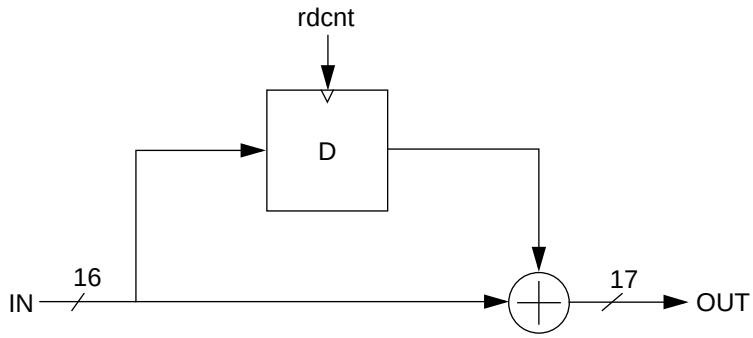


Fig. 80 Line-to-line averager.

the differentiator

The differentiator (Fig. 31) generates the required zero in the frequency characteristic of the PLL. The gain α_{df} of the delayed path, is one of the parameters that can be varied to obtain the desired transfer characteristic of the PLL. The limiter of Fig. 75 is implemented by sending only the ten least significant bits of the output of the differentiator to the input stage of the DDS.

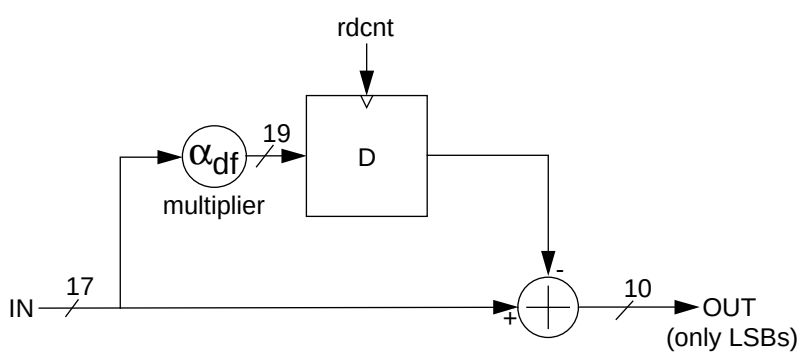


Fig. 81 Differentiator.

The sigma-delta converter

A sigma-delta converter (Fig. 82) converts the analogue input signal into a train of ones and zeros. If this train of ones and zeros is passed through an analogue continuous-time low-pass filter, the original analogue signal is retrieved.

The sigma-delta modulator which is used in this design is a simplified version of the sigma-delta modulator described in [66].

The subtractor in the configuration of Fig. 83 is implemented in the current domain. The original design has a voltage input and a voltage-to-current converter. As the input signal of the sigma-delta modulator is the output current of the phase detector, no voltage-to-current converter is needed in the colour decoder. The 1-bit DA converter is realised as a current source with a two-way switch. The fourth-order loop filter of the original design is replaced by a first-order loop filter (integrator). The loop filter is realised by connecting capacitor C between the current outputs of the subtraction point.

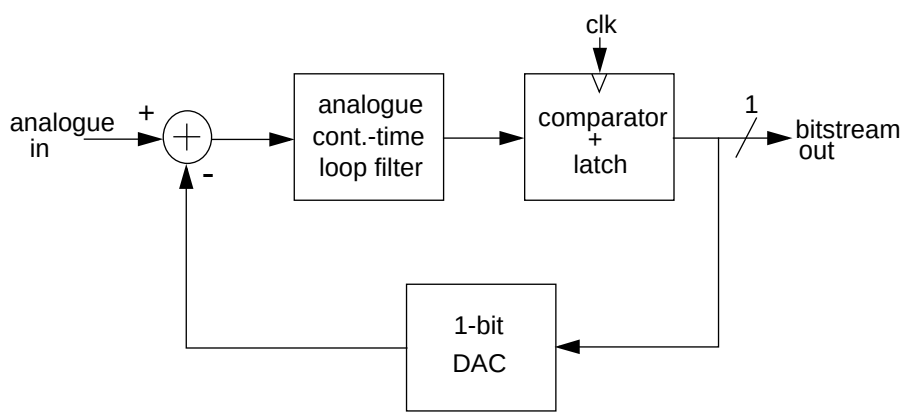


Fig. 82 Block diagram of a1-bit first-order sigma-delta modulator.

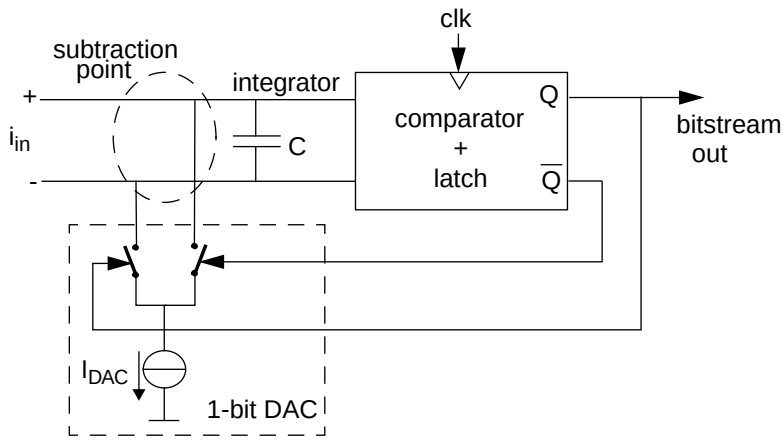


Fig. 83 1-Bit first-order sigma-delta modulator.

The DAC for the sine and cosine signals

As the DAC has only eight bits of resolution it can be made with emitter-scaling of fairly small bipolar transistors. The basic diagram of the DAC is shown in Fig. 84. The bias current is divided over a total of 255 emitters. The emitter of the transistor of the MSB consists of 128 unit-emitters. So T_7 will draw 128 times more current than the transistor of the LSB (T_0).

The INL and DNL of the DAC have to be less than 0.5LSB, i.e. the maximum allowable full-scale error is 0.2%. The weight of the LSB is MSB/128. As mismatch has a Gaussian nature, the mismatch in the LSB may be $\sqrt{128}$ times higher than the overall mismatch. So, the allowable mismatch for the LSB is approximately 2.2%. The maximum allowable mismatch of the LSB determines the size of the emitters of the transistors in the DAC. Taking the maximum allowable mismatch to be a 4σ spread, it follows that σ=0.55%. Applying the general mismatch rule for the collector currents [67], [68]

$$\sigma = \frac{A_{I_C}}{\sqrt{WL}} \tag{23}$$

and filling in the process data (A_{Ic}=1.6%μm) [68] it follows that W=L=3μm.

As the emitter size of the transistors cannot be chosen arbitrarily in the process (due to restrictions on the contact holes), and to keep the layout as small as possible, the size of the

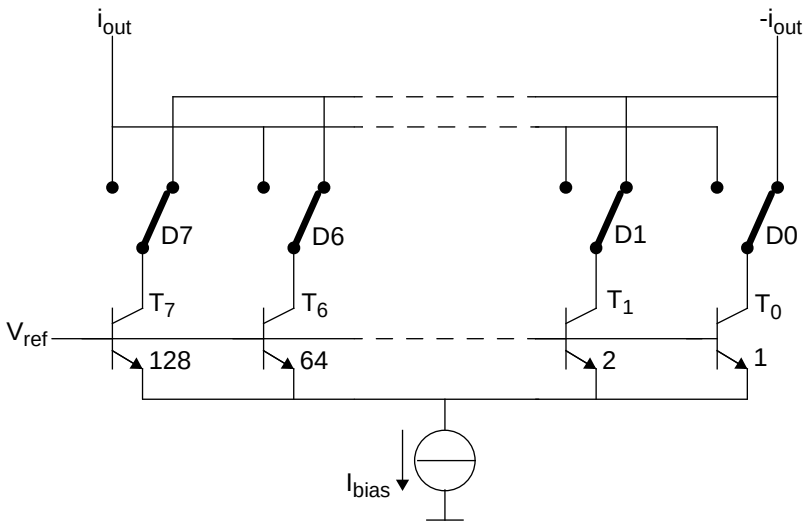


Fig. 84 Basic block diagram of the DA converter.

LSB transistor (T_0) was chosen 1.95*3.9µm, and all other transistors were made with unit-emitters of 3.9*3.9µm. In other words, T_0 has half a unit-emitter, T_1 has one unit-emitter, T_2 has two unit-emitters, etc.. Although the emitter size of T_0 is smaller than the calculated minimum emitter size, the overall inaccuracy of the DAC is less than 0.5LSB (see simulation result in Fig. 85). This is due to the fact that the unit-emitter size used in T_1 to T_7 is slightly bigger than the calculated value. The total emitter area in the DAC, however, is $(2^7\text{-}2)*3.9*3.9\mu m^2 + 1*1.95*3.9\mu m^2$ instead of $(2^8\text{-}1)*3.9*3.9\mu m^2$. So the area is only half of what it would be if T_0 had the same unit-emitter size as all other transistors.

The mismatch of the DAC was simulated by setting all bits, except the MSB, in a low state. The MSB was set in a high state. The spread of the differential output current of the DAC is shown in Fig. 85. The figure shows that one LSB step of the DAC is $3.9*10^{-3}$ (i.e. 1/255). The worst case spread is about $1.5*10^{-3}$. So, the spread is less than 0.5LSB.

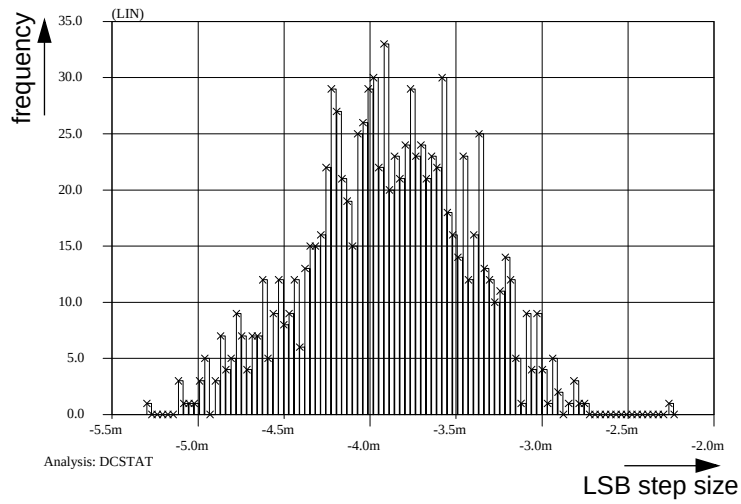


Fig. 85 Statistical analysis of mismatch in the DAC (simulation).

At low frequencies the DAC can easily achieve 8-bit accuracy, but at high frequencies the situation is completely different. The switches are made of two NMOS transistors (Fig. 86 shows the construction of one bit in the DAC), whose gates are driven with inverted signals, as only one of them has to be conducting at any one time. At 24MHz the delay time of one inverter (ca. 0.5ns) has a major influence on the glitches in the output currents as during the transition of the input data both NMOS transistors can be conducting or in the off-state simultaneously. These glitches will produce many unwanted frequency components in the output spectrum. Therefore the NMOS transistors are driven from the outputs of two flip-flops with inverted input signals.

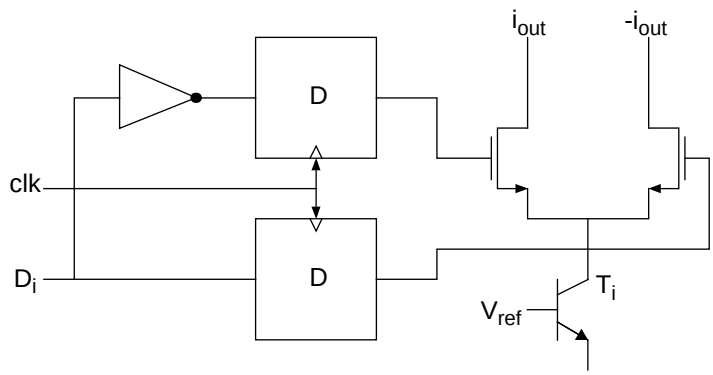


Fig. 86 Switch arrangement of one bit to minimise glitches.

The analogue low-pass filter

The DAC output signals are fed to low-pass filters. These filters have to eliminate the clock and its harmonics. This is important, because if there are spurious signals (e.g. crosstalk from the substrate) on the input signal, the clock and its harmonics will fold these spurious signals and noise back to the baseband, where they will pollute the colour difference output signals.

The output signal of the DACs is a current. So the low-pass filters must have a current input. The influence of the filter on the amplitude of a 4.4MHz sine wave must be negligible. A maximum attenuation of 0.5dB is allowable. The clock and its harmonics should be suppressed more than 55dB. This ensures that if there is crosstalk from the digital circuits to the input the colour decoder this will not result in visible disturbances on the TV screen. A ninth-order filter would fulfil both requirements.

If the multipliers in the demodulators are linear enough, and if the crosstalk from the substrate is kept low enough, the demands on the clock elimination needn't be so strong. As a compromise between cost and performance a third-order Sallen and Key filter was chosen. The filter does not have a control of the cut-off frequency, which means that the cut-off frequency must be chosen such, that even with the worst case spread, the 4.4MHz sine wave is attenuated by less than 0.5dB.

Fig. 87 shows the diagram of the low-pass filter. The DACs have a differential output current, but the low-pass filter is not a truly differential filter. Both output terminals of one DAC are fed to two identical low-pass filters, so that the combination of the output signals of the

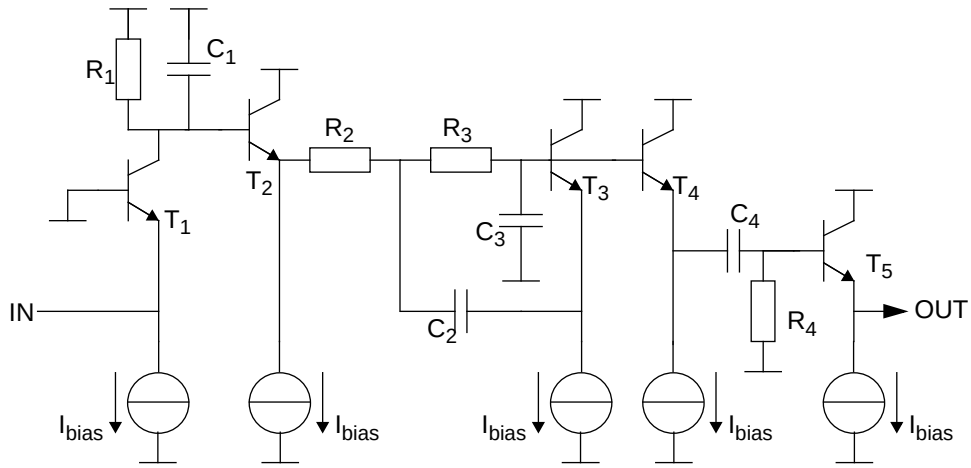


Fig. 87 Low-pass filter.

low-pass filters is quasi-differential. The current from the DACs is fed to the actual filter through a cascoding transistor (T_1). This transistor must be part of the filter and not the DAC, as otherwise the parasitic collector-substrate and collector-base capacitances of the DAC transistors and the wiring would influence the transfer characteristic of the filter. As the modulation depth of the DAC output current is 100%, there are points in time where the current from one of the output terminals of the DAC is zero. If there is no current flowing through the cascoding transistor T_1, it will be very slow. This will degrade the input signal of the actual filter. Therefore a DC current (I_{bias}) is added to the outputs of the DACs to keep the cascoding transistor fast.

The output of the low-pass filter is taken from the base, not the emitter, of the emitter follower (T_3) that is in the feedback loop of the filter. A second emitter follower (T_4) makes sure the output impedance is still low. This construction has the advantage that the suppression of very high frequencies is far better than if the emitter of T_3 is taken as the output. The reason for the bad suppression of very high frequencies is that the suppression is limited by the emitter impedance of T_3. At very high frequencies the transfer is determined by the ratio of R_2 and the emitter resistance of T_3.

As the offset on the inputs of the multipliers must be very low to prevent subcarrier breakthrough to the output of the demodulator, the outputs of the Sallen and Key filters are AC coupled to them. After the AC coupling capacitor there is an emitter follower. One emitter follower produces only little offset, and if the follower weren't there, the parasitic capacitance of

the inputs of the multipliers would cause an attenuation of the colour carrier. This is unacceptable, as it would cause a lot of spread on the amplitude of the demodulated chrominance signal.

The multipliers

As Fig. 65 shows, three multipliers are needed in the mixed-signal colour decoder. Two of these produce the output colour difference signals. The third multiplier closes the loop of the PLL.

the demodulating multipliers

The two multipliers in the colour demodulator, that produce the colour difference signals at their output, use the topology of the Gilbert gain cell [69]. Fig. 88 shows the basic configuration.

In the analogue demodulator the multipliers that produce the R-Y and B-Y output signals are effectively rectifiers. This means that output signals of the oscillator are connected directly to the bases of the four upper transistors of the right-hand stage of Fig. 88. In the new system the outputs of the low-pass filters at the output of the DDS do not have high enough a suppression of the clock frequency to use rectification instead of linear multiplication. Using a

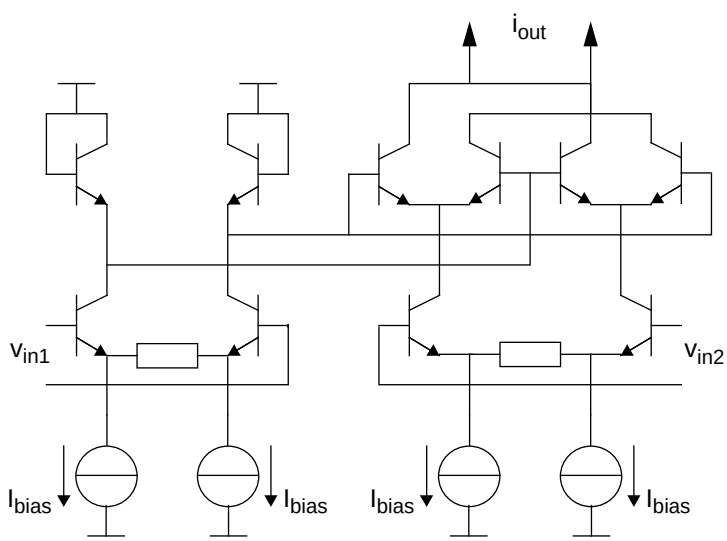


Fig. 88 Multiplier.

higher-order filter is possible, but this would require considerably more silicon area than the linearisation of the multiplier. With a linear multiplier (crosstalk) frequencies on the input signal, that are around the clock frequency, are not folded back to the baseband.

the multiplier in the phase detector

In the analogue as well as the new system, the multiplier that acts as the phase detector is a multiplier with a high gain on both inputs. So the multiplier is in effect a switching phase detector and not a linear phase detector [40]. Compared to the topology of the multipliers described above, this means that the left-hand amplifier is omitted. The input signal is fed directly to the bases of the upper four transistors of the right-hand amplifier. The resistor between the emitters of the lower transistors is replaced by a wire.

Simulation results of the complete PLL

The transfer of the mixed-signal PLL of the colour decoder is calculated is appendix D. Fig. 89 shows the simulated open-loop transfer characteristics of the mixed-signal colour decoder. The transfer is given for four different gain values: $A_{cnt} = 2$, $A_{cnt} = 4$, $A_{cnt} = 8$, and $A_{cnt} = 16$. Comparing this transfer with that of the analogue system (Fig. 54), it can be seen that for an identical transfer in the tracking range the optimum value of A_{cnt} lies between $A_{cnt} = 2$ and $A_{cnt} = 4$. For the acquisition range the optimum value of A_{cnt} lies between $A_{cnt} = 8$ and $A_{cnt} = 16$. This is in agreement with the calculation of appendix D.

For $A_{cnt} = 16$ the phase margin is 45^{o}. This is slightly better than the 37^{o} phase margin of the analogue system.

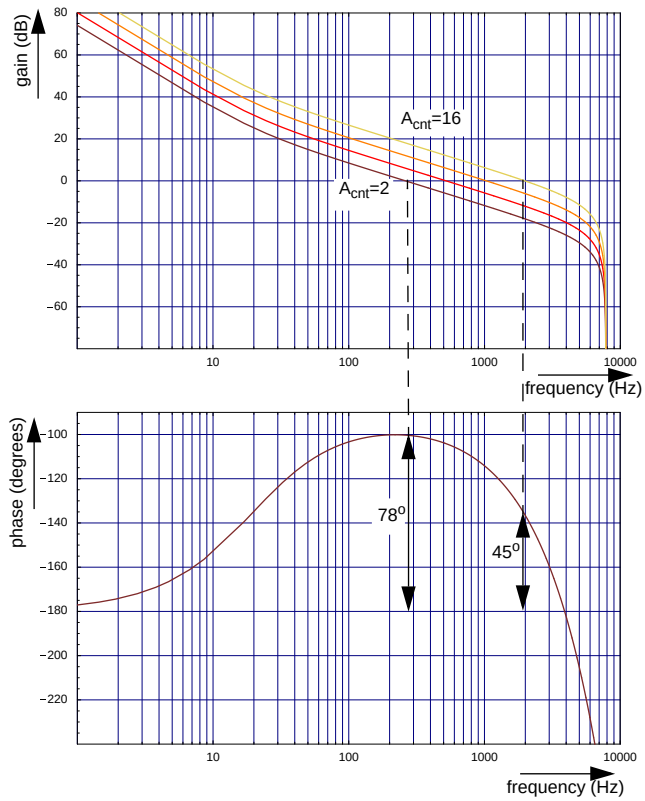


Fig. 89 Simulated open-loop transfer characteristics of the mixed-signal colour decoder for A_{cnt} = 2, A_{cnt} = 4, A_{cnt} = 8, and A_{cnt} = 16.

Fig. 90 shows the reponse on a 90^{o} phase step. The conclusions of the simulation of the open-loop transfer characteristics are also true for this simulation.

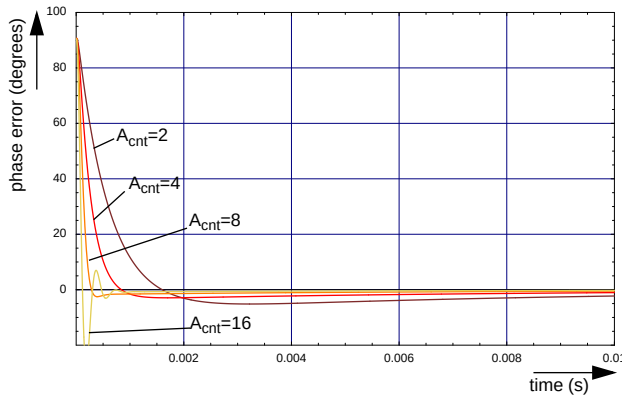


Fig. 90 Simulated transient response for a 90^{o} phase step on the input signal for A_{cnt} = 2, A_{cnt} = 4, A_{cnt} = 8, and A_{cnt} = 16.

Circuit realisation

A test IC with the mixed-signal colour decoder has been fabricated in a 0.6µm BiCMOS process [68]. The test IC also contains a number of additional circuits like lock detectors. Fig. 91 shows a photograph of the test IC. The area of the analogue circuits (without the additional circuits) is $0.5mm^2$. The area of the digital circuit is $1.1mm^2$. The area of the digital circuit was not optimised to shorten the layout time. An optimised layout of the digital circuit would occupy an area of $0.5mm^2$.

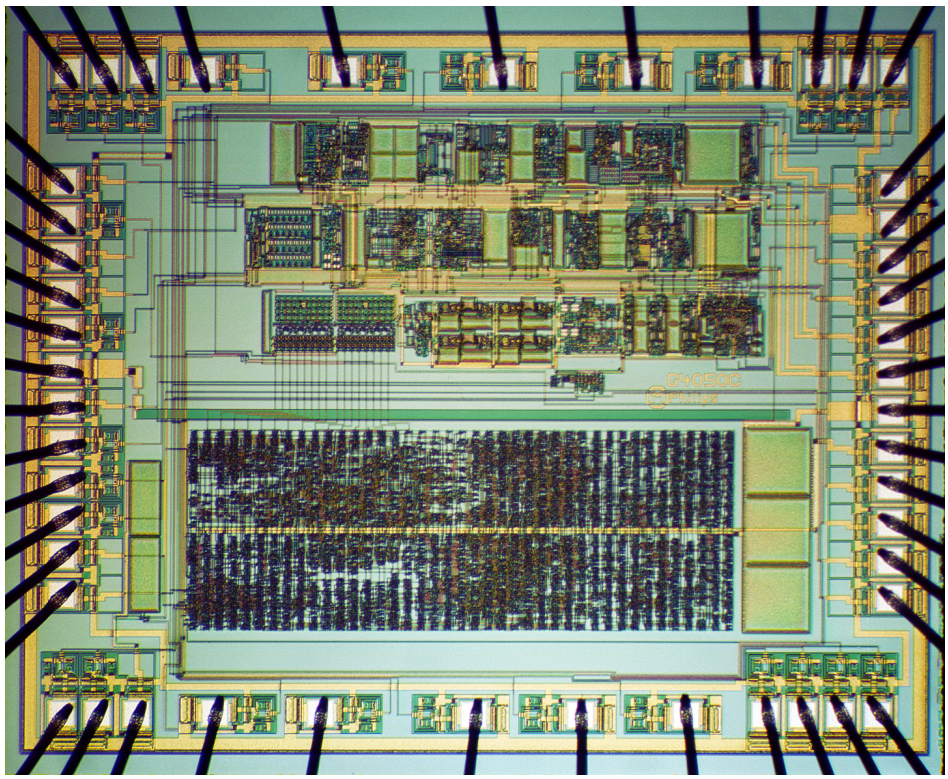


Fig. 91 Test IC of the mixed-signal colour demodulator.

Measurement results

All measurements described in this section were performed with a 4.43MHz colour carrier frequency. Changing the frequency does not change the results significantly.

spectrum of the sine wave at the output of the low-pass filter

Fig. 92 shows the measured spectrum of the sine output of the DSS after digital-to-analogue conversion and low-pass filtering. The highest spurious is more than 55dB down with respect to the colour carrier frequency. This is in good agreement with the simulation (Fig. 73).

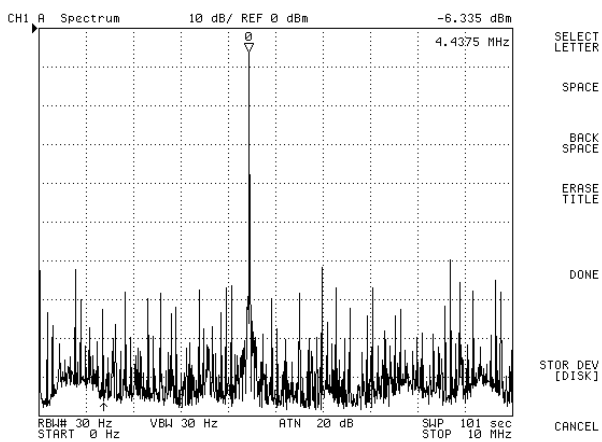


Fig. 92 Measured spectrum of the sine output of the DDS after digital-to-analogue conversion.

response on EBU colour bar input signal

Fig. 93 shows a PAL CVBS input signal and the colour difference output signals. The averager of the mixed-signal system completely eliminates the H/2 ripple due to the burst swing: the shape of the colour difference signals of two consecutive lines is exactly identical. The analogue system (Fig. 52) does show some H/2 ripple, despite the addition of C_2 to the PLL loop filter.

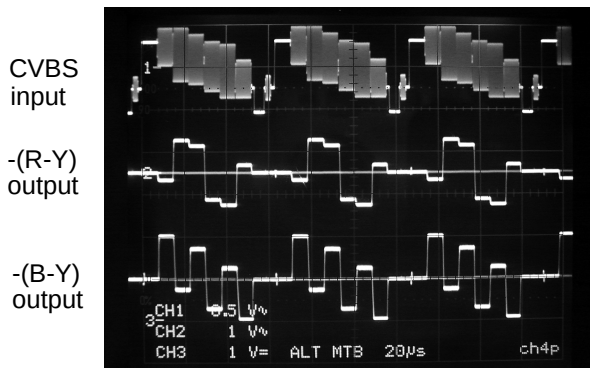


Fig. 93 CVBS input signal and colour difference output signals.

output spectrum with a continuous 4.43MHz input signal

Fig. 94 shows the spectrum of the -(B-Y) output signal of the test IC when a continuous 4.43MHz sine wave is fed to the input of the colour decoder. With such an input signal, the -(B-Y) output signal is a DC signal and a signal at 8.86MHz with an amplitude equal to the DC component ($2\sin^2(\omega_{sc}t) = 1 + \sin(2\omega_{sc}t)$). The spectrum analyser does not give a correct reading for DC signals, so the 8.86MHz signal must be used as the reference to see how much the spurious signals in the passband are down with respect to the signal. In this experiment the -(B-Y) signal is passed through a 1.5MHz first-order low-pass filter, instead of the normal third-order filter, before it is fed to the spectrum analyser. As a result the measured 8.86MHz component is suppressed by 11dB.

From this spectrum it can be concluded that the frequency components in the passband (0 to 1.5MHz) of the colour difference signals are more than 55dB down with respect to the unattenuated -(B-Y) signal. The spurious frequencies outside the passband are also below -55dB with respect to the unattenuated -(B-Y) signal. The latter spurious frequencies will be suppressed to an even lower level by the third order 1.5MHz low-pass filter at the output of the colour decoder.

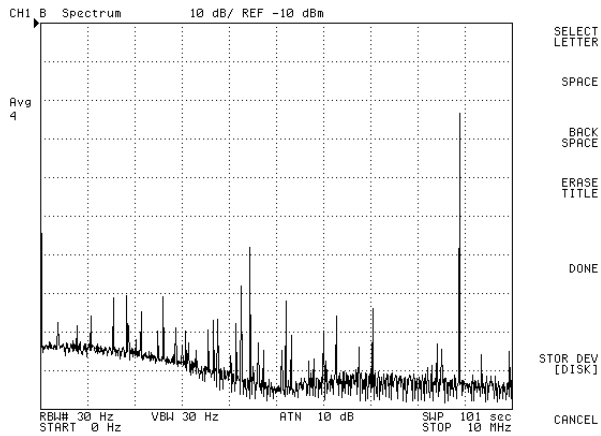


Fig. 94 Measured spectrum of the -(B-Y) output for a continuous sine input signal.

dynamic behaviour of the colour demodulator PLL

Fig. 95 shows the response to a 90^{o} phase step on the input burst signal. The value of A_{cnt} has been set to $A_{cnt} = 4$ in this measurement. This response is measured on the -(B-Y) output. The horizontal lines that are also visible in the photograph are the burst and blanking levels of the -(B-Y) signal. These levels are not relevant in this measurement. The measurement is in close agreement with the simulation of Fig. 90. The measurements for the other values of A_{cnt} are also close to the simulated response.

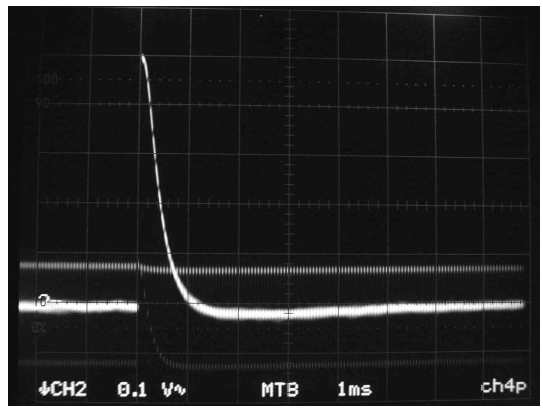


Fig. 95 Response to a 90^{o} phase step on the burst.

other measurements

Table 10 summarises the measurement results.

supply voltage	5V
supply current	5.0mA (analogue) 2.1mA (digital)
circuit area	0.5mm^2 (analogue) 1.1mm^2 (digital) 0.5mm^2 (digital, after optimising layout)
centre frequency	3.579545MHz (NTSC-M) 3.575611MHz (PAL-M) 3.582056MHz (PAL-N) 4.433619MHz (PAL-B,G)
acquisition/tracking range	+/-720Hz (all standards)
static phase error	0.5^{o}
signal-to-noise ratio (V_{pp} to rms noise, 1.5MHz bandwidth)	54dB (B-Y output) 55dB (R-Y output)

Table 10 Measurement results of the mixed-signal colour demodulator.

From the above measurements it can be concluded that the new mixed-signal colour decoder has a performance which is nearly identical to the performance of the traditional analogue system [43].

The colour decoder in a one-chip TV processor

The test IC described above was made as this makes it easy to measure the performance of the colour decoder and its component parts. The mixed-signal PLL has also been introduced (with some modifications to comply with customers' demands) in a family of one-chip TV processors [71]. Fig. 96 shows a die photograph. The measured performance of the test IC described above and the colour decoder in the one-chip TV processor is identical. The other circuits in the one-chip TV processor have no measurable influence (e.g. due to crosstalk) on the performance of the colour decoder circuit.

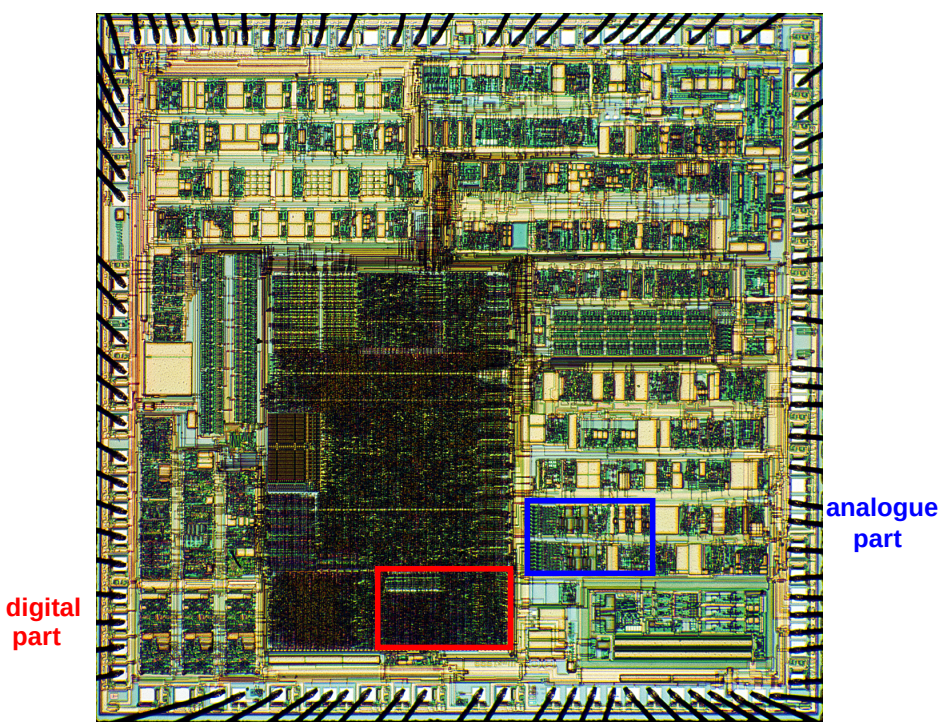


Fig. 96 Die photograph of a one-chip TV processor with the mixed-signal colour decoder.

Conclusions

A mixed-signal colour demodulator system with a topology based upon an analogue system has been presented. The performance of the new system is nearly identical to that of the traditional analogue system. The mixed-signal demodulator system combines the best elements of the analogue and digital worlds. The signal path is completely analogue, so no high-performance ADCs are needed. The link from the analogue to the digital domain is a simple one-bit sigma-delta converter that only has to convert a quasi-DC signal. The total system cost is reduced considerably thanks to the elimination of a number of expensive external components.

chapter 5

Analogue VLSI testing

Introduction

One of the aspects of analogue IC design that is very often neglected is testability. During the production process each IC is tested twice: The first time on the wafer to select good ICs for encapsulation (wafer testing). After encapsulation the ICs are tested again (final testing) to make sure that no fault has been introduced during the encapsulation process.

Testing of the ICs before encapsulation is necessary, as the manufacturing process of an IC consists of many hundreds of steps. All these steps (e.g. implanting, cleaning, lithography) have to executed without any inhomogeneity or impurity in the chemical substances and equipment that are used in these process steps. Small inhomogeneities or impurities can cause defects in the components in the ICs on the wafer (or in the connections between the components). Encapsulating an IC is rather costly, so only good ICs should be encapsulated.

Testing an IC does not add value to it. Customers pay for the function(s) in the IC and simply expect only good ICs to be delivered to them. Therefore testing should be as cheap as possible. This implies that the equipment used for testing should be as simple as possible. And the time it takes to test one IC should also be as short as possible.

In the digital IC design world formalised test approaches exist (e.g. scan testing [72] and I_{DDQ} testing [73]). These tests do not check the function of the IC, but they check whether the network of the components in the IC is correct. No such formalised techniques exist for analogue ICs. Analogue testing is usually functional testing: real time testing with signals as they are applied in a standard application.

Table 11 gives an overview of the differences between analogue and digital testing.

Digital	Analogue
Scan, I_{DDQ} -- short test time -- simple test board	Functional test -- real time test -- “application” test board
Generic structural test	Application-like test
When specified faults are absent, IC ***is*** very likely to be ***good***	When function is performed well, IC ***is not*** likely to be ***bad***

Table 11 Comparison of digital and analogue testing.

These differences lead to a substantial difference is the IC-specific hardware that is required to test an IC. For digital ICs a simple test board with few components can be used (Fig. 97a). For analogue circuits the test board is effectively an application board, with extra facilities (e.g. switches) to allow injection of test signals and observation of output signals. As Fig. 97b shows, such an analogue test board is far more complicated (and hence more difficult to design and build) than a digital test board. One of the reasons why it is hard to design a good wafer test board, is that the leads from the bondpads to the board are far longer than the bond-wires in an IC encapsulation. This makes decoupling of supply pins and high-frequency operation difficult.

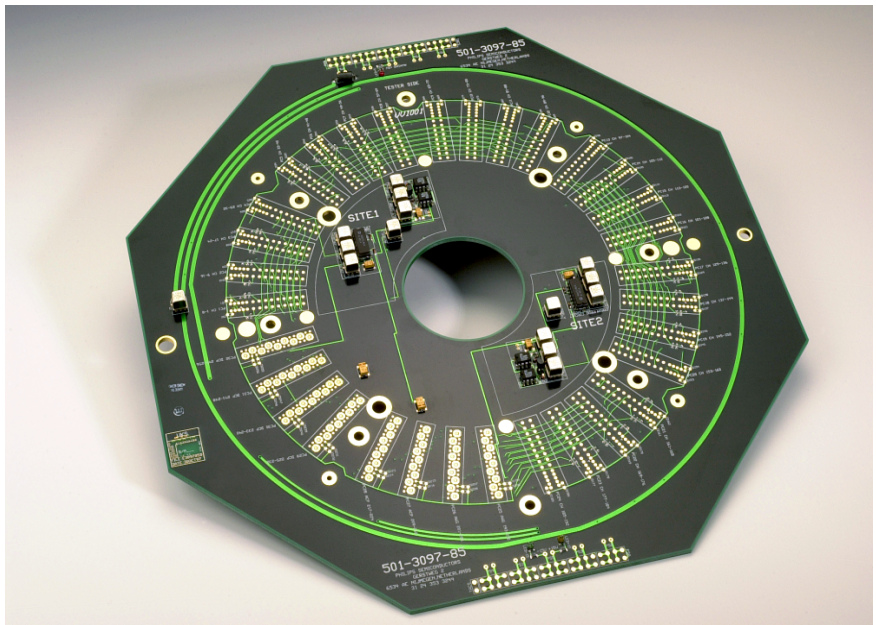
The aim of the research described in this chapter was to come to a fast, generic test method for analogue VLSI ICs that finds as many faulty ICs as possible. The ultimate goal would be to completely eliminate the need for functional testing. The test method for analogue VLSI described in this chapter is generic and does not require changes to the circuits inside the IC. This test method determines whether an IC is good or not by measuring the currents flowing through its constituent circuits. The test method was christened I_{CCQ}[1] as it bears some resemblance to I_{DDQ} testing.

Functional and non-functional IC test methods

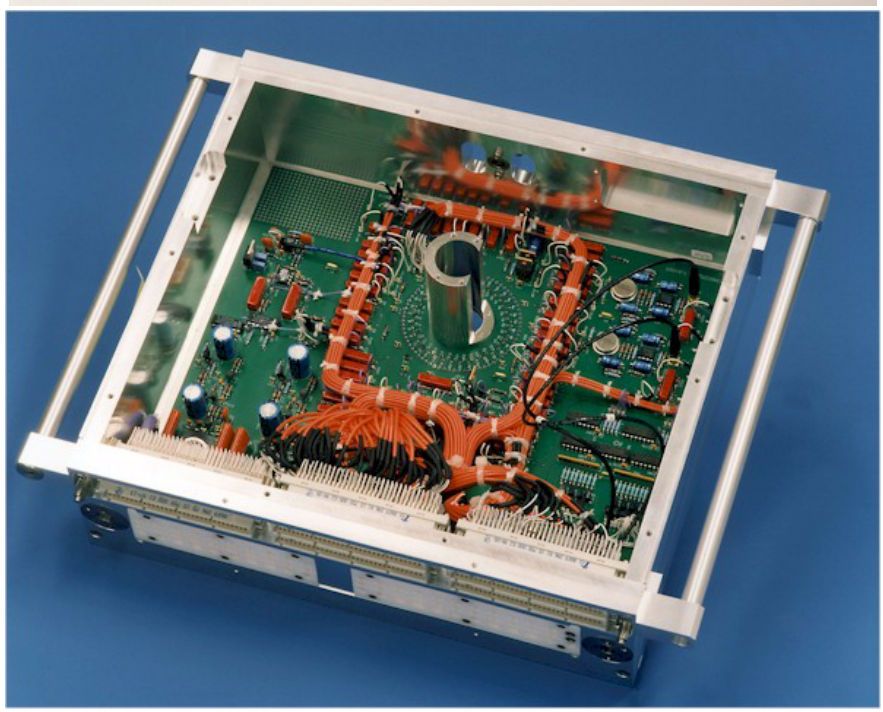
In this section a number of (non)-functional test techniques is described. All these test methods have their pros and cons. After the description of the I_{CCQ} method the pros and cons of the techniques described in this section will be compared with those of I_{CCQ}.

In digital CMOS circuits I_{DDQ} testing is used as a global test to see if unwanted current

1. The abbreviation I_{DDQ} stands for “test of the Quiescent I_{DD}”. The abbreviation I_{CCQ} stands for “test of the Quality of I_{CC}”, I_{CC} being the designation of analogue supply current. I_{CCQ} is not limited to quiescent I_{CC} testing. It can also cope with a dynamic I_{CC}.



(a)



(b)

Fig. 97 Comparison of typical wafer test boards: (a) digital, (b) mixed-signal.

flows somewhere in the IC, when the clocks are switched off. If that turns out to be the case the IC is rejected. This test is global and not spec oriented, but does provide a quick and effective sieve to detect faulty circuits [73].

In some digital circuits Built-in Current (BIC) testing is used to check the quiescent currents [74]. This technique, which can be regarded as a refinement of I_{DDQ} testing, uses a resistor in the ground rail to convert the ground current to a voltage. In the normal operating mode this resistor is short-circuited. In test mode the voltage across the measuring resistor is compared with some reference voltage. If the quiescent current is greater than the reference the IC is rejected.

Macro-based testing [75] is a formalised way to test blocks in an analogue IC by feeding signals to the input of each block and observing their output signals. If all blocks are good, the IC is considered good.

In [76] an analogue scan test technique is proposed. In this technique the outputs of analogue circuits inside the IC are sampled at regular intervals. These samples are subsequently shifted to a test pad through an analogue shift register. In the test equipment the actual values of the samples are compared with the expected values, and based upon that the IC under test either passes the test or is rejected.

Macro-based testing and analogue scan testing are in fact closely related to functional testing. These test methods alleviate some of the problems caused by the ever-growing complexity of analogue ICs. Research on true non-functional tests for analogue circuits has also been reported.

Oscillation-based testing [77] is a test technique that, during testing, connects the analogue circuits in an oscillator structure in such a way that the oscillation frequency indicates whether the circuit is good or not. This method is proposed as a Built In Self Test (BIST).

Most of the research on non-functional testing centres on supply current testing. A good overview of these methods is given in [78]. The conclusion of this paper is that with current testing a significant part of the defective ICs can be detected. However, with current testing not all faulty ICs can be found, as changes in the supply current are mostly caused by shorts or opens in the routing layers. This kind of defect often causes a so-called catastrophic failure, i.e. as a result of the defect the IC no longer performs the desired function. Parametric faults (i.e. a fault that causes e.g. the gain of an amplifier to be 10dB instead of 20dB) are not always detectable by a variation of the supply current. The shorts and opens in the routing layers, as well as other defects that cause the supply current to deviate from its nominal value, can sometimes be detected more easily by not testing with the nominal supply voltage, but by using a supply voltage outside the normal operating region [79].

Current testing in analogue ICs

In analogue circuits the I_{DDQ} technique as used in digital CMOS ICs is not applicable. Analogue circuits rely on the presence of a bias current for a correct operation. When testing analogue ICs the supply current is measured to get a rough indication whether the IC is good or not [78]-[79]. However, with this technique the supply current of the whole IC is measured. So if a circuit that draws 1% of the supply current is 50% off target due to e.g. a processing defect, the supply current of the whole IC will change by only 0.5%. As the spread of the current due to process variations within one wafer is of the order of 1%, a variation of 0.5% is too small to justify rejection of such an IC.

Fig. 98 shows the effect of a defect on the current of an IC. In the figure the current distributions as a result of process spread of three circuits in good ICs are shown, as well as the dis-

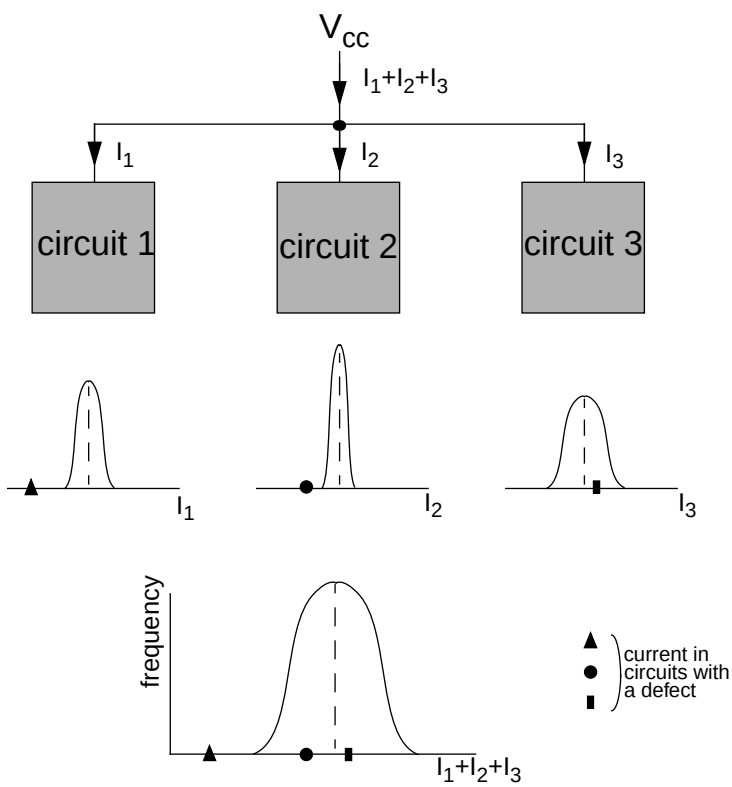


Fig. 98 Distribution of the supply current in an IC and the distribution of the total current. The supply current of three individual circuits with a defect is also indicated.

tribution of the sum of these currents. In the current distribution curve of each circuit, the current of a circuit with a defect in it is indicated. The current as a result of the defect in circuit 1 has a large deviation from its nominal value (solid triangle). In circuit 2 the defect causes the current to be just outside the range of the nominal current (solid circle). The current of circuit 3 is within its normal distribution despite the fact that it has a defect (solid rectangle). If the sum of the currents of these three circuits is measured on the supply pin, only the large defect of circuit 1 can be detected. The defects of circuit 2 and 3 cause a deviation of the total IC current that is still within the normal distribution of the total device current.

The most ideal form of current measuring technique would be to monitor each current branch separately. This is usually impossible due to the large amount of current branches. It would be helpful though if as many currents could be monitored as is still practical. Using several bond pads to connect to each supply or ground pin is a way to increase the number of observable currents at pretesting. However, the number of bond pads is limited to about five pads per ground/supply pin. More than five bond wires simply do not fit on the leadfinger of the encapsulation. So, if more current sensing points are needed, something extra will have to done inside the IC.

Simulations

In order to see whether measuring currents is an effective method to detect faulty ICs, simulations were done on a part of an IC. This IC is running in production, so it is not a circuit especially designed for this test. The simulation was done with a computer program called DOTSS (Defect Oriented Test Simulation System) [80]. This program takes the layout of a circuit and randomly places defect particles in it. These defects can be e.g. dust particles, pinholes in oxide that fill up with metal, or any other effect that causes a short circuit between two interconnection lines in the IC. The number, size and the size-distribution of the defect particles are taken from factory data. The program assumes that a particle causes a short circuit if (a) the particle overlaps two or more interconnection lines (bridging defect in one interconnection layer), or (b) the particle is situated between two interconnection lines in different interconnection layers (pin-hole defect between two interconnection layers). Only the interconnection masks are used to introduce the defect particles. It is also assumed that a particle cannot cause an interruption of the metal lines. This assumption should not affect the accuracy of the simulations too much, as factory data shows that the vast majority of rejected ICs are rejected as a result of short circuits in the interconnection layers [81].

Fig. 99 illustrates the way the program works. The top-left shows the layout of the circuit. To this layout defect particles are added with a certain distribution depending on the particle-size (top-middle). This results in a modified layout as shown in the top-right. The shorts that the particles cause in the layout are translated back to the electronic circuit. Bottom-left

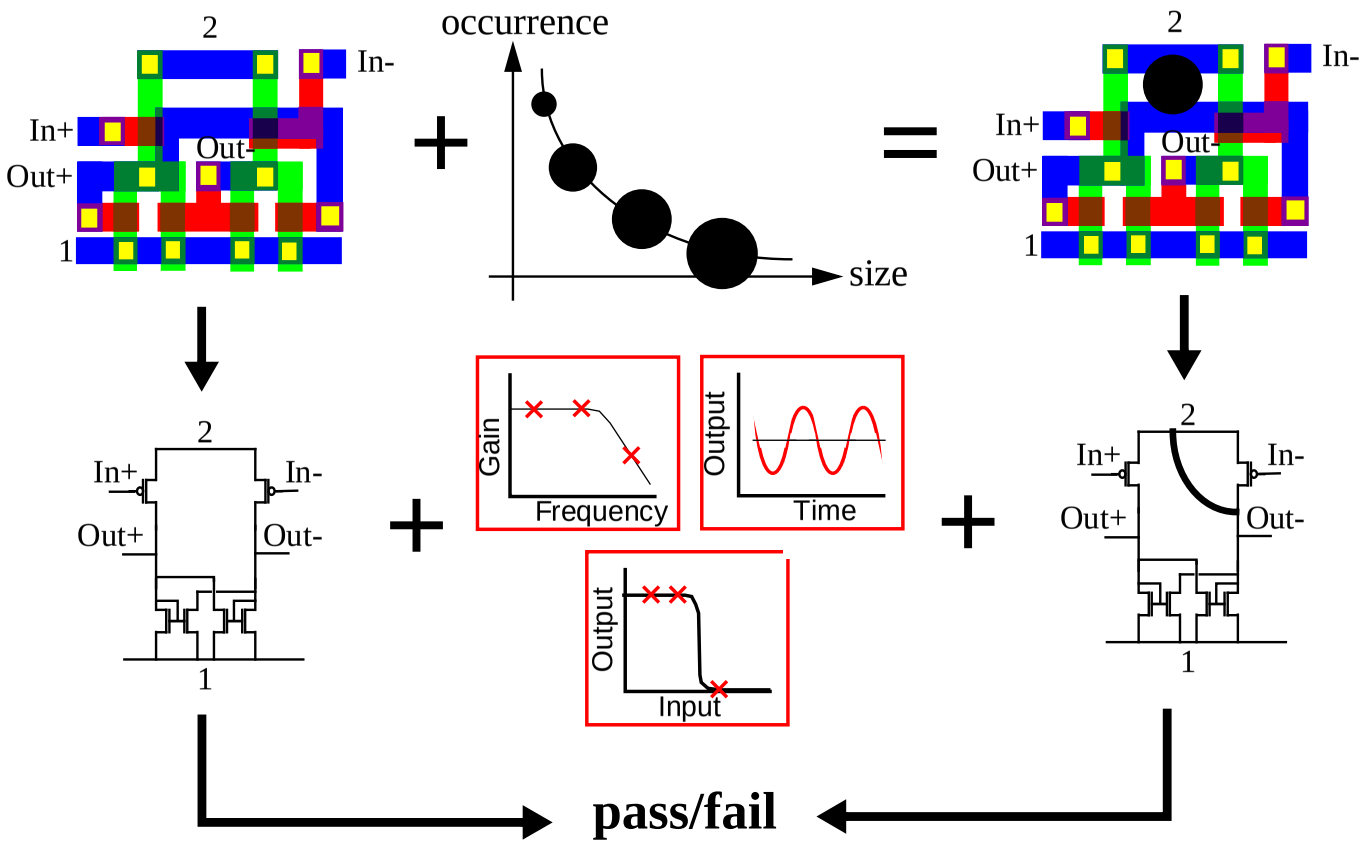


Fig. 99 Idea behind DOTSS.

shows the defect-free circuit, bottom-right the circuit with the shorts. The two resulting circuits can now be compared with a circuit simulator. The performance can be compared for DC, AC and transient responses.

current distribution due to defects

With DOTSS the DC current through a number of circuits was analysed. Fig. 100 shows the simulated currents through two different circuits for nominal process parameters. The DC

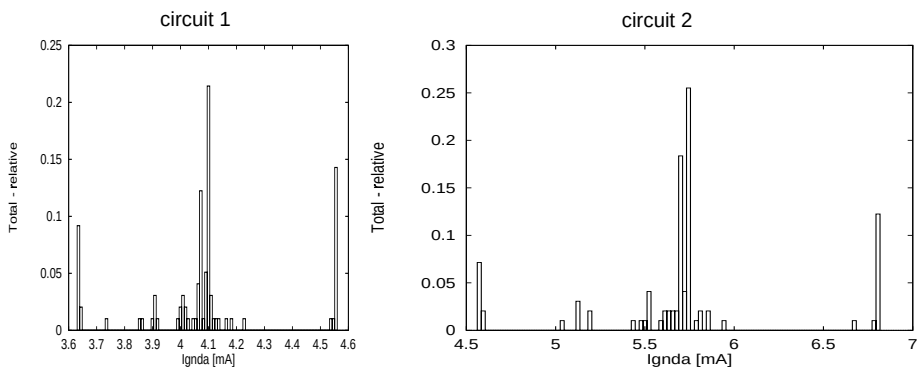


Fig. 100 Simulated current distribution with randomly introduced defects for two different circuits.

current was determined for 200 different defects, i.e. 200 times a defect was randomly introduced in the circuit. Some of these defects will not cause a short circuit (e.g. because they lie between two metal lines without touching them), so they actually do not introduce defects into the IC. Others will cause short circuits but do not influence the DC current (e.g. a short-circuit of the outputs of a differential amplifier). But many defects will cause a short-circuit and change the DC current as can be seen in Fig. 100.

The routine described above was applied to 14 different circuits of the aforementioned IC. Fig. 101 lists the names of the circuits and shows the percentage of ICs in which these circuits have a current that deviates more than 5% and 10% from the nominal current. This means that for e.g. the circuit called BRCON 40% of the circuits with a defect are detected if a circuit is rejected if its current is more than 10% higher or lower than the nominal current. If a circuit is rejected if its current is more than 5% higher or lower than the nominal current, 47% of the circuits with a defect are detected.

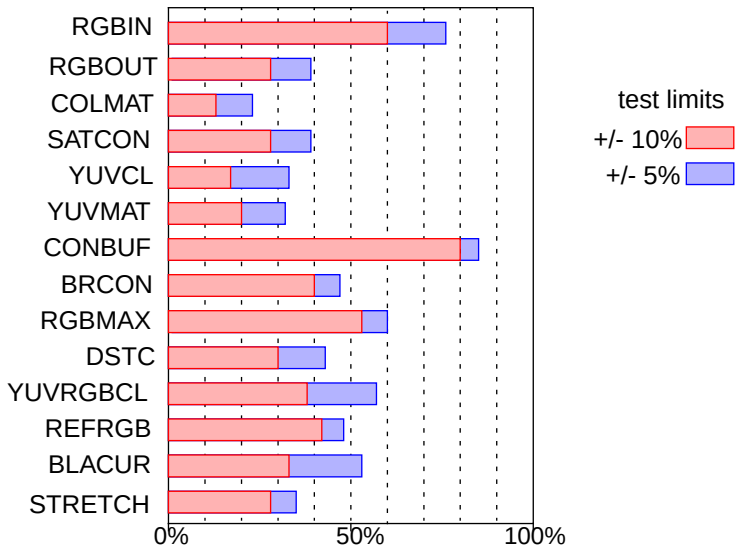


Fig. 101 Simulation on 14 different circuits in one IC showing the percentage of circuits that have more than 5% or 10% deviation from the nominal current due to defects.

current distribution due to process spread

Fig. 102 shows the effect of process parameter spread on the same two circuits as the ones analysed in Fig. 100. The distribution of the current due to process parameter spread is of the same order as the distribution due to defects. From this it follows that measuring the DC current of a circuit is not sufficient to say whether or not it has a defect. Results similar to the ones above have been reported in the literature [82].

reject criterion based on current measurements

The fact that the absolute current flowing in a circuit doesn't reveal whether it has a defect or not does not mean that DC current testing is useless. In IC design constant use is made of the fact that although the absolute values of the components are subject to a lot of spread, the relative accuracy of two components is very high. So, the absolute current in one circuit shouldn't be measured, but the current in a number of circuits in one IC should be measured and these currents should be compared [83]-[88]. The ratio of the currents should be the same,

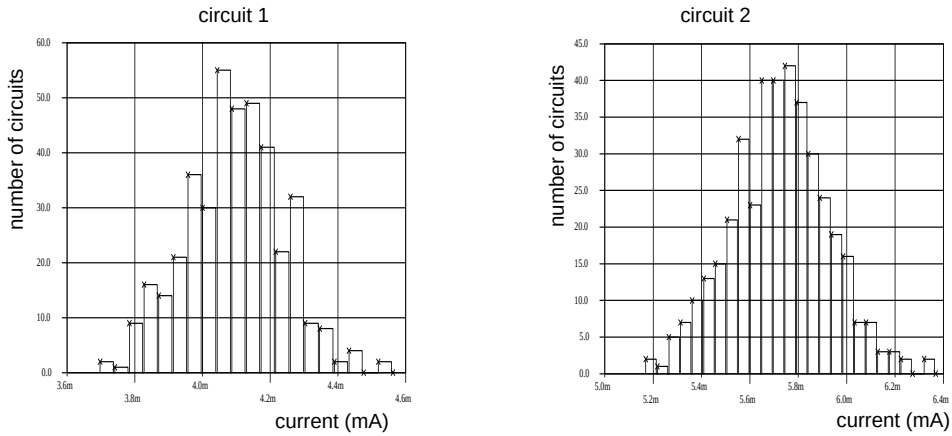


Fig. 102 Simulation of the current distribution due to process spreads for two different circuits.

no matter what the actual process parameters are.

Fig. 103 shows the current distribution of two different circuits in good ICs. Both circuits have a certain distribution range of the current due to process variations. As the currents in the two circuits in one IC are matched, good ICs will have the same relative deviation from the nominal current. That means that if the currents of the two circuits are plotted against each other as in Fig. 103, good ICs are located on the line. In Fig. 103 the currents in the two circuits in three individual circuits are also indicated. The IC indicated by the solid circle is on the line, as the currents in both circuits deviate from the nominal value by the same amount. So this IC passes the test. The IC indicated by the solid triangle has one circuit with a current that falls within the normal distribution (circuit 1) and one circuit with a current that falls outside the normal distribution (circuit 2). So this IC can be detected as a faulty IC by measuring the absolute currents in the circuits. The IC indicated by the solid rectangle has currents flowing in both circuit 1 and circuit 2 that fall within the normal current distribution. So if only absolute currents are considered, this IC will pass as good. But, if the currents in the two circuits are compared (i.e. a relative current measurement) the IC will be rejected, as the currents in the two circuits are not well matched.

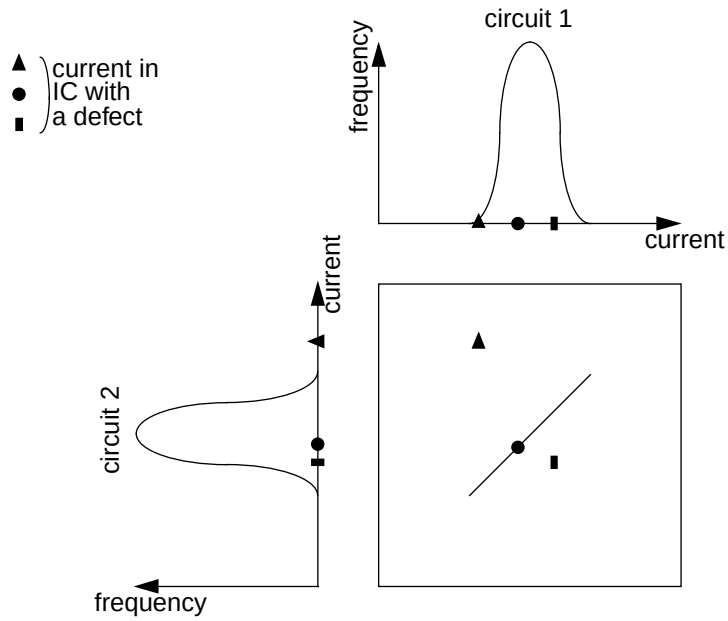


Fig. 103 By comparing the currents of two different circuits in one IC, faulty ICs can be detected even if the current of both circuits is within the normal distribution.

Measuring currents inside an IC

There are several ways in which the current flowing in individual circuits in an IC can be measured. Switching off circuits in the IC by e.g. a switch in the supply rail (Fig. 104a) [89], or by switching off the master bias generator are two possibilities. However, as most circuits in an IC are DC-coupled the abnormal biasing condition, that results from these actions, may lead to unwanted currents flowing in the IC, that may even cause its destruction. In an IC with many components such effects are very hard to predict. Apart from this disadvantage, switches in the supply rail either cause a lot of voltage drop (e.g. emitter followers or common emitter stages driven into saturation) or require very large components (e.g. MOS switches).

An alternative way of measuring the current in individual circuit is shown in Fig. 104b. Each circuit has its own current meter in its supply (or ground) line. This way of measuring the current has the advantage that all circuits can be running with their normal current, and nothing is switched on or off in the IC during the measurement. But, the current meter itself will

cause a voltage drop in the supply lines, just like the switches the circuit of Fig. 104a. This needn't be a problem if the resistance of the aluminium of the supply line itself is used as the current-to-voltage converter and the voltage is measured with a volt meter [83]-[88]. In this way something which is normally considered a parasitic effect is put to practical use.

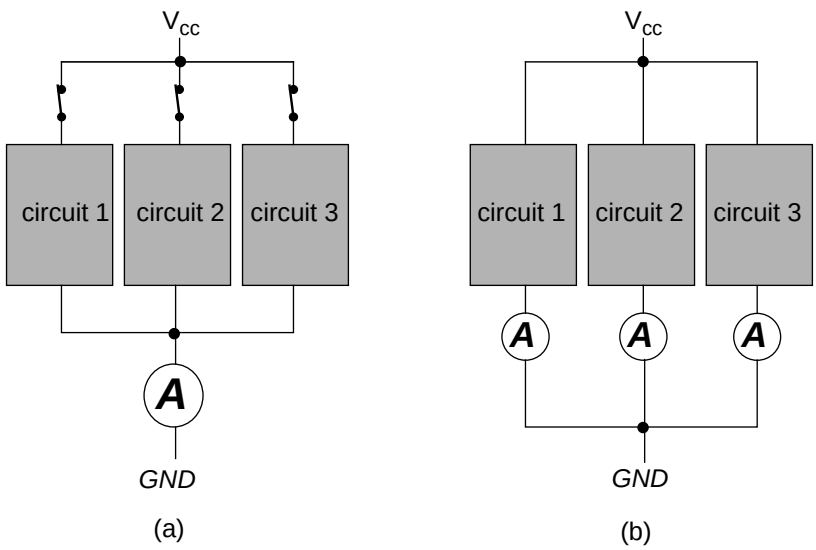


Fig. 104 Two ways to measure current in individual circuits.

amplifying the voltage drop in the supply lines

The voltage drop in the supply lines is usually in the millivolt range. If it were more the supply lines would have too much influence on the performance of the IC. However, measuring a voltage of a few millivolts in a test factory is nigh impossible due to the high levels of electromagnetic interference (EMI) one usually encounters in such factories. For a reliable measurement the signal should be amplified.

Amplifying a few mV can be done simply and accurately with a differential pair of transistors. A differential pair of bipolar transistors gives a 4% change of the collector currents for 1mV input voltage change. However, there is the problem of the offset of the differential pair. That problem can be overcome quite easily by measuring two times, with the inputs of the differential pair interchanged between the measurements. The offset of the differential pair is eliminated by taking the average of the two measurements. The influence of the tail current is

eliminated by taking the ratio of the collector currents instead of their difference. Taking the ratio of the collector currents is in fact calculating the input voltage of the differential pair (i.e. the voltage drop in the supply line), since:

$$V_{IN} = \frac{kT}{q} ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{24}$$

where I_{C1} and I_{C2} are the collector currents of the transistors of the differential pair.

Fig. 105 shows the arrangement of the amplifier that measures the voltage drop in the supply rail. With PNP transistors instead of NPN transistors, the voltage drop in the ground line can be measured.

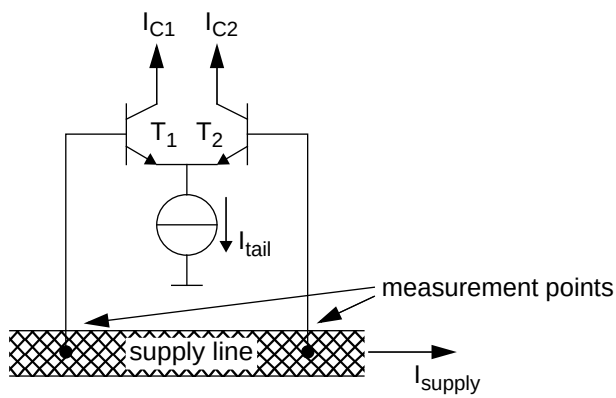


Fig. 105 Differential pair used to measure the voltage drop in the supply line.

If the input voltage of the differential pair is 0V, there is no information in the measurement. On the other hand, if the input voltage of the differential pair is, say, 1V all the current flows in one branch even if the input voltage varies by tens of per cents. This makes it impossible to measure the ratio of the collector currents accurately. So there should be an optimal input voltage to get as high an accuracy in the measurement as possible. Appendix E shows that a voltage drop of 39mV gives the most accurate results. However, for voltages within the range of 10 to 80mV the measurement inaccuracy is still less than two times the inaccuracy for 39mV. This means that the optimal voltage drop across the supply lines is not very critical. This is important for making robust systems that can cope with spreads in the process parameters and temperature. The insensitivity of the measurement error to variations in the voltage drop in the supply lines also allows minor changes in the IC to be made without having to reconnect the I_{CCQ} measurement points.

As described above, the amplifier is needed to get the signal above the level of EMI in the test factory. For each application an optimal amplifier will have to be chosen. In CMOS processes without bipolar transistors a differential amplifier may not be good enough as the gain of a differential pair of MOS transistors is always lower than the transconductance of a differential pair of bipolar transistors at the same bias current. If the voltage drop in the supply lines is very low (e.g. in low power applications) a simple differential pair may not provide enough gain, so more complex amplifiers will be needed.

The I_{CCQ} test method

Fig. 106 shows the general idea of the I_{CCQ} test technique: use several well-chosen measurement points (M_1-M_6) on the supply (or ground) lines to find out what the currents through the various circuits inside the IC are. Each pair of measurement points (such a pair will be called test point in the following) must be placed on a supply line that only feeds the circuit whose current is to be measured by these measurement points. If there is a star-connection of ground and supply lines between the bond pads and circuits (which is often the case in analogue ICs to reduce the risk of crosstalk between circuits) finding suitable measurement points is fairly easy. The distance between the measurement points can be varied to get as near as possible to the optimal value of the voltage drop in the supply line.

After the currents in the circuits in the IC have been measured, they are compared with

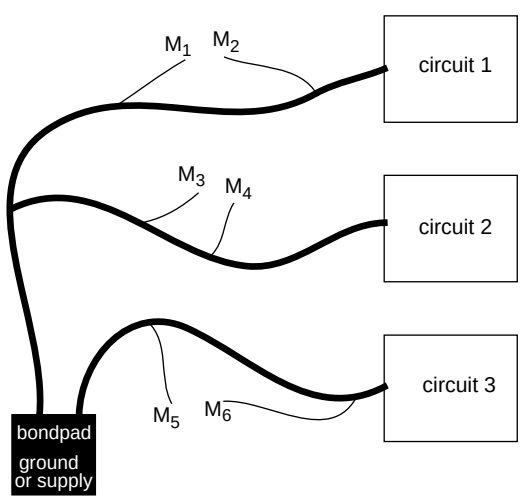


Fig. 106 Basic configuration for I_{CCQ} testing.

each other to decide which ICs are good and which ICs are bad. Basically there are two ways to compare the currents in the circuits. The first way is to take the ratio of the currents of e.g circuit 1 and circuit 2 within one IC. If all ICs are measured under fixed conditions, the ratio of all these currents inside one IC should show a very small spread. This method can be used for both wafer and final testing. The second way is to take the current ratio of e.g. circuit 1 in two adjacent ICs on a wafer.

I_{CCQ} test circuitry

Fig. 107 shows a straightforward way to combine all the measurement points and get the measurement data to the outside world: take N differential pairs and connect all their outputs together. The collector currents of the active differential amplifier can be measured on two test pads. A shift register selects the active pair of measurement points and throws the toggle switch at the input of its differential amplifier.

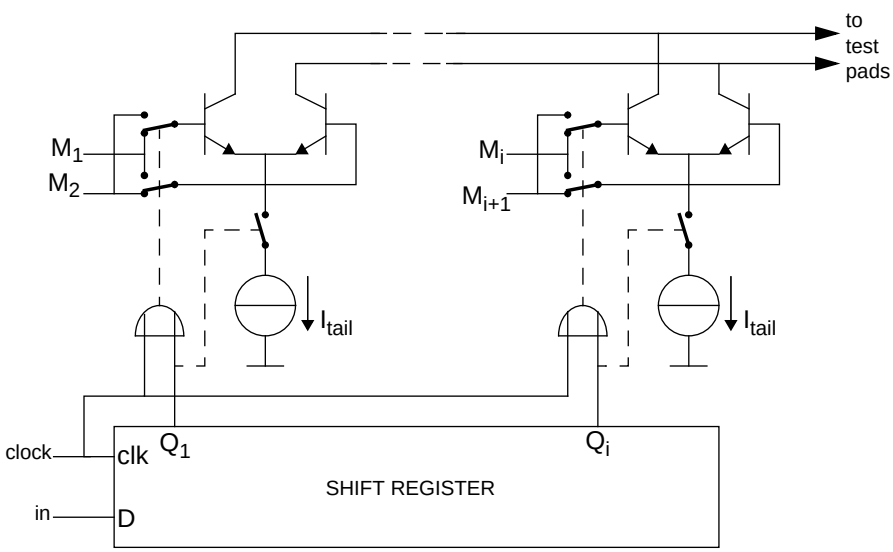


Fig. 107 Straightforward I_{CCQ} set-up.

simplified I_{CCQ} set-up

Fig. 108 shows an alternative solution with fewer components. Here only one differential pair and one toggle switch are used for the whole IC. The switch at the input of the differential

pair is toggled during the time one test point is active. The shift register selects the test point that gets connected to the measurement lines. The shift register and switches are distributed throughout the IC.

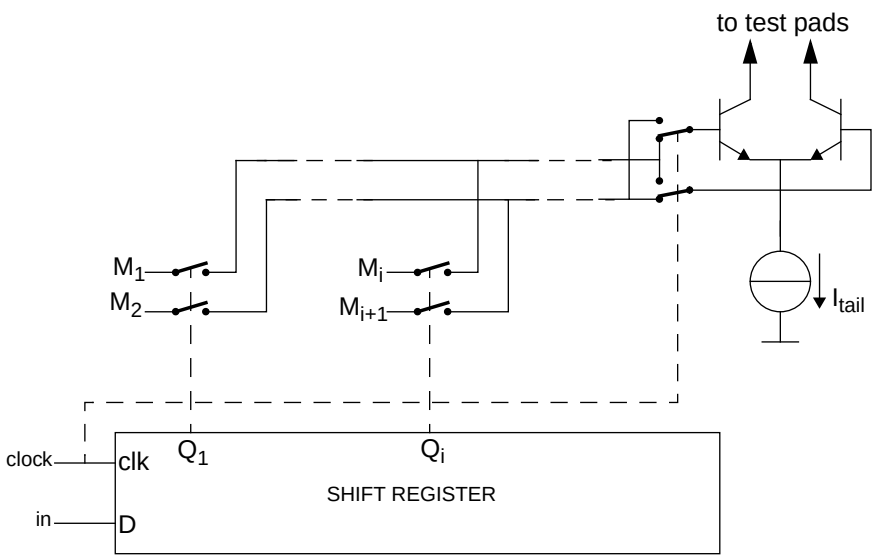


Fig. 108 Simplified I_{CCQ} set-up.

Fig. 109 shows a BiCMOS implementation of the circuit in Fig. 108. This implementation requires only eight MOS transistors per test point and seven wires to connect these stages with one another. The seven wires are: VDD and VSS for supply of the shift sections, $\phi 1$ and $\phi 2$ (non-overlapping clock phases), the wire to connect the output of one section with the input of the next, and the lines going to the differential pair. As the VSS and VDD lines are usually available everywhere in the IC, only five extra wires are required. With these five wires it is possible to distribute a shift register of arbitrary length (i.e. an arbitrary number of test points) throughout the IC. Fig. 110 gives an overview of all the timing signals required for the circuit in Fig. 109.

The circuit of Fig. 109 monitors the ground rail voltage drop. By taking an NPN differential pair and PMOS switches the supply rail can be monitored. When the ground as well as the supply lines are monitored the outputs of both inverters of the shift sections can be used to drive switches.

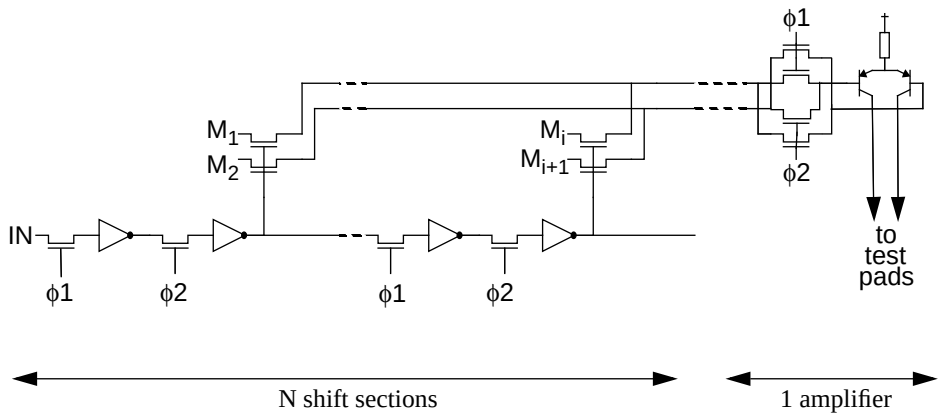


Fig. 109 BiCMOS implementation of the I_{CCQ} test circuit.

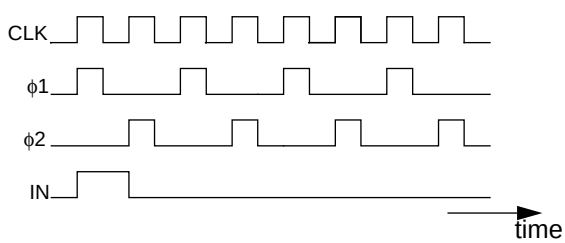


Fig. 110 Timing signals for I_{CCQ} shift register and toggle switch.

Comparison of I_{CCQ} with other techniques

This section compares the I_{CCQ} test method with the test methods mentioned at the beginning of this chapter.

I_{DDQ} testing

The I_{DDQ} technique as used in digital CMOS ICs is not applicable just like that in analogue ICs. Analogue circuits rely on the presence of a bias current for a correct operation. So, if the rejection criterion of faulty ICs is the presence of a current, no analogue IC would pass the test.

built-in current testing

In some digital circuits Built-in Current (BIC) testing is used to check the quiescent ground currents [74]. This technique uses a resistor in the ground rail to convert the ground current to a voltage. In the normal operating mode this resistor is short-circuited. In test mode the voltage across the measuring resistor is compared with some reference voltage. If the quiescent current is greater than the reference the IC is rejected. As BIC testing is a refinement of I_{DDQ} testing, it tries to detect rather small currents. Therefore it is hard to use the resistance of the ground lines as the conversion resistor like in the I_{CCQ} method. Usually in analogue circuits the impedance of the supply rail and especially the ground rail must be very low. Consequently the resistors and switches, as used in BIC testing, are highly undesirable in analogue circuits.

macro-based testing

Macro-based testing [75] is a formalised way to test blocks in an analogue IC by feeding signals to the input of each block and observing their output signals. If all blocks are good, the IC is considered good.

Macro-based testing is a variation of functional testing that still requires a complicated test board, and requires many extra components (switches and buffers) inside the IC. Macro-based testing requires a thorough knowledge of the IC. This is necessary to know which test signals should be used and where the switches and buffers should be positioned to give a maximum test coverage of the IC.

analogue scan testing

In [76] an analogue scan test technique is proposed. In this technique the outputs of analogue circuits inside the IC are sampled. These samples are subsequently shifted to a test pad through an analogue shift register. This does, of course, put a very high demand on the transfer efficiency of the analogue shift register in order to make sure that the signal does not degrade. The I_{CCQ} technique discussed in this paper has the advantage that the shift register is digital, so signal degradation is no issue. It also does not require changes to the circuits to be tested. For the analogue scan method on the other hand a sample-and-hold circuit has to be added to each node that has to be monitored. The advantage of the analogue scan method is that it is a test that can also detect parametric faults. The I_{CCQ} method is intended as a quick sieve to reject faulty circuits, but does not guarantee full functionality.

Analogue scan testing is in fact a variation of functional testing. Like macro-based testing

it requires both thorough knowledge of the IC and complicated test hardware.

oscillation-based testing

Oscillation-based testing is a test technique that during testing connects the analogue circuits in an oscillator structure. The oscillation frequency indicates whether the circuit is good or not. For this test method additional circuitry is needed to turn the analogue blocks into oscillators. Furthermore, a thorough knowledge of the circuit properties is required to make sure that structure into which the circuit under test is connected is really an oscillator. Also the dependence of the oscillation frequency on processing parameters must be taken into account. This makes this method rather time-consuming to implement.

current test techniques

Comparing the I_{CCQ} test method with current measuring test techniques seems superfluous, as I_{CCQ} testing *is* a current measuring technique. But, I_{CCQ} is the first formalised test technique based on current measurement that not only measures the current, but also uses the matching properties of circuits in an IC to find faulty ICs. The matching properties are used by measuring the relative instead of the absolute current in the circuits. As I_{CCQ} uses the matching properties of circuits in ICs to decide between good and bad ICs, no thorough knowledge of the IC is needed.

To sum it all up we can say that the main advantage of the I_{CCQ} test technique is that it is parallel to the supply lines. This implies that it does not influence the operation of the IC in any way. It is non-invasive to the circuits; it does not require any changes to the circuit whose current is measured, it does not add extra voltage drop on the supply rails, and it can measure the current of one circuit while the whole IC is working.

I_{CCQ} in a mass production IC

The I_{CCQ} test method was verified in a one-chip TV processor IC [90]. Fig. 111 shows a photograph of the IC. A description of one of this IC's predecessors can be found in [91]. This test vehicle is a mixed-signal BiCMOS IC in which the TV signal is processed by analogue circuits, whereas the control part is digital. I_{CCQ} was introduced in a production IC instead of in a test IC, because this makes it easy to generate enough data for (statistical) analyses. In these analyses the test coverage of I_{CCQ} can be compared with the existing (functional) production test program.

The IC contains nearly 50,000 components. About 30 per cent of these components are in

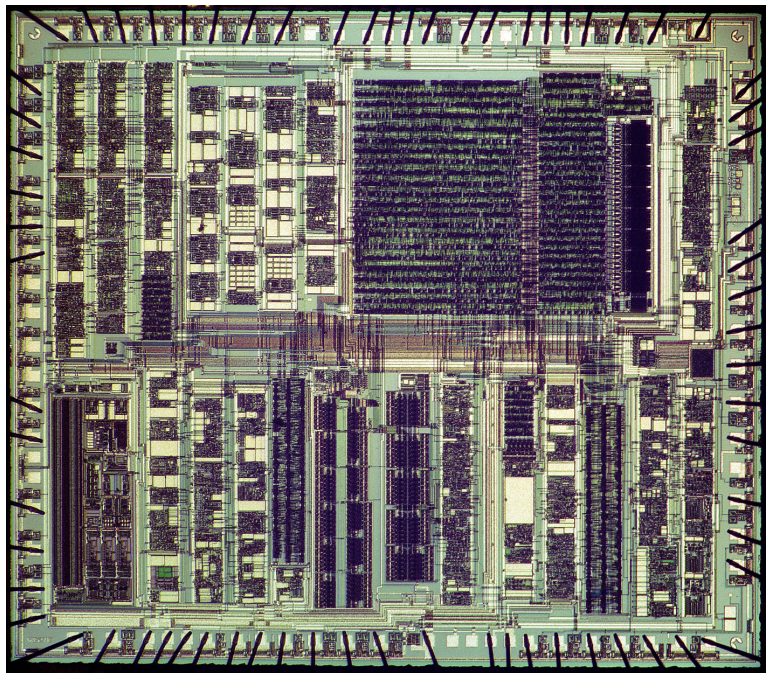


Fig. 111 Chip photograph of the one-chip TV processor IC with I_{CCQ} capability.

the analogue part. The whole IC draws a current of 120mA from an 8V supply. The analogue part consumes 110mA. The analogue part is divided into 150 basic functional cells. To these cells 24 I_{CCQ} test points were added. So on average each I_{CCQ} test point monitors six basic functional cells with an average current consumption of 4.6mA. The I_{CCQ} test points guard 580 components on average. Each I_{CCQ} test point has eight components. The read-out amplifier and clock generator comprise 61 components. So all in all there is an overhead of 253 components in the IC. This means that the overhead for I_{CCQ} testing in this IC is 1.8%.

Let's compare that with the overhead of the scantest that is used in the digital part. The digital part contains 475 flip-flops. Each flip-flop has a four-transistor-multiplexer at its input for the scanpath. This means that the total digital part has 1900 components for the scantest on a total of 33000 components for the digital functions. This is a 5.8% overhead.

The I_{CCQ} circuitry was shoehorned into the IC of Fig. 111 in just a few days, after its I_{CCQ}-less layout had been finished, without having to increase the IC dimensions. The test points were positioned such, that each test point monitors approximately equal areas of silicon and at the same time approximately equal amounts of current. This may not be the most optimal way of testing, but a better criterion was not available at the time the layout was made. If

there are more optimal ways of placing the test points, it must be possible to find these by analysing the measurement data.

The IC has two analogue supply pins and one analogue ground pin. The analogue supply pins serve a total of seven bond pads, the analogue ground pin connects to four bond pads. This splitting up of the ground and supply to several bond pads also allows the measurement of smaller currents than the total IC current at wafer testing. So one of the questions that has to be answered is whether I_{CCQ} testing gives a better fault coverage than simply measuring the currents flowing through the multiplicity of bond pads.

Experimental results of the I_{CCQ} test circuitry

To test the operation of the I_{CCQ} test circuitry, the set-up shown in Fig. 112 was used. The collector currents of the sense amplifier of the I_{CCQ} circuitry are fed to two current-to-voltage converters. The output voltages of the current-to-voltage converters are subtracted and fed to an oscilloscope.

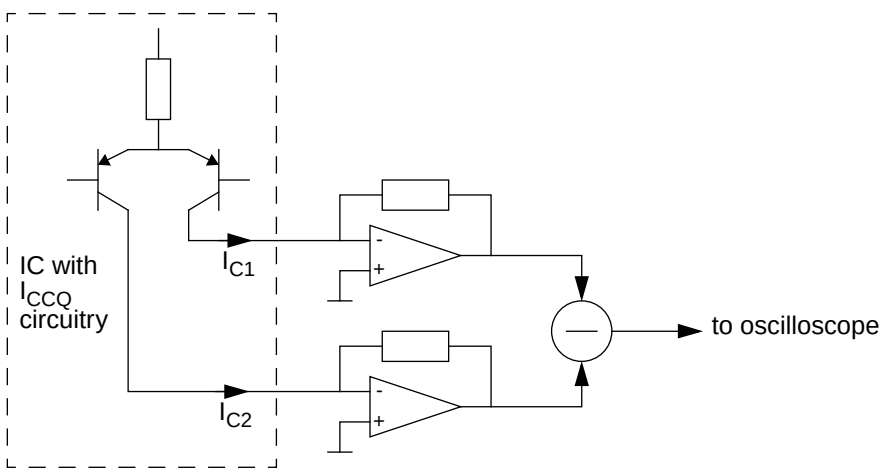


Fig. 112 Test set-up to test the correct operation of the I_{CCQ} circuitry.

Fig. 113 is an oscillogram of the output voltage of the subtractor. From left to right all 24 I_{CCQ} test point in the IC are scanned. Each test point generates a positive and a negative voltage excursion, as each test point is measured twice with the inputs of the amplifier interchanged. At first glance the figure looks symmetric around the X-axis. But, because the positive and negative excursions are time-shifted, it is not really symmetric. No attempt was made to have the same “phase” for all test points. So some test points have their positive excur-

sion first, while others have their negative excursion first. This oscillogram will be different for different IC types. Hence it can be regarded as the IC's I_{CCQ} signature.

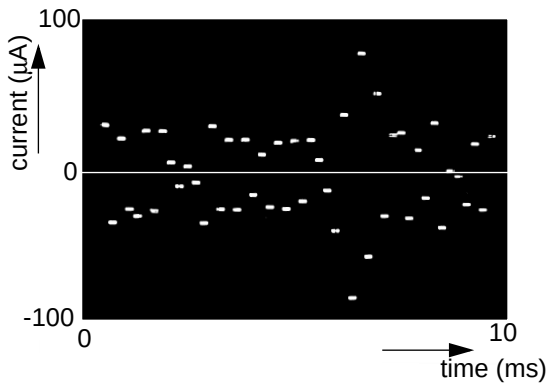


Fig. 113 I_{CCQ} signature of the one-chip TV processor of Fig. 111.

Fig. 114 compares the signatures of three ICs: one defect-free (Fig. 114a) and two with a defect (Fig. 114b and c). For clarity only the upper half of the signature with respect to Fig. 113 is shown. The fifth measurement point of one faulty device (Fig. 114b) shows a much larger current than the fifth measurement point of the good device (see arrows). The fifth measurements point of the other faulty (Fig. 114c) device shows a much smaller current than the good device. On the oscilloscope only fairly large deviations of the current can be discerned. With an accurate current meter current deviations below one per cent are easily detectable.

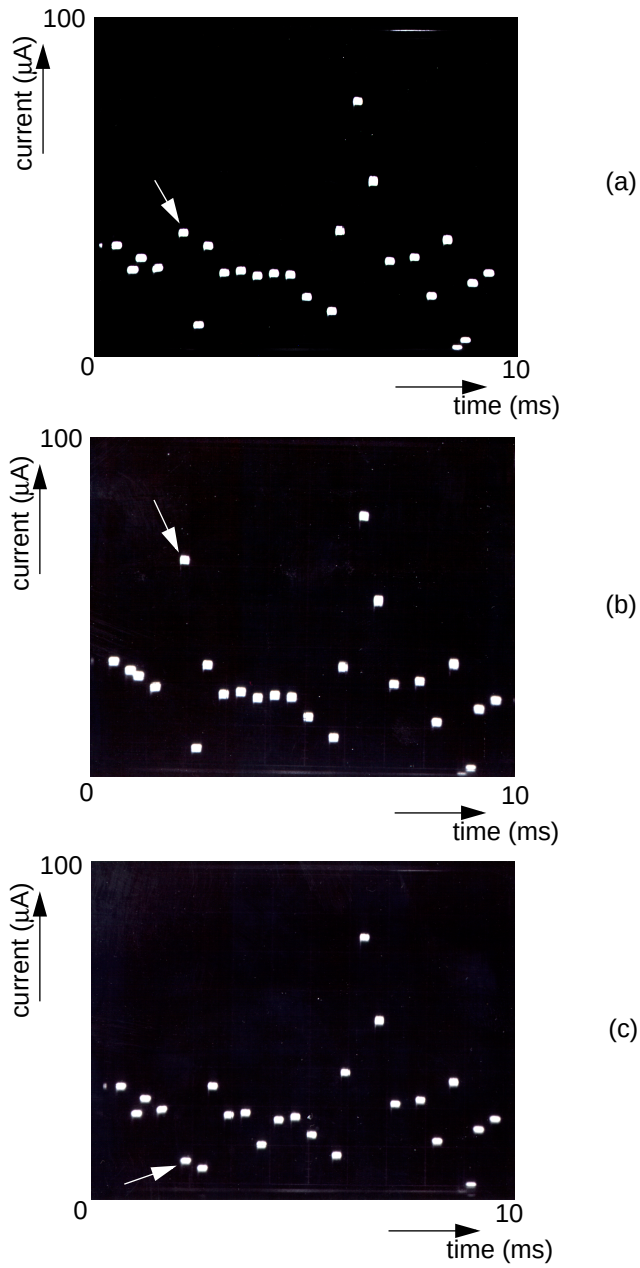


Fig. 114 Upper half of the I_{CCQ} signature of a good IC (a) and two faulty ICs (b and c).

The signatures shown above measure the DC current in the various circuit inside an IC. However, I_{CCQ} can also be used for AC measurements.

Fig. 115 shows the I_{CCQ} signature of an IC with AC currents on top of the DC current. Extra information can be gathered by looking at e.g. the peak-to-peak amplitude, or the frequency of the AC component.

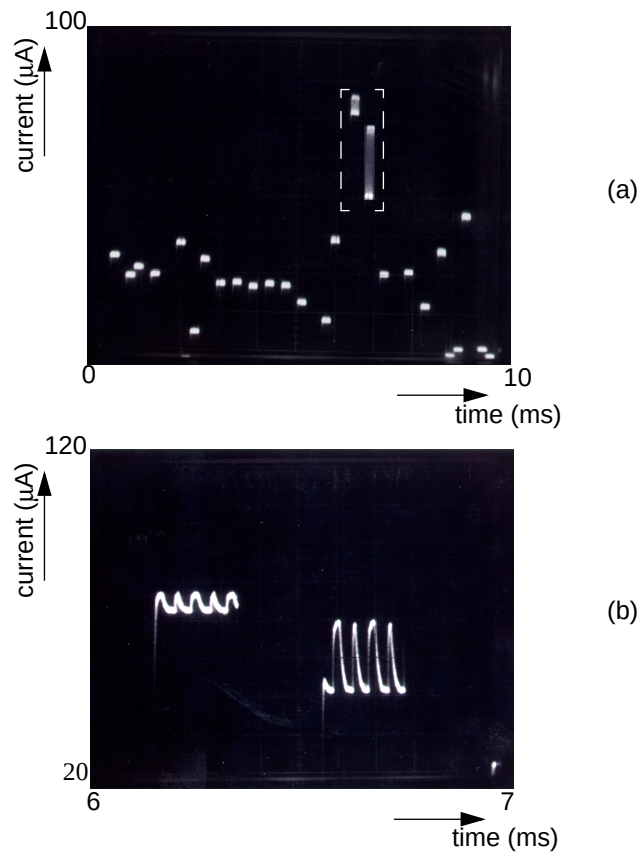


Fig. 115 (a) I_{CCQ} signature with AC component. (b) Detail.

Although in the following only the DC current will be used as a rejection criterion, Fig. 115 shows that I_{CCQ} need not be limited to DC testing.

Experimental results of the I_{CCQ} test technique

The oscillograms shown above were taken by converting the current of both collectors of

the I_{CCQ} output amplifier into a voltage and subsequently taking the difference of these with an oscilloscope (Fig. 112). The measurements that are described in the following were all made by using the *ratio* of the collector currents. This allows an accurate calculation of the voltage drop in the supply/ground lines (see equation (24).

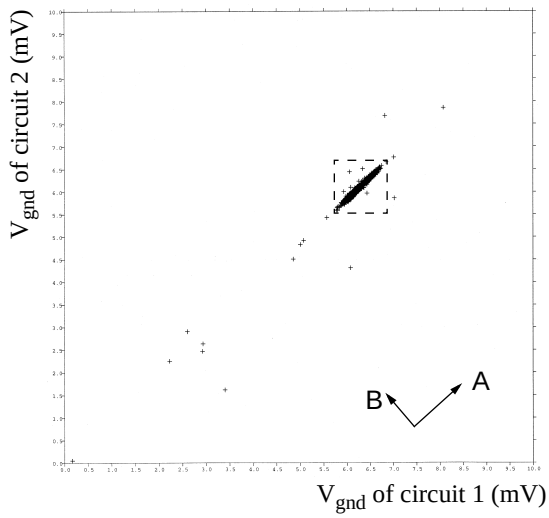


Fig. 116 Comparison of the ground rail voltage drop measured by two I_{CCQ} test points in one IC.

The plot of Fig. 116 compares the voltage drop in the ground lines as measured by two I_{CCQ} test points in one IC. The two I_{CCQ} test points that are compared are in the same IC, and each cross in Fig. 116 represents the result of one IC. The total number of tested ICs is 250. If all ICs were perfectly equal, the plot would have all crosses right on top of each other. Due to process variations and mismatch, however, the distribution is not a point but ellipse-shaped. The elongation of the ellipse in the direction of arrow A is caused by the process variations. The width of the ellipse in the direction of arrow B is caused by mismatch between the circuits. The crosses around the ellipse are rejected ICs. An important thing to notice is that besides all the ICs outside the dashed box, there are also ICs inside the dashed box that are rejected. The voltage drop in the ground lines for these ICs is within the normal distribution for both test points. Therefore these ICs can only be rejected by comparing two test points (see also Fig. 103).

Determination of test limits

Setting the pass/fail limits of I_{CCQ} testing is not a straightforward procedure. First, the I_{CCQ} measurements are not part of the device specification with corresponding unambiguous limits. And secondly, there is no underlying fault model which unambiguously predicts the deviation of I_{CCQ} measurements between good and faulty products. Hence limits need to be established empirically.

With the I_{CCQ} test method ICs in which the distribution of the currents, that flow in the various circuits inside the IC, deviates from the normal distribution should be rejected. The (empirical) procedure to determine the pass/fail limits is as follows:

1) Test at least one wafer, but preferably a number of wafers from different batches, with the functional test program and measure all the I_{CCQ} test points in all ICs.

2) Store all functional test program and I_{CCQ} measurement data in a database. For ease of use the ratio of the collector currents measured in the I_{CCQ} measurement is calculated back to the voltage drop in the supply line (equation (24)) that each test point monitors.

3) Select the data of the devices that passed the functional test program.

4) Determine the correlation factor between the data of all pairs of I_{CCQ} test points.

5) Select the pairs of I_{CCQ} test points with the highest correlation, making sure that each I_{CCQ} test point is present in the selected set.

6) For each selected pair of I_{CCQ} test points calculate the average value of the ratio of their measurement data. Each I_{CCQ} test point generates a number that is equivalent to the voltage drop in the ground rail. In this calculation the ratio of the voltage drops measured by the selected set of I_{CCQ} test points is determined for each IC. If the voltage drop measured by I_{CCQ} test point m is designated V_m, and if I_{CCQ} test points m and n are in the selected set of test points, the ratio V_m/V_n is calculated for each IC individually. After that the average value of V_m/V_n is calculated for all the ICs in the database.

7) Return to the full database that includes the rejected devices.

8) Empirically determine the maximum allowable deviation from the average value for each selected pair of I_{CCQ} test points that on the one hand rejects as many devices that failed on the functional test program as possible, and on the

other hand rejects as few devices as possible that passed the functional test program. The maximum allowable deviation can be different for all pairs of test points. For one pair of test points a maximum deviation of, say, 3% may be optimal, while for another pair a deviation of 2% may be optimal.

With the test limits that have been determined with the procedure above, new wafers can be tested. Each IC in which the V_m/V_n ratio of one (or more) test point pairs deviates more than the empirically found maximum allowable deviation, is rejected.

Interpretation of test results

ICs that are rejected by the test program can be divided into three sub-populations: I_{CCQ} rejects, I_P rejects (test of the total power supply current) and FTP rejects (functional test program). The functional test program includes the structural tests for the digital part of the IC (scan test and I_{DDQ}). Fig. 117 shows a Venn diagram of the total population of wafer test rejects.

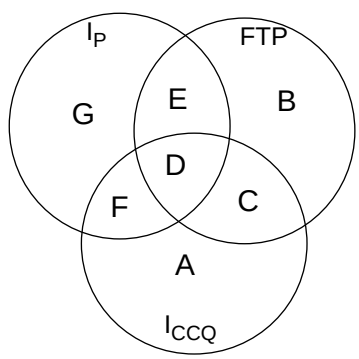


Fig. 117 Venn diagram of rejected ICs.

I_{CCQ} testing can be considered effective if there is a large overlap in detection of faulty products between I_{CCQ} tests and the functional tests (areas C and D). If this overlap is maximised, ideally to 100%, the corresponding analogue tests are redundant and can be removed from the functional test program. And even if this is not the case, examining the parts which fail on both the FTP and the I_{CCQ} test may reveal a subset of tests which are redundant and can thus be removed from the functional test program.

Another interesting quantity at wafer test is the ratio of number of rejects detected with I_{CCQ} tests to that detected with the conventional I_p (power supply current) test (area D and F).

As I_{CCQ} testing can be considered refinement of I_P testing the areas E and G should be empty, whereas areas A and C should contain far more rejects than areas D and F.

An IC should only be rejected if it is functionally bad. Therefore area A should be (nearly) zero. However, there are reasons why I_{CCQ} testing can be effective, even if area A is not zero. These will be discussed later.

In the following the term hit-rate will be used to indicate the effectiveness of the I_{CCQ} test. The hit-rate is defined as the ratio of number of defective circuits found by I_{CCQ} divided by the total number of defective circuits. Ideally the hit-rate should be equal to one.

I_{CCQ} effectiveness at wafer testing

Two experiments were performed to see how effective the I_{CCQ} test method is in finding faulty ICs during wafer testing.

first experiment

For the first experiment, the test limits were determined on 250 samples with the procedure described above. With these test limits a batch of wafers was tested. Fig. 118 shows the distribution of 1000 rejects of the wafer test program of this batch. The diagram shows that the functional test program (FTP) rejects 99.3% of all the rejected ICs. The I_{CCQ} test detects 42.7% of the faulty ICs.

The power supply current test (I_P) detects 10.5% of the faulty circuits. So, all in all, I_{CCQ} detects four times more failing ICs than power supply current testing.

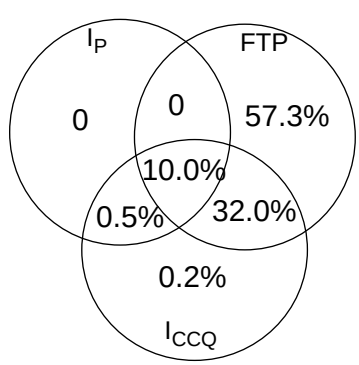


Fig. 118 Venn diagram of 1000 rejected ICs (first experiment).

second experiment

The results of Fig. 118 were obtained by comparing the best correlated I_{CCQ} test points in one IC. However, as more batches were tested, it soon became clear that unless the test limits are set rather wide for some batches the numbers if I_{CCQ}-only rejects (area A of Fig. 117) becomes unacceptably high. The reason for that is that the bias generation of the various circuits in the IC is not identical, so the matching properties of these circuits are not optimal. Therefore a switch was made to comparing the currents through identical circuit in adjacent ICs on the wafer. Making this switch implies that setting the test limits becomes somewhat easier, as it is no longer necessary to find the best matching test points. This means that steps 4 and 5 of the procedure to find the test limits are no longer necessary.

The results presented above were obtained by taking the current ratios of the I_{CCQ} test points for a nominal bias setting. A refinement of the test method introduced in the second experiment was to set the supply voltage of the IC to the maximum that the IC can withstand (9V), while at the same time overruling the (internally generated) reference voltage of 4V by an external source of 5V. This way defects in the ICs have a maximum stress, so the chance of finding faulty ICs is increased. Fig. 119 shows the distribution of 23,600 analogue rejects gathered from five batches.

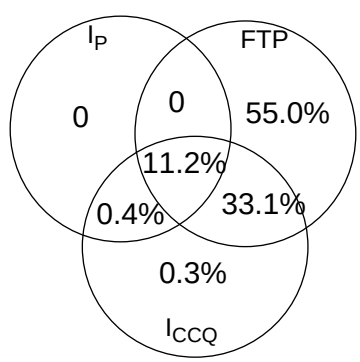


Fig. 119 Venn diagram of 23,600 rejected ICs of five batches (second experiment).

As can be seen in Fig. 119 the total amount of faulty ICs found by I_{CCQ} is increased by a few per cent (from 42.7% to 45%) by the changes made to the original test approach.

From the above results it is clear that the hit-rate is not equal to one. This does not mean, however, that I_{CCQ} testing has no significance. If the I_{CCQ} test is performed at the start of the

test program and the test program is aborted immediately upon detection of a failure, the average test time can be considerably reduced.

Analysis of I_{CCQ} test data of ten batches

The test method as used in the second experiment described above was used to test ten batches of the one-chip TV processor IC. Below an analysis of the test results is given.

1) Correlation between I_{CCQ} and I_p
   Nearly all devices which fail the conventional I_p test also fail the I_{CCQ} test. This is to be expected since I_{CCQ} can be considered a refinement of the I_p test. A ratio of 2.7 was found between the number of I_{CCQ} rejects and the number of I_p rejects. Seeing that there are 24 I_{CCQ} test points and the seven I_p test points (ratio 3.1), the increase in hit-rate is almost linear with the number of test points.

2) Correlation of I_{CCQ} and individual tests of the final test program
   When analysing the reject data of the first batch (1000 rejected samples) a number of tests of the functional test program appeared to have 100% correlation with I_{CCQ} testing [84]. However, this could not be repeated with this experiment. The higher the number of rejected samples, the lower the number of tests that have a 100% correlation with I_{CCQ}.

3) I_{CCQ} hit-rate versus wafer yield
   There is a high degree of correlation between the wafer yield and the I_{CCQ} hit-rate. If the yield of a particular wafer decreases, the I_{CCQ} hit-rate increases. In this experiment the correlation coefficient was -0.97. This means that if the average yield of a batch is 90% and the I_{CCQ} hit-rate is 45%, a wafer with a yield of 81% (i.e. 10% lower than the average 90% yield) will have an I_{CCQ} hit-rate of 49.4% (i.e. 9.7% higher than the average 45% hit-rate).

4) Local I_{CCQ} hit-rate
   The global I_{CCQ} hit-rate can be defined as the combined areas C and D with respect to the total area of fig. Fig. 117. In the first two experiments the global hit-rates were 42% and 44.3%, respectively (Fig. 118 and Fig. 119). The design of the one-chip TV processor IC combines six subsystems (or macros) to form the complete IC. For the purpose of optimising the placement of I_{CCQ} cells it is interesting to investigate the hit-rate per macro. For four of the ten batches it was examined what the hit-rate of the I_{CCQ} test points of a macro was. In this experiment the local I_{CCQ} hit-rate is defined as the ratio of rejects found

through I_{CCQ} test points of a macro divided by rejects found by the macro-specific tests for that macro of the functional test program. This was subsequently compared with the number of I_{CCQ} cells for that macro. The result of this was that there is a trend that more cells lead to a higher local I_{CCQ} hit-rate. This is in line with the observation in item 1) above: the more I_{CCQ} test points, the higher the hit-rate.

5) Simplified wafer test scenario

A high I_{CCQ} hit-rate is interesting from the point of view of test cost reduction. For an analogue IC of this complexity a long average test time is commonplace. This is primarily due to the analogue tests performed on good parts. Thus a significant saving in test time can be achieved when a number (or all) of the analogue tests are removed. An analysis was made on five of the ten batches of the global I_{CCQ} effectiveness, when performing only I_{CCQ} and the digital tests of the functional test program. In other words, the test program was reduced to scan testing, I_{DDQ} testing and I_{CCQ} testing. The percentage of faulty devices which are not detected with this stripped test program relative to the total number tested turned out to be 2.9%. In other words, wafer test yield will increase by this amount and final test yield will reduce by the same amount. Whether the reduction of the test costs that I_{CCQ} brings (thanks to the reduced test time and hardware) outweighs the extra costs that are made due to the scrapping of mounted devices, depends on the cost structure of the wafer and assembly fabs.

6) I_{CCQ}-only rejects

The number of rejected ICs which fail only in the I_{CCQ} test ranged from less than 0.1% to 2.2% per batch. These can be classified in four categories:

1) products which fail the final test program
2) products which fail life-tests
3) defective I_{CCQ} test circuit
4) yield loss (i.e. good ICs that are rejected)

The fourth category should be empty, as every needlessly rejected IC limits the potential financial profit that can be made on the IC.

The third category should be treated like a faulty IC. The fact that there is a defect in the IC, even though it is seen only in the I_{CCQ} test components, means that it is suspect and therefore it should be rejected.

The first two categories, however, are benefits of the I_{CCQ} methodology. The first category will save on packaging cost, while the second will improve the quality, as fewer ICs will break down after operating for just a short time. The

first two categories will be discussed in the next sections.

I_{CCQ} effectiveness at final testing

Wafer test programs usually cover less functionality of an IC than final test programs. This is due to the fact that during wafer testing long probes connect the IC to the test equipment. This makes e.g. high-frequency or small-signal operation very difficult. The final test interface is more like a real-life application, so that all of its functionality can be checked.

To examine the ability of I_{CCQ} testing to find faulty ICs, that will pass the wafer test program but fail the final test program, 152 I_{CCQ}-only rejects were packaged and put through the final test program. Of these 152 ICs 54 were rejected by the final test program. From this it can be concluded that I_{CCQ} detects 36% of the faulty ICs that pass the wafer test program. So the yield loss due to I_{CCQ} testing is not equal to the 0.3% I_{CCQ}-only rejects (Fig. 119), but 0.2%. The yield loss can be considered even lower if I_{CCQ}-only rejects appear to have reliability problems.

I_{CCQ} as a reliability test

One of the reasons why an IC may fail on I_{CCQ}, but pass the final test program might be that there is a weak spot in the IC. Such a weak spot may not impair the normal operation of the device, so that it passes the final test program. But this weak spot may severely limit the life-time of the IC. To check this hypothesis, 32 samples from the 98 that were not rejected by the final test program, in the experiment described above, were put on a life-test. As a reference group 32 samples from the normal production flow were taken. After 168 hours of high temperature stress testing both groups had one failing device. So it must be concluded that I_{CCQ}-only rejects are not especially suspect for early-life failure.

I_{CCQ} and boundary scan testing

During final testing one of the problems encountered in an IC with several bond pads connected to one ground or supply pin is how to ascertain whether all bond wires are present. I_{CCQ} detected all ICs in which one such bond wire was (deliberately) removed. This also means that I_{CCQ}-like circuitry can be used in boundary scan testing of a printed circuit board. Here the problem is to find ground and supply pins that are not correctly soldered to the board. As all ground and supply pins are usually all connected to a power grid inside the IC, this is not as easy as it seems. If one or more solder joints are failing, the IC will probably still work. But, as the current is flowing through fewer pins things like substrate bounce may lead to problems, or electromigration may occur after the IC has been running for a while. As I_{CCQ} can

find broken bonding wires it should also be able to detect failing solder joints.

Future research

Although the first results of I_{CCQ} look very promising, the hit-rate (i.e. the ratio of faulty ICs detected by I_{CCQ} and the functional test program) is not (yet?) high enough to replace functional testing by I_{CCQ} testing.

One way to improve the hit-rate is to define a good strategy for selecting the measurement points. In the IC described above an attempt was made to monitor approximately equal amounts of both silicon area and current for all test points. Comparing the characteristics of the circuits that are monitored by a test point with the hit-rate of that test point should give some clues as to how to improve the test point selection strategy.

Conclusions

In this chapter a test technique for analogue VLSI circuits was presented that uses the current distribution in an IC to separate good and bad ICs. The currents are measured by measuring the voltage drop that the supply currents cause in the supply rails. Normally the voltage drop in the supply lines is considered an undesirable effect, but as aluminium supply lines aren't superconductors, there will always be some voltage drop across them, if supply current is flowing. So an effect that is normally considered parasitic is put to good use.

The I_{CCQ} test method uses the matching properties of integrated circuits to determine whether an IC is good or bad, so even bad ICs whose supply currents fall within the normal distribution can be detected.

The I_{CCQ} test technique offers opportunities for substantial saving of the test time of large analogue and mixed-signal ICs. For the IC described above the I_{CCQ} test time is only 40ms, as opposed to a functional test time of 5s.

The I_{CCQ} test method is non-invasive to the circuit in the IC: it can be added to an IC without the need for any changes to the circuits that are monitored. As the I_{CCQ} monitors are in parallel to the supply lines they neither load nor influence the circuits in any way. This also has an advantage when persuading analogue IC designers to use this test method. No analogue designer likes to adapt his circuit for test options once she/he has the design functionally up to spec.

appendix A

Simple noise analysis on the circuit of Fig. 29

The circuit of Fig. 29 (without the capacitor) can be regarded as an active load resistor of a transconductor. In this appendix a simple noise analysis will be done on the circuit of Fig. 29 to get some feeling for its signal-to-noise ratio with respect to that of a passive load resistor.

Inspecting the circuit of Fig. 29, it can be concluded immediately that the components in the shaded area are not contributing to the differential output noise voltage. This is due to the fact that they are in the common-mode path. Only T_3 will have a small contribution to the differential output noise voltage, as its noise is not exactly 100% correlated to its counterpart in the other half of the circuit. However, its contribution to the differential output noise voltage is negligible compared to the contribution of T_2. So, for a simple noise analysis only the contribution of T_1 and T_2 has to be considered.

Fig. 120 shows the resulting circuit on which the noise calculation is performed.

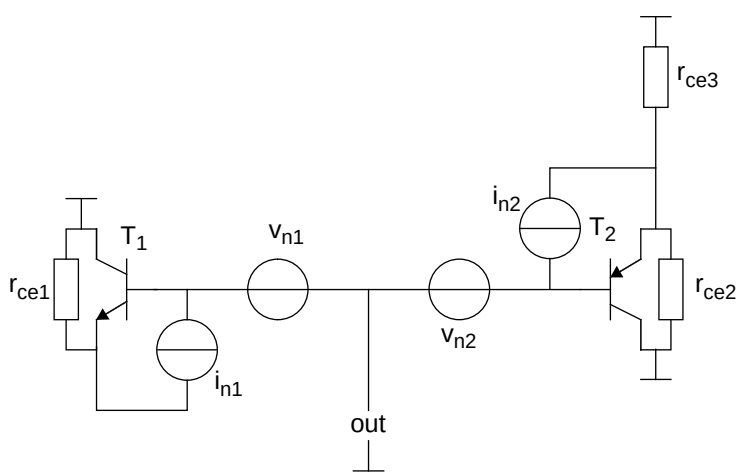


Fig. 120 Equivalent circuit diagram for simple noise analysis.

As this is a simple noise calculation, the 1/f noise and base resistance are neglected in the following calculation. With these assumptions, the power spectral density (PSD) of the noise current sources is $S(i_n) = 2qI_B$ and the PSD of the noise voltage sources is: $S(v_n) = 2kTr_e$ [37].

The output noise voltage generated by T_1 in a signal bandwidth B is (note that the output noise voltage is calculated on the base node of T_1):

$$\overline{v_{n,\,out,\,T1}^2} = 4kTB\left(\frac{\alpha_{e1}r_{ce1}^2}{r_{e1}} + \alpha_{e1}r_{e1} + \frac{r_{e1}}{2}\right) \tag{25}$$

As the term with r_{ce1} is a factor of qV_{EA}/kT greater than the term with $\alpha_{e1}r_{e1}$, the terms with r_{e1} will be neglected. Only the influence of the noise current source and the collector-emitter resistance will be calculated in the rest of this analysis. In Fig. 120 it can be seen that the total output noise voltage is generated by the parallel connection of T_1 and T_2. So,

$$\overline{v_{n,\,out}^2} = ((\alpha_{e1}r_{ce1}) \parallel (\alpha_{e2}(r_{ce2} \parallel r_{ce3})))^2\left(\overline{i_{n1}^2} + \overline{i_{n2}^2}\right) \tag{26}$$

From equation 8 it follows that the resistive term in this expression is identical to the half the resistance of the prototype circuit (the calculation so far is for only one half of the differential circuit).

$$((\alpha_{e1}r_{ce1}) \parallel (\alpha_{e2}(r_{ce2} \parallel r_{ce3}))) = \frac{R}{2} \tag{27}$$

As the DC base bias current of T_2 is delivered by T_1, their input noise current sources are identical. This, combined with the simplification of equation 27, yields the output noise voltage of the complete differential circuit, after multiplying by a factor of two.

$$\overline{v_{n,\,tot}^2} = 2\left(\frac{R}{2}\right)^2\left(2\overline{i_{n1}^2}\right) \tag{28}$$

Equation 28 can be rewritten as:

$$\overline{v_{n,\,tot}^2} = 2kTB\frac{R^2}{\alpha_{e1}r_{e1}} \tag{29}$$

The noise voltage of a passive resistance with value R is:

$$\overline{v_{n,\,R}^2} = 4kTBR \tag{30}$$

Combining equations 29 and 30 yields:

$$\frac{\overline{v_{n,\,tot}^2}}{\overline{v_{n,\,R}^2}} = \frac{R}{2\alpha_{e1}r_{e1}} \tag{31}$$

The degradation of the total output noise voltage is equal to the square root of equation 31. With the process data of Table 3 the degradation factor equals 25 (28dB). The degradation factor is independent of the bias current, as both the resistance R of the passive network and the bias current of the transistor circuit (and hence r_e) have a linear relationship with the time-constant. A simulation (without 1/f effect) of the circuit of Fig. 29 showed a degradation of the output noise voltage of a factor of 28 (29dB).

appendix B

Mixed-signal quadrature demodulator with a multi-carrier regeneration system

The following pages of this appendix are a reprint of [62]. It describes an alternative to the quadrature demodulator of the chapter 4, with a lower specification. In making the system described in [62] it was assumed that the spectrum of the (co)sine outputs of the quadrature generator was white noise, and that this noise should be 50dB below the carrier. For standard video signals this is an adequate assumption. For more critical signals, however, this is not good enough. The spectrum of the (co)sine looks like white noise to a large extent, but there are a number of discrete frequencies which are dominant. These discrete frequencies can give rise to faintly visible line structures on the TV screen. Therefore the design of chapter 4 was made aiming for a suppression of the dominant frequencies in the (co)sine spectrum of more than 55dB [63]. This led to the use of 8-bit DACs, instead of 6-bit DACs.

Apart from the spec, the construction of the demodulator itself was changed. The main differences between the two demodulators are around the DACs. In the design of [62] multiplying DACs were used. However, these have the disadvantage that not only the contents of the analogue input signal around the clock frequency, but also around the multiples of the clock frequency, are demodulated to the baseband. This may give a strong deterioration of the output signal when this circuit is added to a larger system. Crosstalk from the rest of the system to the input of the demodulator will result in a poor signal-to-noise-plus-spurious ratio. On top of this, the use of 8-bit (instead of 6-bit) multiplying DACs in the design of [62] would lead to an unacceptable increase of the circuit area.

The tracking/acquisition range was increased from 500Hz (used in the design of [62]) to 700Hz in the design of chapter 4, to guarantee that even if the 24MHz clock frequency is a few hundred Hertz off target, the colour decoder can always lock to the incoming burst.

These changes of insight led to significant differences between the demodulators of [62] and chapter 4.

Brief Papers

Mixed-Signal Quadrature Demodulator with a Multicarrier Regeneration System

Joop P. M van Lammeren and Roy W. B. Wissing

***Abstract*—This paper presents a combined analog/digital demodulation system built around a (PLL) with digital carrier regeneration. The input signal itself is not digitized, but the PLL is digital wherever it is possible. The link between the analog and the digital domain is a 1-bit sigma–delta converter that converts the (quasi-dc) output signal of the PLL's phase detector into a bitstream. The PLL's loop filter doubles as a decimation filter for the bitstream. The analog I and Q output signals are obtained by multiplying the analog input signal with the digital output signal of the PLL in two four-quadrant multiplying digital-to-analog converters.**

***Index Terms*—Mixed-signal integrated circuit, PLL, video signal processing.**

I. Introduction

THIS paper describes a mixed-signal phase-locked-loop (PLL)-based quadrature demodulator with a programmable carrier frequency. The PLL is narrow-band to prevent locking to spurious frequency components near the carrier frequency. This kind of PLL is needed in many applications. This paper describes a design specifically made for a PAL/NTSC color television.

Fig. 1 shows the time-domain representation and the spectrum of a TV signal. The start of each line is signaled with a synchronization (sync) pulse. The picture information is carried as a combination of a luminance signal and a chrominance signal. The chrominance signal contains the color information, quadrature modulated on a subcarrier. The amplitude of the subcarrier is determined by the saturation of the color, and the phase of the subcarrier is determined by the color tint. As the phase of the subcarrier carries information, it is necessary to have an absolute phase reference. This reference is present at the beginning of each line: the burst. With a PLL that is closed during the burst time and open during the rest of the line time (so its oscillator is free-running), a demodulator for the chrominance signal (also called color decoder) can be made. For NTSC signals, the phase of the burst is always the same. For PAL signals, the phase of the burst of one line leads, while the next lags by 45°. So for PAL the PLL must follow the average phase of two successive bursts.

The signal shown in Fig. 1 is just one line. As a TV signal is composed of 15 625 or 15 734 lines per second (PAL or NTSC), the spectrum contains strong components at multiples of this line frequency, all the way up to the upper band limit of the chrominance and luminance signals. The PLL of the demodulator must not lock to any of these harmonics.

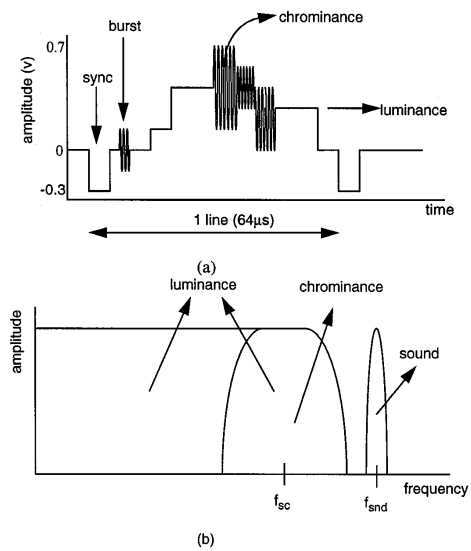


Fig. 1. TV signal in (a) time domain and (b) frequency domain.

There are four different subcarrier frequencies in use around the world. The harmonics of the line frequency of one system can be just a few hundred hertz away from the color subcarrier frequency of another. Therefore, the lock-in range of the PLL must be limited to about 500 Hz. With a bigger lock-in range, the PLL may lock to a multiple of the line frequency of one system, making the lock detector of the PLL think it has locked to a color carrier of another. This is a highly undesirable situation, as it makes automatic detection of the color system being received impossible.

II. Traditional Analog PAL/NTSC Color Demodulator

The traditional way of making a PLL that fulfills the requirements described above is shown in Fig. 2. The core of the PLL is a quadrature voltage-controlled crystal oscillator (VCXO). The VCXO has one (external) crystal for each of the color subcarrier frequencies. Which crystal is connected to the VCXO is determined by an identification circuit. This identification circuit is a

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lock detector with some extra intelligence. The cosine output of the VCXO is connected to a multiplier that multiplies the cosine with the incoming signal. This multiplier (or phase detector) is only active during the burst time. The output of the phase detector connects to a low-pass loop filter. This filter is a series connection of a capacitor (C1) and a resistor (R1). The resistor introduces a zero in the filter transfer to improve the stability and lock-in speed of the PLL. Capacitor C2 suppresses the phase changes of successive bursts for PAL signals. The output of the loop filter is fed to the frequency control input of the VCXO. Apart from the phase detector, the quadrature outputs of the VCXO also drive two multipliers that demodulate the chrominance signal. After low-pass filtering the outputs of the multipliers, the quadrature output signals are available for further processing.

III. Requirements on the New Demodulator

The PLL described above is a very reliable and robust system but has a severe nontechnical drawback: total system cost. Each of the four possible subcarrier frequencies requires its own crystal. As these crystals must be cut such that it is possible to detune them slightly from their nominal frequencies, they are more expensive than "normal" crystals.

Therefore, a PLL with only one crystal, preferably a nontunable one, would bring significant cost savings. If such a PLL can run on a fixed-frequency crystal, this also means it can run on the system clock, if it is part of a larger system. In the latter case the PLL turns into a no-crystal PLL. If the external loop filter can also be integrated, the cost saving will be even higher.

The requirements on the new demodulator can be listed as follows, ordered by importance.

1) Keep the circuit behavior identical to the analog demodulator. The analog system performs well enough, only its cost is too high.
2) Eliminate the need for tunable crystals. The tunable crystals are the most important cost factors of the analog system. The system to which the demodulator will be added has a clock frequency of 24 MHz. If possible, this frequency should be used.
3) Do not digitize the input signal. The demodulator is part of an analog signal processing system. If only one circuit in the signal-processing chain is digital, this means that an analog-to-digital converter (ADC), anti-aliasing filter, digital-to-analog converter (DAC), and reconstruction filter will be necessary to connect the color decoder to the rest of the system. This overhead is important as it increases the cost of the new design, making it harder to compete with the analog demodulator.
4) Integrate the external loop filter. The cost of the external components is not high, but eliminating the loop filter does release a pin of the IC. In signal-processing IC's, pins tend to be very precious, as on the one hand many pins are required to provide maximum flexibility, whereas on the other hand the number of pins must be kept to a minimum for cost reasons.
5) Avoid critical analog components and subcircuits. This is a "nice-to-have" requirement that will make the integration of the new circuit in a bigger system, as well as portability to another process, easier.

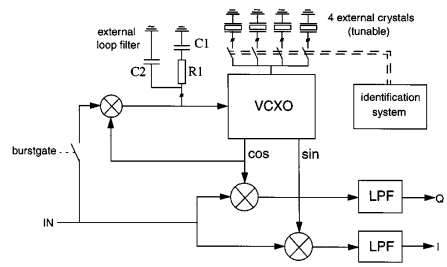

Fig. 2. Traditional analog PAL/NTSC color demodulator.

IV. The New Demodulator

When designing the new demodulator, it is important to bear in mind that it is part of an overall analog signal processing system. A pure digital PLL [1] requires digitization of the input signal and D/A conversion of the output signal. The overhead of the converters is such that a system based on a pure digital PLL would require far more silicon area than the mixed-signal design that will be proposed later in this section. In [2], a discrete-time oscillator (DTO)-based mixed-signal quadrature demodulator, which does not require digitization of the input signal, is described. However, in [2], the output frequency of the DTO is controlled by means of a VCXO. An analog PLL, inside the overall PLL, filters the desired subcarrier frequency components out of the spectrum generated by the DTO. So this solution does not meet items 2) and 5) of our list of requirements.

As the analog system shows a very good performance, the new mixed-signal demodulator was designed with a topology that follows the analog system as much as possible [3]. Fig. 3 shows the block diagram of the new design. The voltage-controlled oscillator has been replaced by a direct digital synthesizer (DDS) [4]. A DDS (Fig. 4) is a circuit that composes a DTO whose output is converted into sine and cosine output words by means of lookup tables (LUT's). The subcarrier frequency is selected by setting the value of K_{nom}, and the deviation from the nominal frequency is determined by input signal K_{flt}. As the sine and cosine are identical functions, but with a time shift, the LUT's do no't need to store complete cycles of both functions. Two LUT's, both storing one-eighth of a cycle, are enough to retrieve the full sine and cosine waveforms [5]. The DDS runs on a 24-MHz clock and is 24 bits wide to attain the required frequency resolution. The output word width of the LUT's only need be six bits for sufficient suppression of the spurious frequencies generated by the DTO.

In a pure digital PLL, the phase detector would be a digital multiplier that multiplies the cosine output signal of the DDS with the digitized input signal. However, as stated above, the input signal should not be digitized in the new system. Therefore, the phase detector of the analog system is replaced by a multiplying DAC in this mixed-signal PLL. A multiplying DAC is one that multiplies the analog input signal by a digital word and outputs an analog signal. A multiplying DAC can be made by a connecting the input signal to a resistor string. The output signal is made by connecting one of the nodes in the string to the

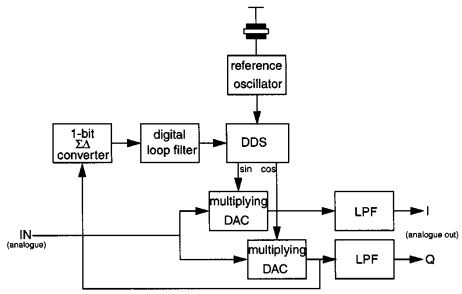

Fig. 3. Mixed-signal quadrature demodulator.

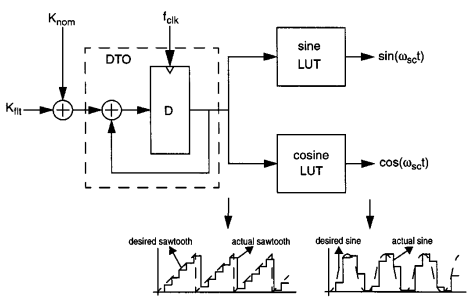

Fig. 4. Block diagram of the direct digital synthesizer.

output node under control of the digital input word [6]. As a multiplying DAC is a rather big circuit in comparison to the phase detector in the analog circuit, one multiplying DAC is used for both the demodulation of the Q-signal and the phase detection.

The ADC at the output of the phase detector is a sigma–delta converter. The phase error is a quasi-dc signal when the PLL is locked. When the PLL is not in lock, the frequency of the phase error signal is maximally twice the catching range (i.e., 1000 Hz) for NTSC signals. For PAL signals, the maximum frequency is half of the line frequency f_H (due to the alternating phase). As the clock frequency is 24 MHz, the oversampling rate is high enough to work with a 1-bit sigma–delta converter [7]. The input structure of the loop filter can act as the decimation filter for the sigma–delta converter's bitstream.

The loop filter is a completely integrated digital filter, so the external components of the analog system are not needed in the new system.

Fig. 5 shows the spectrum of a number of signals in the mixed-signal demodulator. The DTO generates a very wide spectrum, as there is no simple relation between its clock and its output frequency. The LUT's act as very sharp bandpass filters that remove all frequencies, except the desired color subcarrier frequency. As the system is discrete-time, some frequency components around the clock frequency (and its harmonics) will remain. The output spectrum of the multiplying DAC's contains the down-converted chrominance input signal, with its mirror image at two times the subcarrier frequency (and the spectrum around the clock frequency and its harmonics). The low-pass filters at the outputs of the multiplying DAC's remove all the undesired frequency bands, so only the quadrature demodulated chrominance signals remain.

V. Requirements on the Digital Loop Filter

The PLL loop filter is an important component for the overall system performance. As the external loop filter of the analog system is both costly and prone to picking up interference, it was replaced by a fully integrated digital loop filter in the new design. Looking at the loop filter of the analog color decoder PLL, six functions can be distinguished for the digital loop filter.

1) Act as integrator for a (theoretically) infinite open loop response at dc to obtain a zero steady-state phase error (equivalent to C1 of the analog loop filter).
2) Introduce a zero in the phase characteristic (equivalent to R1 of the analog loop filter).
3) Suppress the burst swing in PAL mode (equivalent to C2 of the analog loop filter).
4) Act as a decimation filter for the conversion of the 24-MHz bitstream from the sigma–delta modulator into low-pass filtered two's-complement digital words with the required resolution and a lower sampling frequency.
5) Provide the color decoder PLL with enhanced loop gain in the acquisition mode. In the analog color decoder, the acquisition mode is switched on by increasing the gain of the phase detector. In this mixed-signal PLL, the gain is increased in the loop filter.
6) Limit the tuning range of the digital quadrature generator to ±500 Hz by limiting the output signal of the digital loop filter.

VI. The Loop Filter Configuration

The block diagram of the loop filter for the color decoder PLL is shown in Fig. 6. The up/down counter acts as an integrator (requirement 1). A register that samples the output of the up/down counter at a lower clock frequency acts as down-sampling filter (requirement 4). The differentiator introduces a zero in the transfer characteristic (requirement 2). The averager suppresses the PAL burst swing (requirement 3). The tuning range of the quadrature generator is restricted by the frequency limiter (requirement 6). Requirement 5 is met by switching the step size of the steps with which the up/down counter counts up or down.

The input bitstream controls the direction of the counting of the up/down counter; a digital "1" increases the counter contents by 1 LSB, while a "0" decreases the counter contents by 1 LSB. As the counter is never reset, the low-frequency phase error coded in the bitstream is integrated in the counter. In acquisition mode, the up/down counter counts with steps of 4 LSB instead of 1 LSB.

As the up/down counter acts as an integrator, in the frequency domain, a low-pass characteristic is obtained. Therefore, the up/down counter doubles as a prefilter for the down-sampling process. The 24-MHz bitstream is converted into digital words by the up/down counter, and the quantization noise in the

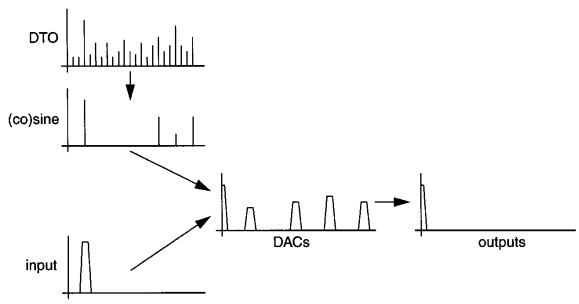

Fig. 5. Spectra of some signals in the new quadrature demodulator.

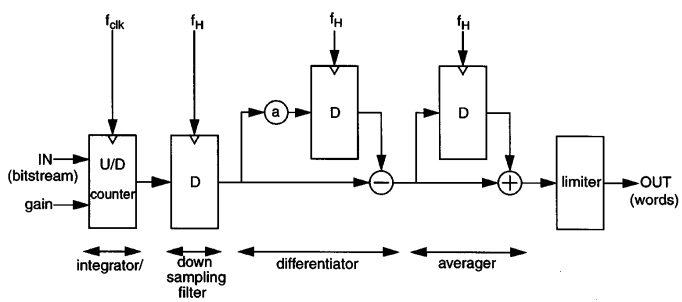

Fig. 6. Block diagram of the digital loop filter.

bitstream is low-pass filtered. The $2f_{sc}$ components that are inherently present at the output of the phase detector are not filtered before digitization by the sigma–delta modulator. They will be correctly coded into the bitstream and will be suppressed by the integrating action of the up/down counter.

When choosing a lower sampling frequency for the remaining part of the digital loop filter, the maximum output frequency of the useful signal of the phase detector (and the sigma–delta modulator) has to be considered. This maximum is determined by the $f_H/2$ burst swing during PAL reception. As there are no signal components higher than half the line frequency, the line frequency was chosen as the sampling frequency of the digital loop filter.

VII. Circuit Realization

The system described above has been integrated in a one-chip TV processor IC (Fig. 7). The one-chip TV processor is an analog signal-processing IC that contains all functions needed to make an analog TV, except the tuner and power amplifiers. The IC is made in a 0.6-μm BiCMOS process. A description of one of this IC's precursors can be found in [8].

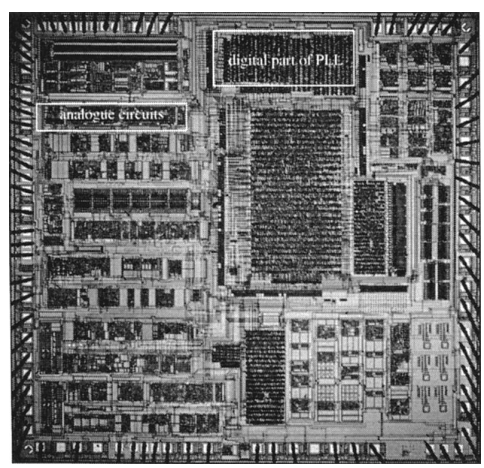

Fig. 7. Die photo of a one-chip TV processor with the mixed-signal quadrature demodulator.

VIII. Experimental Results

Fig. 8 shows a standard European Broadcasting Union color bar input signal and the demodulated output signals. The B-Y and R-Y signals are the I- and Q-output signals of the quadrature demodulator, respectively.

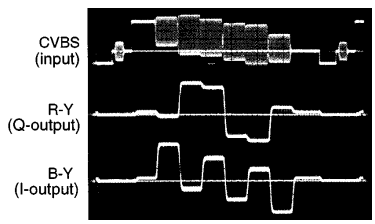

Fig. 8. EBU color bar: CVBS input, R-Y and B-Y output signals.

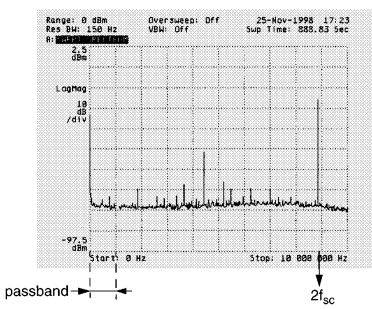

Fig. 9. Output spectrum of the demodulator with a continuous 4.4-MHz input signal.

TABLE I
SYSTEM CHARACTERISTICS

process	0.6μm BiCMOS
area	0.33mm^2 (analogue) 0.78mm^2 (digital)
supply current	6mA @ 5V
clock frequency	24MHz
subcarrier frequencies	3.575611MHz (PAL-M) 3.579545MHz (NTSC-M) 3.582056MHz (PAL-N) 4.433619MHz (PAL-B,G,I)
catching/holding range	+/-500Hz
SNR	54dB (peak-peak signal to rms noise)

Fig. 9 shows the spectrum at the output of one of the multiplying DAC's with a continuous 4.4-MHz sine wave on its input. Using this test signal instead of an actual TV signal means that the spectrum does not show a component at each multiple of the line frequency. The spectrum shows the 8.8-MHz double carrier frequency ($2f_{sc}$) and the dc component that arise due to the demodulation process: $\sin^2(\omega_{sc}t) = 0.5(1 + \cos(2\omega_{sc}t))$. Apart from these frequencies, also a 4.4-MHz component is visible. This component arises due to offset in the circuits' driving the multiplying DAC's. The strongest spurious frequency in the passband ($0, \ldots, 1$ MHz) is at 800 kHz. This frequency is nearly 50 dB down with respect to the $2f_{sc}$ signal. In this measurement, the $2f_{sc}$ signal is taken as the amplitude reference instead of the dc signal. Both have the same amplitude after demodulation, but the spectrum analyzer does not give a correct reading for dc signals. The other spurious frequencies are outside the passband and will be eliminated by the low-pass filter at the output of the multiplying DAC.

Visual tests show that the performance of the presented quadrature demodulator is on a par with that of traditional demodulators for standard video signals and standard viewing conditions. A higher performance (i.e., lower spurious components in the output signal) can be obtained by increasing the number of bits in the LUT's and the DAC's. Increasing the clock frequency will also make it easier to reduce unwanted frequencies.

Table I shows some measured characteristics of the quadrature demodulator system. The measurement results are similar to that of a traditional analog system [9]. Although the new system occupies two times more silicon area than the traditional system, it is very cost-effective thanks to the high cost savings on the external crystals and the loop filter. In the traditional system, the catching/holding range is determined mainly by the characteristics of the external tunable crystal. In the new system, the catching/holding range is determined by the limiting value of the limiter at the output of the digital loop filter. Therefore, the new system shows a lower spread on this parameter.

IX. CONCLUSIONS

A multicarrier quadrature demodulator system has been realized that combines the best elements of the analog and digital worlds. The data path is analog, but everything around it is digital. The link between the analog and the digital domain is a simple 1-bit sigma–delta modulator that only has to convert a quasi-dc signal. Compared to the traditional analog solution, the total system cost is reduced considerably thanks to the elimination of a number of expensive external components. The mixed-signal system requires no external components at all.

ACKNOWLEDGMENT

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appendix C

Calculation of the transfer function of the analogue PLL

Fig. 121 shows the block diagram of the analogue colour decoder PLL. It consists of three parts: a voltage-controlled crystal oscillator VCXO, a multiplying phase detector PD and an external loop filter.

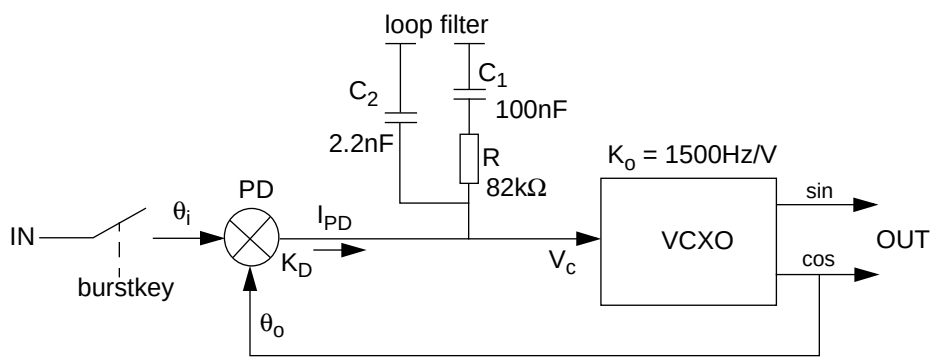

Fig. 121 Block diagram of the analogue colour decoder PLL.

To close the loop of the PLL the cosine output of the VCXO is connected to the phase detector. In the phase detector the phase of the VCXO signal is compared with the phase of the incoming colour burst. The phase detector is shown in Fig. 88. The output current of the phase detector is:

$$I_{PD} = K_D(\theta_i - \theta_o) \tag{32}$$

In this equation I_{PD} is the average output current in µA, θ_i is the phase of the incoming colour burst and θ_o is the phase of VCXO cosine output (both in rad), and K_D is the phase detector gain in µA/rad. As the phase detector is only active during the colour burst, a burst duty-cycle δ has to be taken into account (the output current of the phase detector is zero out-

side the burst intervals). The burst duration is about 3µs per video line (64µs) [70], so the duty cycle δ is about 0.05.

In a switching phase detector the nominal phase detector gain K_{Dnom} is equal to the tail current divided by π/2 [40]. In the phase detector of Fig. 88 the tail current is $2I_{bias}$. Entering all this into equation 32 yields:

$$K_D = \frac{4\delta}{\pi} I_{bias} \tag{33}$$

Two regions of operation have to be distinguished for the phase detector:

1) Acquisition mode
   the PLL is unlocked (e.g. when starting up or when changing the received TV channel). During this mode the acquisition process is accelerated by increasing the phase detector gain by a factor of five to K_D = 16µA/rad.

2) Tracking mode
   the PLL is already in lock and tracks the phase of the incoming colour bursts. In this mode the phase detector gain is K_D = 3.2µA/rad.

The output current of the phase detector is converted into a control voltage V_c for the VCXO by the impedance of the PLL loop filter. The impedance characteristic of the loop filter partly determines the bandwidth and damping of the PLL. However, only C_1 and R in Fig. 121 contribute to these parameters. Capacitor C_2 is not meant to control the PLL's bandwidth and damping. C_2 has only been added to the loop filter for sufficient suppression of the PAL $f_H/2$ burst swing. Therefore C_2 will be left out of the model. In that case the PLL can be treated as a second-order loop with natural frequency ω_n and damping ζ. The closed loop phase transfer function of a second-order PLL in the Laplace domain is [40]:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{34}$$

The phase transfer function of the colour decoder PLL of Fig. 121 can also be written as:

$$\frac{d\theta_o}{dt} = 2\pi f_o = K_o V_c \tag{35}$$

with V_c the control voltage and f_o the output frequency of the VCXO. The VCXO sensitivity K_o is 1500Hz/V = 2π∗1500rad/Vs.

In the Laplace domain equation 35 becomes:

$$\theta_o(s) = \frac{K_o}{s} V_c(s) \tag{36}$$

The transfer of the PLL loop filter is (neglecting C_2):

$$V_c(s) = \left(R + \frac{1}{sC_1}\right) I_{PD}(s) \tag{37}$$

The transfer of the phase detector in the Laplace domain is:

$$I_{PD}(s) = K_D(\theta_i(s) - \theta_o(s)) \tag{38}$$

Combining the equations 36, 37 and 38 gives:

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_D R s + \frac{K_o K_D}{C_1}}{s^2 + K_o K_D R s + \frac{K_o K_D}{C_1}} \tag{39}$$

When comparing equation 39 with the general transfer function of a second-order PLL (equation 34), the natural frequency ω_n and damping ζ of the analogue colour decoder PLL are found to be (note that in [40] K_D is expressed in V/rad, but here K_D is expressed in µA/rad):

$$\omega_n = \sqrt{\frac{K_o K_D}{C_1}} \tag{40}$$

$$\zeta = \frac{R}{2}\sqrt{K_o K_D C_1} \tag{41}$$

The second capacitor C_2 of the loop filter (Fig. 121) introduces a non-dominant pole if $1/RC_2 >> 2\zeta\omega_n$ (the gain of a second-order PLL is one at a corner frequency $\omega = 2\zeta\omega_n$ [40]). In that case it will not have a great influence on the natural frequency ω_n and the damping ζ. C_2 then only improves the attenuation of high frequency components outside the PLL's bandwidth. C_2 was added for just that reason: attenuation of the $f_H/2$ (≈7.8kHz) component in the PAL colour bursts.

appendix D

Calculation of the transfer function of the mixed-signal PLL

PLL model

The block diagram of the mixed-signal colour decoder PLL is shown in Fig. 122. For the calculation of the transfer function in the phase domain the PLL is split up into three parts: the phase detector, the loop filter and the oscillator. The mathematical models of these three components will be derived first. Because of the discrete-time character of the system, the z-transform will be used.

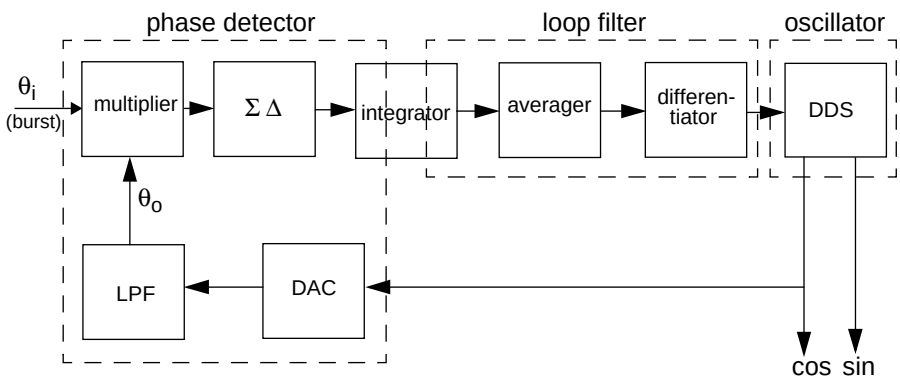

Fig. 122 Block diagram of the mixed-signal colour decoder PLL.

Transfer of the phase detector

A mathematical model for the phase detector of the PLL can be obtained by combining the DAC, the low-pass filter, the multiplier, the sigma-delta modulator and part of the up/down

counter (the input part of the integrator) in one module, as shown in Fig. 123.

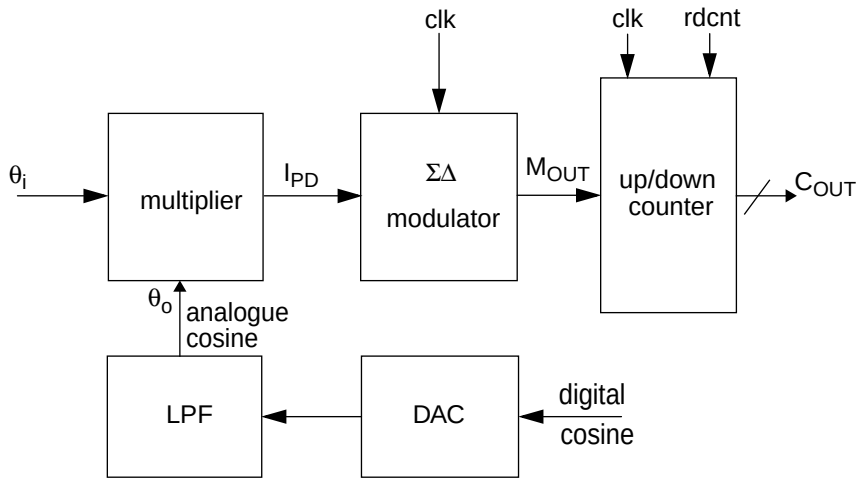

Fig. 123 Block diagram of the phase detector for the calculation of its transfer function.

The transfer function of this phase detector is (with $\Delta\theta = \theta_i - \theta_o$):

$$C_{OUT} = K_D \Delta\theta \tag{42}$$

As its name suggests, the DAC merely converts the digital cosine to an analogue cosine. Hence its transfer function H_{DAC} is $H_{DAC} = 1$. The low-pass filter is only in the system to suppress the clock harmonics. The signal frequency band is completely untouched. Therefore the transfer function of the LPF can also be set at $H_{LPF} = 1$.

The multiplier in Fig. 123 is equal to the one of the analogue system. Note that in the analogue system the multiplier *is* the phase detector, whereas here it is only part of the phase detector. So, the output current of the multiplier is:

$$I_{PD} = K_M \Delta\theta \tag{43}$$

where

$$K_M = \frac{2 I_{PD,\,max}}{\pi} \tag{44}$$

and $\Delta\theta$ is the phase error between D/A converted cosine of the DDS (θ_o) and the analogue colour burst signal (θ_i). This transfer function is identical to the transfer of the phase detector in the analogue system (I_{bias} is called $I_{PD,max}$ in the mixed-signal circuit's phase detector).

The analogue output current I_{PD} is converted into a bitstream by the sigma-delta modulator. When $I_{PD} = 0$ the sigma-delta modulator produces an equal number of ones and zeros during a burst interval (t_b) and the nett output number M_{OUT} of the phase detector is 0. When I_{PD} is a positive current the modulator produces more ones than zeros and M_{OUT} becomes a positive number. When I_{PD} is negative the modulator produces more zeros than ones and M_{OUT} becomes a negative number. If $|I_{PD}| > I_{\Sigma\Delta,max}$ the sigma-delta modulator is overloaded and $|M_{OUT}|$ becomes approximately $|M_{OUT}| = t_b/t_{clk}$. $I_{\Sigma\Delta,max}$ is equal to the current I_{DAC} in Fig. 83.

Assuming the sigma-delta modulator is linear over its full input range and is not overloaded, a linear relation is obtained between the analogue input current and the number of ones (or zeros) in the bitstream during a certain time interval. So, as the phase detector is active only during the burst time t_b, the relation between the number of ones (or zeros) in the bitstream and the analogue input current is:

$$M_{OUT} = \frac{t_b}{t_{clk}} \frac{I_{PD}}{I_{\Sigma\Delta,\,max}} \tag{45}$$

with M_{OUT} the effective number of "up" pulses going to the up/down counter in a burst period (a negative number of "up" pulses means that the contents of the counter will be lower after that burst period), $I_{PD,max}$ the maximum output current of the phase detector and $I_{\Sigma\Delta,max}$ the input range of the sigma-delta modulator.

The up/down counter increases (or decreases) its value by steps of A_{cnt} LSBs. So, C_{OUT} becomes:

$$C_{OUT} = A_{cnt} M_{OUT} \tag{46}$$

Combining equations 42, 43, 44, 45 and 46 yields the complete transfer function of the phase detector:

$$K_D = A_{cnt} \frac{t_b}{t_{clk}} \frac{2I_{PD,\,max}}{\pi I_{\Sigma\Delta,\,max}} \tag{47}$$

If the maximum output current of the phase detector is lower than the maximum input current of the sigma-delta modulator the system will not have an optimum signal-to-noise ratio. If the maximum output current of the phase detector is higher than the maximum input current of

the sigma-delta modulator the system will saturate. Therefore $I_{PD,max}$ was chosen equal to $I_{\Sigma\Delta,max}$. This simplifies equation 47 to:

$$K_D = A_{cnt}\frac{2t_b}{\pi t_{clk}} \tag{48}$$

Transfer of the digital loop filter

The block diagram of the loop filter is shown in Fig. 124. The clock frequency of the loop filter is the line frequency and the (digital) input signal of the loop filter consists of the burst samples from the phase detector (C_{OUT} in Fig. 123).

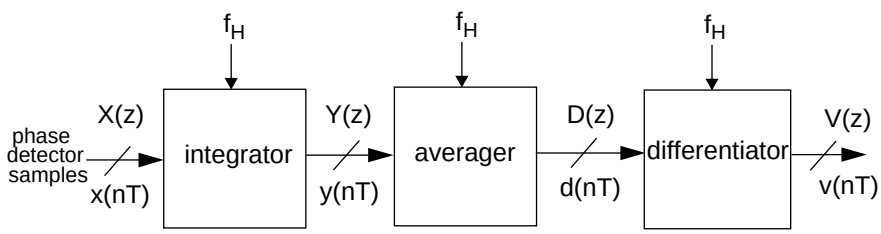

Fig. 124 Block diagram of the digital loop filter.

The function of the up/down counter can be split up in two parts. First, it has an integrating function during one burstkey interval. This function has been taken up in the transfer function of the phase detector (equation 48). The second function of the up/down counter is integration of the successive phase detector samples, resulting from the colour bursts. This second function of the up/down counter will be taken up in the transfer function of the loop filter.

The transfer function of the integrator (i.e. the up/down counter) is:

$$y(nT) = x(nT) + y((n-1)T) \tag{49}$$

Where y(nT) is the current output state of the up/down counter, y((n-1)T) is the counter state in the previous line interval, and x(nT) is the current phase detector sample, resulting from one colour burst.

In the z-domain the equation 49 becomes:

$$Y(z) - (z^{-1}Y(z)) = X(z) \tag{50}$$

So, the transfer of the integrator is:

$$H_{INT}(z) = \frac{Y(z)}{X(z)} = \frac{1}{1-z^{-1}} = \frac{z}{z-1} \tag{51}$$

In the same manner the transfer function of the differentiator (Fig. 81) can be derived.

$$d(nT) = y(nT) - (\alpha_{df} \cdot y((n-1)T)) \tag{52}$$

$$D(z) = Y(z) - (\alpha_{df} \cdot z^{-1} \cdot Y(z)) \tag{53}$$

$$H_{DIFF}(z) = \frac{D(z)}{Y(z)} = 1 - (\alpha_{df} \cdot z^{-1}) = \frac{z-\alpha_{df}}{z} \tag{54}$$

The transfer function of the averager of Fig. 80 is:

$$H_{AV}(z) = 1 + z^{-1} \tag{55}$$

For frequencies within the bandwidth of the PLL this can be approximated by:

$$H_{AV}(z) \approx 2 \tag{56}$$

Combining all the above yields the transfer function of the complete digital loop filter:

$$H_{DLF}(z) = 2\frac{z-\alpha_{df}}{z-1} \tag{57}$$

Transfer of the DDS

The output phase $\theta_o(nT)$ of the DDS at time nT is:

$$\theta_o(nT) = \theta_o((n-1)T) + \omega T \tag{58}$$

With:

$$\omega = K_o V_{IN}((n-1)T) \tag{59}$$

where K_o is the oscillator sensitivity in rad/s per LSB and V_{IN} is the input signal of the oscillator in LSBs.

Combining equations 58 and 59 gives:

$$\theta_o(nT) = \theta_o((n-1)T) + K_o T V_{IN}((n-1)T) \tag{60}$$

Or, in the z-domain:

$$\theta_o(z) = z^{-1}\theta_o(z) + z^{-1}K_o T V_{IN}(z) \tag{61}$$

From this the transfer of the DDS can be calculated:

$$H_{DDS}(z) = \frac{\theta_o(z)}{V_{IN}(z)} = \frac{K_o T}{z-1} \tag{62}$$

Transfer of the mixed-signal demodulator

The open-loop transfer function of the complete colour decoder PLL in the z-domain is obtained by combining equations 48, 57 and 62:

$$H_{ol}(z) = \left(\frac{\theta_o(z)}{\theta_i(z)}\right)_{ol} = H_D(z)H_{DLF}(z)H_{DDS}(z) \tag{63}$$

The transfer function of the phase detector in the z-domain follows from equation 48:

$$H_D(z) = K_D \tag{64}$$

with: $\Delta\theta(z) = \theta_i(z) - \theta_o(z)$. Equation 63 then becomes:

$$H_{ol}(z) = \frac{2K_D K_o T(z-\alpha_{df})}{(z-1)^2} \tag{65}$$

From equation 65 the closed loop transfer function of the colour decoder PLL can be derived:

$$H_{PLL}(z) = \frac{\theta_o(z)}{\theta_i(z)} = \frac{2K_o K_D T(z-\alpha_{df})}{(z-1)^2 + 2K_o K_D T(z-\alpha_{df})} \tag{66}$$

In order to determine the natural frequency ω_n and the damping ζ of this discrete-time PLL its transfer function has to be compared with the general transfer function of a second-order continuous-time PLL, as given by equation 34. Therefore equation 66 has to be converted to the complex frequency domain using:

$$z = e^{j\omega T} = \cos(\omega T) + j\sin(\omega T) \tag{67}$$

For low signal frequencies ($\omega T << 1$), z can be approximated by:

$$z \approx 1 + j\omega T \tag{68}$$

which in the Laplace domain becomes:

$$z \approx 1 + sT \tag{69}$$

When replacing z by $1+sT$ in equation 66 a continuous-time approximation is obtained for the transfer function of the PLL:

$$H_{PLL}(s) \approx \frac{2K_oK_Ds + \dfrac{2K_oK_D(1-\alpha_{df})}{T}}{s^2 + 2K_oK_Ds + \dfrac{2K_oK_D(1-\alpha_{df})}{T}} \tag{70}$$

Comparing equation 70 with the general transfer function of the second-order PLL in the Laplace domain leads to the following equations for natural frequency ω_n and damping ζ of the mixed-signal colour decoder PLL:

Natural frequency:

$$\omega_n = \sqrt{\frac{2K_oK_D(1-\alpha_{df})}{T}} \tag{71}$$

Damping:

$$\zeta = \sqrt{\frac{K_oK_DT}{2(1-\alpha_{df})}} \tag{72}$$

In the above equations $K_o = 2\cdot\pi\cdot 1.43\text{Hz/LSB} \approx 9.0\text{rad/LSB}\cdot\text{s}$, and $T = 64\mu\text{s}$. The

mixed-signal colour decoder PLL should have the same properties as the analogue colour decoder PLL. So, $\omega_n = 550$rad/s and $\zeta = 2.25$ in the tracking mode, and $\omega_n = 1228$rad/s and $\zeta = 5$ in the acquisition mode. This can be achieved by choosing optimal values for the parameter A_{cnt} (which determines the value of K_D (equation 47)) and α_{df}. For α_{df} the value $\alpha_{df} = 1\text{-}2^{-7}$ was chosen. This way the factor α_{df} can be realised by bit-shifting and adding instead of using a multiplier. This is advantageous as multipliers are very large circuits, while adders are fairly small. With the above value for α_{df}, $A_{cnt} = 2.7$ is needed for the tracking mode and $A_{cnt} = 13.5$ for the acquisition mode. As these are awkward values in a digital circuit, in the test IC the values $A_{cnt} = 2$, $A_{cnt} = 4$, $A_{cnt} = 8$ and $A_{cnt} = 16$ were implemented. In a final implementation in a one-chip TV processor IC the two values that satisfy the system requirements best will be chosen.

appendix E

Influence of the differential amplifier on the measurement error

To make optimum use of the I_{CCQ} test the voltage on the inputs of the differential pairs should have a specific value. If the voltage between their inputs exceeds 100mV nearly all current flows in one branch. This means that even with an extremely low measurement fault the calculation of the ratio of the collector currents will show a great measurement error. On the other hand, if the voltage on the inputs is zero, there is no information at all. So, there must be a value of the input voltage that gives the most accurate measurement.

The collector currents of the differential pair are measured. The input voltage V_{IN} of the differential pair is:

$$V_{IN} = \frac{kT}{q} ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{73}$$

where I_{C1} and I_{C2} are the collector currents. The collector currents are averaged over two measurements to cancel out its offset. For simplicity it is assumed that the differential pair has no offset and only one measurement is done.

The measurement error is assumed to be a fixed percentage of the full-scale current. The total tail current is assumed equal to full-scale current of the current meter. In the following equation ε represents the absolute measurement error. Based on the previous ε is defined as $\varepsilon = I_{tail}/\beta$, where β is the full-scale error.

The measurement error on the voltage drop on the supply line is taken as the difference of the maximum and the minimum voltage that are possible with the measurement error of the currents, and divide this number by two:

$$V_{err} \leq \frac{kT}{2q}\left(ln\left(\frac{I_{C1} + \varepsilon}{I_{C2} - \varepsilon}\right) - ln\left(\frac{I_{C1} - \varepsilon}{I_{C2} + \varepsilon}\right)\right) \tag{74}$$

First we define $I_{C1} = (1-\gamma)I_{tail}/2$, and $I_{C2} = (1+\gamma)I_{tail}/2$. Next we define $\alpha = I_{C1}/I_{C2}$. From this it follows that $\gamma = (1-\alpha)/(1+\alpha)$ and

$$\alpha = e^{\left(\frac{qV_{IN}}{kT}\right)} \tag{75}$$

To get the relative error the absolute error voltage is divided by the actual voltage drop.

$$error \leq \frac{V_{err}}{V_{IN}} \tag{76}$$

The brave of heart will combine all the above equations and (try to) differentiate the resulting error function to find the optimum voltage drop V_{IN}. However, apart from knowing the optimum voltage drop it is also important to know how flat the optimum is. Therefore it is more informative to simply feed the equations into a computer and plot the error function.

Fig. 125 shows the error function for $\beta = 1000$ (i.e. a full-scale measuring error of 0.1%). The optimal input voltage is 39mV, but for voltages in the range between 10 and 80mV the error is less than twice the error at 39mV. This means that the measurement error is rather insensitive to variation of the voltage drop in the supply lines. This is important as the voltage drop will vary from batch to batch and also with temperature. The insensitivity of the measurement error to variation in the voltage drop in the supply lines also allows minor changes in the circuit to be made without having to reconnect the I_{CCQ} measurement points.

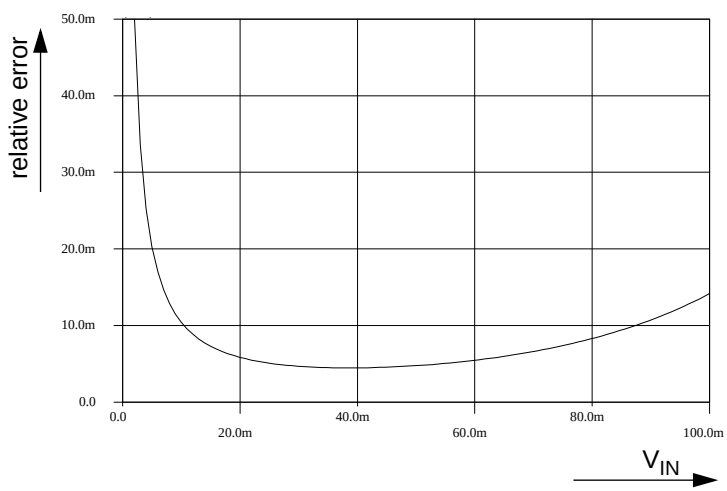

Fig. 125 Relative measurement error as a function of V_{IN}.

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original contributions

1) add-on circuit to significantly reduce the unity-gain bandwidth of a g_mC filter with an arbitrary transconductor

2) analysis of the limitations and simple noise analysis of the add-on circuit

3) derivatives of the add-on circuit with increased DC gain

4) adaptation of the add-on circuit for application in an offset cancellation loop

5) analysis and comparison of several PLL configurations closely related an analogue PLL for use in a quadrature demodulator, with the aim of eliminating external crystals

6) anti-quantisation noise keying pulse for the PLL

7) reduction of the influence the PAL +/-45^o phase jumps by using a line-averager instead of a capacitor-equivalent in the digital loop filter

8) use of the (parasitic) resistance of supply lines as conversion resistor to enable current measurement in these lines through the voltage drop across them

9) IC test method based on the above that is non-invasive to the circuits-under-test

10) test method for ICs based on (supply current) matching of individual circuits (I_{CCQ} testing)

11) a low-overhead implementation of the above test method through multiplexing of measurement points with a distributed shift register

12) statistically relevant test data through the introduction of the I_{CCQ} test method in a mass-produced IC

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summary

This dissertation describes integrated circuit techniques for one-chip TV systems which focus on lowering the total cost of the application. Three different approaches to cost reduction are explored.

Chapter 3 describes an integrator circuit with a low unity-gain bandwidth. This circuit is applied in a voltage controlled crystal oscillator to minimise the offset on the quadrature outputs. The integrator circuit can be regarded as an integrated alternative to a large external capacitor.

Chapter 4 describes a mixed-signal quadrature demodulator that performs as much as possible of the signal processing in the digital domain, without digitising the input signal. This demodulator is an example of a subsystem that has been designed to use the signals that are already present in the IC to such an extent, that this subsystem no longer needs its own external components.

Chapter 5 discusses a fast, generic test method for analogue VLSI circuits. This test method reduces the test time of an IC significantly with a only small number of additional components. The test method is non-invasive to the circuits under test. The additional components only monitor the supply current of the circuits, so they have no influence whatsoever on the operation of the IC.

samenvatting

Circuittechnieken voor low-cost one-chip TV systemen

Dit proefschrift beschrijft circuittechnieken voor geintegreerde schakelingen voor TV systemen waarbij de nadruk ligt op het verlagen van de kosten van de totale applicatie. Drie verschillende werkwijzen worden beschreven.

Hoofdstuk 3 beschrijft een integratorschakeling met een laag versterking-bandbreedte product. Deze schakeling wordt toegepast in een spanningsgestuurde kristaloscillator om de offsetspanning op de kwadratuuruitgangen te minimaliseren. De integratorschakeling kan beschouwd worden als een geintegreerde versie van een grote externe condensator.

Hoofdstuk 4 beschrijft een mixed-signal kwadratuurdemodulator die de signaalbewerking zoveel mogelijk in het digitale domein uitvoert, zonder het ingangssignaal te digitaliseren. Deze demodulator is een voorbeeld van een subsysteem dat zodanig ontworpen is dat externe componenten voor dit subsysteem overbodig zijn, doordat optimaal gebruik gemaakt wordt van de signalen die al aanwezig zijn in het IC.

Hoofdstuk 5 beschrijft een snelle, generieke testmethode voor analoge VLSI schakelingen. Deze testmethode vermindert de testtijd van een IC aanzienlijk met gebruikmaking van slechts een gering aantal extra componenten. De testmethode vereist geen veranderingen aan de schakelingen in het IC. De extra componenten meten slechts de voedingsstromen van de schakelingen in het IC, waardoor zij geen enkele invloed uitoefenen op de werking van het IC.

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biografie

Joop van Lammeren is in 1960 in Papenveer geboren. In november 1983 studeerde hij af bij de vakgroep Elektronica, afdeling Elektrotechniek, van de Technische Universiteit Delft. Sinds januari 1984 werkt hij bij Philips Semiconductors in Nijmegen aan analoge en mixed-signal IC's. Tijdens het schrijven van dit proefschrift was hij Product Team Leader High-End TV ICs.