Wideband Low-Noise Integrated SQUID Systems

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Cover: Optical micrographs of (from left to right): Ramp-type Nb/Al,AlO_x/Al/Nb Josephson junctions, a single dc SQUID of the prototype coded SQUID arrays and the first dc SQUID based on ramp-type Nb/Al,AlO_x/Al/Nb junctions. Background: Sensor SQUID of a two-stage SQUID system.

The work described in this thesis has been performed in the Low Temperature Division of the Department of Applied Physics at the University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands.

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PROEFSCHRIFT

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dr. ir. J. Flokstra (assistent-promotor)

Contents

Chapter 1

Introduction

For centuries, the perpetual motion machines have intrigued mankind and various designs of these machines have been developed. One of the first perpetual motion machines was suggested in 1150 in India by Bhaskara. Via the Arabs, the idea of a machine that could produce continuous power was picked up in Europe. In the 13th century, the medieval architect Villard de Honnecourt made the first European sketch of a perpetual motion machine and in the 15th century, Leonardo da Vinci made several drawings of machines that should generate 'free' energy.

Today, two main kinds of perpetual motion are distinguished: (1) the continual motion of a machine which creates its own energy, thereby violating the 1st law of thermodynamics[i]; (2) any device which converts heat completely into work, thereby contravening the 2nd law of thermodynamics[ii] [1]. Figure 1.1 shows the lithograph "Waterfall" made in 1961 by Escher. It can be seen as an example of a perpetual motion machine of the first kind: The water runs downwards in a closed cycle, turning the mill wheel and generating energy continuously. However, although this construction looks very realistic on paper, it can never be realized in reality.

In the McGraw-Hill Dictionary of Scientific and Technical Terms [2], a third kind of perpetual motion machine is distinguished. A perpetual motion machine of the third kind is a device which has a component that can continue moving forever. This type of device however, is *not* impossible to create although it cannot perform useful work. An example of a perpetual motion machine of the third kind is a superconductor. When cooling down a superconductor below its critical temperature T_c, its electrical resistance vanishes completely. Consequently, if a direct current is caused to flow in a superconducting ring, this current will continue to flow without application of any external force. From experiments it has been estimated that the lower bound of the characteristic decay time of the current is some 10^5 years [3].

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[i] The 1st law of thermodynamics tells us that in any process energy is conserved. This implies that a perpetual motion machine of the first kind cannot be created.

[ii] The 2nd law of thermodynamics imposes limits on the efficiency of processes that convert heat into work: A process whose only effect is the complete conversion of heat into work is impossible. Therefore, it is impossible to create a perpetual motion machine of the second kind.

Fig. 1.1 "Waterfall" by M.C. Escher. © 2002 Cordon Art, Baarn, The Netherlands [4]. All rights reserved. Used by permission.

Hence, if we see the perpetual flow of water in Escher's lithograph as a metaphor for a perpetual electrical current flowing in a superconducting ring, we can conclude that his idea was not completely unrealistic. Unfortunately, the metaphor cannot be extended to the mill: The first law of thermodynamics precludes the use of a 'mill' in a superconducting ring to generate energy, as was discussed above.

Soon after the discovery of superconductivity in 1911, scientists started thinking about practical applications for superconductors. Although various applications have been developed, up to now only a few applications have proven to be of real commercial value. One of the most successful applications is magnetic resonance imaging (MRI) [5], which is increasingly used as a non-invasive medical diagnostic tool. Superconducting magnets are perfectly suited for MRI as they allow the generation of very high, uniform magnetic fields. These high-field superconducting magnets are essential for several other applications, such as particle accelerators used in high-energy physics [6].

Another successful application is the direct current superconducting quantum interference device (dc SQUID), originally developed in 1964 by Jaklevic *et al.* [7,8]. A dc SQUID consists of a superconducting loop, interrupted by two weak links, the Josephson junctions. Today, the dc SQUID is well known to be the most sensitive sensor for magnetic flux available and has therefore a wide range of applications, from the detection of very small magnetic fields produced by the human brain or heart [9] and picovoltmeters [10] to non-destructive testing of aircraft wheels [11] and the readout of cryogenic particle detectors [12,13] or gravitational wave antennae [14,15].

Archeologists for example, used SQUIDs to successfully unearth the ruins of the Cleopatra Palace during the excavations in Egypt in 1996 [16].

Although SQUIDs can be fabricated using a variety of superconductors, the devices discussed in this thesis are based on the low-T_c metallic superconductor Nb, which has a critical temperature of 9.2 K. These SQUIDs are generally operated as flux-to-voltage converters at a temperature of 4.2 K in liquid ^{4}He. However, the flux-to-voltage transfer of a conventional dc SQUID is rather small, such that a direct voltage readout mode, i.e. a readout mode with a room temperature dc preamplifier directly connected to the dc SQUID, leads to preamplifier limitation of the overall system sensitivity. One of the possibilities to solve this matching problem is to increase the flux-to-voltage transfer of the SQUID. For this reason, various second generation dc SQUIDs with a large flux-to-voltage transfer have been developed. The Low Temperature Division at the University of Twente has a long tradition in the development of one of these second generation dc SQUIDs, the double relaxation oscillation SQUID (DROS). This thesis concerns the development and further improvement of SQUID systems based on DROSs and is a continuation of earlier work discussed in the theses of Adelerhof [17] and Van Duuren [18].

In chapter 2 of this thesis, the basics of conventional dc SQUID systems, three different concepts of second generation dc SQUIDs and the operation principles of digital SQUIDs are presented. As is discussed, both second generation dc SQUIDs and digital SQUIDs allow large measurement bandwidths and high slew rates. This is essential for certain applications, such as the readout of cryogenic detectors. Currently, large arrays of cryogenic particle detectors are under development [19], which require sophisticated readout systems to reduce the number of SQUIDs. In chapter 3, the readout of cryogenic particle detectors by means of a SQUID is briefly discussed, followed by a theoretical survey of different kinds of multiplexing that can be used for the readout of large arrays. By using a SQUID system based on code-division multiplexing, the so-called coded-SQUID array, the number of SQUIDs can be reduced considerably. The design of and the experimental results on prototype coded SQUID arrays are presented in chapter 3.

A two-stage SQUID system is just one example of a second generation dc SQUID. It consists of a sensor SQUID and a second stage SQUID that serves as a low-noise cryogenic preamplifier, as is discussed thoroughly in chapter 4. At the University of Twente, we have developed two-stage SQUID systems based on a conventional dc SQUID as the sensor SQUID and a DROS as the second stage. This configuration enables simple readout electronics together with large bandwidths and excellent noise characteristics: The overall system sensitivity of a two-stage SQUID system is determined by the sensor SQUID and not by the second stage or the readout electronics.

Chapter 5 describes the operation principle, the optimization and the design of a digital SQUID based on a DROS, the Smart DROS. The Smart DROS integrates a DROS and a superconducting counter, which linearizes the output of the DROS, on one single chip. This integrated design allows very large bandwidths and slew rates that are orders of magnitude higher than that of standard analogue SQUID systems. Optimized Smart DROSs with high slew rates have been fabricated and characterized. The experiments showed proper operation.

In order to further improve the characteristics, e.g. noise properties and slew rates, of two-stage SQUID systems and Smart DROSs, the capacitance and thus the effective area of the Josephson junctions can be reduced. A useful technique for the fabrication of small-area Josephson junctions utilizes an edge geometry. In chapter 6, the fabrication and the first experiments on these so-called ramp-type junctions and dc SQUIDs based on ramp-type junctions are discussed.

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Chapter 2

SQUIDs

The direct current superconducting quantum interference device (dc SQUID) is well known to be the most sensitive sensor for magnetic flux with a sensitivity that can approach the quantum limit and with a frequency response extending from dc to a few GHz. In sections 2.1 and 2.2, the two keystones of the dc SQUID, the operation principles and some practical aspects of the dc SQUID are discussed.

In most applications, the dc SQUID is used as a flux-to-voltage converter. Since the output voltage is nonlinearly dependent on the applied signal flux, the SQUID is generally operated as a null-detector in a feedback loop, the flux locked loop (FLL). Conventionally, the FLL is implemented in room temperature electronics. Although the output of the SQUID is linearized in this way, the usable bandwidth is limited by the FLL electronics to only a few MHz. Moreover, the flux-to-voltage transfer of a conventional dc SQUID is so small that its output voltage noise is about one order of magnitude smaller than the input voltage noise of a low-noise room temperature dc preamplifier. This leads to preamplifier limitation of the overall system sensitivity in a direct voltage readout mode. For this reason, various second generation dc SQUIDs with a larger flux-to-voltage transfer have been developed. In section 2.3, the series SQUID array, the double relaxation oscillation SQUID (DROS) and the two-stage SQUID system are presented as three examples of the second generation dc SQUIDs.

Dead-time in the feedback loop originating from the transmission delay introduced by the wiring between the SQUID and the room temperature FLL electronics limits the maximum bandwidth that can be achieved. By integrating the SQUID and the FLL circuitry on one chip, the dead-time can be reduced and thus the attainable bandwidth can be increased. This is, for example, advantageous for high-speed applications or when using the SQUID in an unshielded environment. The digital SQUID that combines a SQUID and a digital FLL circuitry on one single chip is discussed in section 2.4 and in section 2.5 it is discussed that each application may require a different SQUID system.

2.1 Superconductivity

For many years after the discovery of superconductivity by Holst and Kamerlingh Onnes in 1911, it has been believed that superconductors had the same properties as normal conductors except for the fact that they showed infinite conductivity below their critical temperatures. In 1933 however, Meissner and Ochsenfeld

demonstrated that a superconductor is a perfect diamagnet, i.e. it is strongly repelled by a magnetic field and it tends to expel a magnetic field from its interior by superconducting screening currents flowing in the surface layer. As a result of this so-called Meissner effect, the magnetic field in the superconductor decreases exponentially over a characteristic length λ_L, the London penetration depth. From that time on, perfect diamagnetism rather than zero resistance was taken to be the fundamental and most revealing property of superconductors.

In 1950, London predicted that any internal magnetic flux in superconductors exists only in discrete amounts. This effect called flux quantization is one of the keystones of the dc SQUID. The second physical phenomenon of superconductivity on which the dc SQUID is based, is called Josephson tunneling. In this section, these two phenomena of superconductivity are discussed briefly. More details about the theory of superconductivity can be found in textbooks on this subject [1,2,3].

2.1.1 Flux quantization

In 1950, years before the microscopic, fundamental theory of Bardeen, Cooper and Schrieffer (BCS theory) was available, London predicted that the internal magnetic flux in superconductors was quantized. Just on the basis that superconductivity represented a macroscopic ordered state and assuming that single electrons were the basic supercurrent carriers, he predicted that the quantization unit was h/e. Here, $h = 6.63{\cdot}10^{-34}$ Js is Planck's constant and $e = 1.60{\cdot}10^{-19}$ C is the charge of an electron.

Instead of the several earlier macroscopic theories, the microscopic BCS theory that was presented in 1957 explained the physical phenomena of superconductors for the first time as consequences of the fundamental laws of physics. The BCS theory however, states that not single electrons but electrons grouped in pairs are the basic supercurrent carriers. In 1956, Cooper already showed that due to the strong electron-phonon interaction in a superconductor, it is energetically favorable for electrons to condense into so-called Cooper pairs at the Fermi energy.

Flux quantization results from the condensation of electrons into Cooper pairs, all occupying the same quantum state, which can be described by a single complex wave function $\Psi = \left|\Psi(\mathbf{r})\right| e^{i\varphi(\mathbf{r})}$. The squared amplitude $\left|\Psi(\mathbf{r})\right|^2$ is proportional to the density of conduction electrons that are condensed into the superconducting state. The phase φ of the wave function is dependent on the supercurrent density $\boldsymbol{J_s}$ and the magnetic vector potential $\boldsymbol{A}$ through [3]

$$\nabla\varphi = 2\pi\left(\frac{2m}{hn_s e}\boldsymbol{J_s} + \frac{2e}{h}\boldsymbol{A}\right). \tag{2.1}$$

In this equation, $m = 9.11{\cdot}10^{-31}$ kg is the mass of an electron and n_s is the number of superconducting electrons per m^3. The single valuedness of the complex wave function requires that along an arbitrary closed path, the phase difference $\Delta\varphi$ is zero (modulo 2π). This phase difference can be found by integrating Eq. (2.1) along a closed path. Taking a path inside the superconductor away from the surface by a

distance larger than λ_L, i.e. where the supercurrent density is zero, and using Stokes' theorem, the phase difference along this path can be written as

$$\Delta\varphi = 2\pi\frac{2e}{h}\oint_c \boldsymbol{A}\cdot\boldsymbol{dl} = 2\pi\frac{2e}{h}\int_a \boldsymbol{B}\cdot\boldsymbol{da} = \mathrm{n}2\pi\,, \tag{2.2}$$

where n is an integer. This can be rearranged to

$$\int_a \boldsymbol{B}\cdot\boldsymbol{da} = \Phi = \mathrm{n}\frac{h}{2e} = \mathrm{n}\Phi_0\,. \tag{2.3}$$

Thus the actual flux quantization unit, the flux quantum, is $\Phi_0 = h/2e$ instead of h/e as predicted by London. As was discussed above, this discrepancy is simply the result of his assumption that single electrons were the supercurrent carriers instead of Cooper pairs.

2.1.2 Josephson tunnel junctions

In 1962, Josephson predicted that two superconducting electrodes separated by a thin insulating layer[i] would display remarkable electromagnetic properties [4]. If the insulating layer is sufficiently thin, the wave functions in both electrodes overlap and Cooper pairs can tunnel from one electrode to the other and according to the dc Josephson equation, a zero voltage supercurrent

$$I_{CP} = I_0 \sin\phi\,, \tag{2.4}$$

will flow. Here, I_0 is the critical current, i.e. the maximum supercurrent, and ϕ is the phase difference between the wave functions in both electrodes. If the current through the junction is larger than I_0, a voltage V will appear across the junction and the phase difference changes in time

$$\frac{\partial\phi}{\partial t} = \frac{2e}{\hbar}V = \frac{2\pi}{\Phi_0}V\,. \tag{2.5}$$

This is the so-called ac Josephson equation. The Josephson equations imply that a time-averaged voltage $<V>$ across the Josephson junction causes an oscillating supercurrent with an amplitude I_0 and a frequency $f_J \approx (484\ \mathrm{MHz/\mu V})<V>$. Both the dc and the ac Josephson effect have been confirmed by a large number of experiments and nowadays, the Josephson junction is the basic element of many superconducting devices, such as the superconducting quantum interference device (SQUID).

At a temperature $T = 0$ K, all conduction electrons are condensed into Cooper pairs at the Fermi energy. At finite temperatures however, some Cooper pairs are thermally excited and electron-like and hole-like charge carriers, the quasiparticles,

[i] Although various kinds of Josephson junctions have been developed, in this thesis only the low-T_c superconductor-insulator-superconductor (SIS) Nb/Al,AlO_x/Al/Nb Josephson tunnel junctions are discussed.

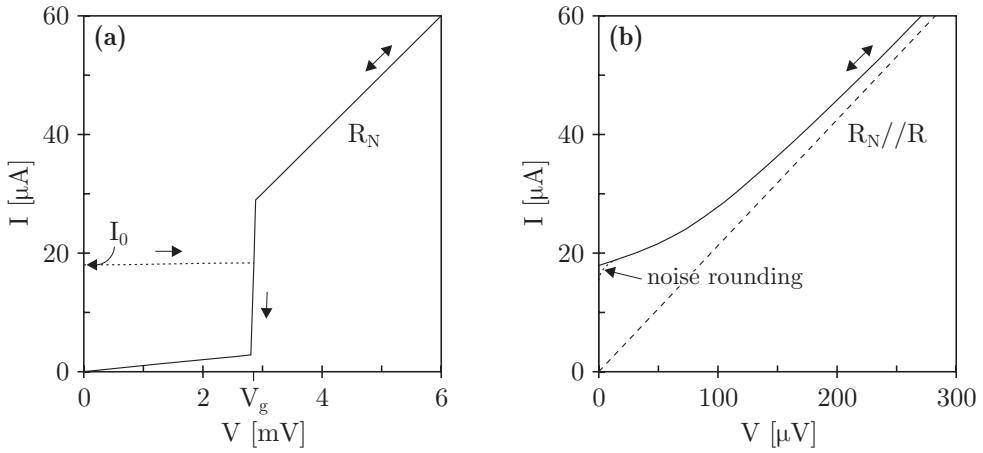

Fig. 2.1 Simulated current vs. voltage (I-V) characteristics of Josephson tunnel junctions. **(a)** Hysteretic junction with $I_0 = 18$ μA, $V_g = 2.8$ mV and $R_N = 100$ Ω. **(b)** Non-hysteretic junction with the same parameters as **(a)** but now shunted with a resistor $R = 4.7$ Ω. This corresponds to a McCumber parameter of $\beta_C = 0.3$. For these numerical simulations using JSIM [5], the effect of noise is not included. In experimental non-hysteretic junctions, noise rounding will appear around $I = I_0$, as is schematically shown.

are formed. If a voltage bias smaller than the gap voltage, $V_g = (\Delta_A + \Delta_B)/e$, is applied to the Josephson tunnel junction, only the thermally excited quasiparticles can tunnel through the insulating barrier, resulting in a small, temperature-dependent tunnel current. Here, $\Delta_{A,B}$ are the energy gaps of the electrodes. For the fabrication process of Nb/Al,AlO_x/Al/Nb Josephson junctions at the University of Twente, the gap voltage is $V_g \approx 2.8$ mV. At bias voltages above V_g, the potential difference supplies enough energy to break Cooper pairs. The result is that the quasiparticle tunnel current suddenly increases at $V = V_g$, as is shown in Fig. 2.1a. At voltages much larger than V_g, the Josephson tunnel junction shows ohmic behavior with a normal resistance R_N.

The amount of hysteresis in the I-V characteristic of the Josephson tunnel junction can be estimated by the widely used RCSJ (resistively and capacitively shunted junction) model[ii] [6,7]. In this model, the Josephson junction is represented by an ideal Josephson element, described by Eqs. (2.4) and (2.5), that is shunted with a resistance R_j and a capacitance C_j. The linear resistance R_j that is used in the RCSJ model should be chosen to represent the effective resistance of the strongly nonlinear quasiparticle resistance and an (optional) additional shunt resistance as well as possible in the relevant voltage regime [1,6]. The capacitance C_j is the capacitance between the electrodes of the junction. If the Josephson junction

[ii] To develop a better understanding of the Josephson dynamics and the hysteresis in a Josephson tunnel junction, simple mechanical analogs have been developed. A useful analog is a ball moving in a "tilted washboard" potential along the coordinate ϕ with a velocity $\partial\phi/\partial t$. For further reading, the reader is referred to, e.g., refs. [1] and [2].

is biased with a constant current I, this current distributes over the three channels. Thus the circuit equation can be written as

$$I = C_j \frac{\partial V}{\partial t} + \frac{V}{R_j} + I_0 \sin\phi \,. \tag{2.6}$$

Using Eq. (2.5), this can be written as

$$\frac{I}{I_0} = \beta_C \frac{\partial^2 \phi}{\partial \theta^2} + \frac{\partial \phi}{\partial \theta} + \sin\phi \,, \tag{2.7}$$

where $\theta = (2\pi I_0 R_j / \Phi_0)t$ and

$$\beta_C = \frac{2\pi I_0 R_j^2 C_j}{\Phi_0} \,, \tag{2.8}$$

is the so-called McCumber parameter. If $\beta_C < 1$, the I-V characteristic of the Josephson junction is non-hysteretic and if $\beta_C > 1$, the junction shows hysteretic behavior. Thus to remove the junction hysteresis, the junction can be shunted with an additional resistance R, which should be small enough such that the McCumber parameter becomes smaller than unity. A simulated I-V characteristic of a shunted, non-hysteretic junction is shown in Fig. 2.1b. In this simulation, the effect of thermal noise was neglected. In non-hysteretic junctions however, thermal noise can cause "noise rounding" of the I-V characteristics at $I \approx I_0$, as is shown in Fig. 2.1b. The noise rounding is described by the noise parameter

$$\Gamma = \frac{k_B T}{I_0 \Phi_0 / 2\pi} \,, \tag{2.9}$$

which is the ratio between the thermal energy, $k_B T$, and the Josephson coupling energy, $I_0\Phi_0/2\pi$ [4]. Here, $k_B = 1.38 \cdot 10^{-23}$ J/K is the Boltzmann constant. Numerical simulations have shown that as long as $\Gamma < 0.2$, the effect of the thermal energy fluctuations in the total energy of the Josephson junction is small [8]. For $T = 4.2$ K, this means that the critical current should be larger than $I_0 = 0.9$ μA. For a noise parameter $\Gamma \geq 1$, the I-V characteristic is so strongly disturbed that the junction shows almost ohmic behavior.

2.2 DC SQUIDs

The two keystones of the dc SQUID, flux quantization and Josephson tunneling, were discussed in the previous section. In this section, the dc SQUID is discussed, starting with its operation principle.

2.2.1 Operation principle

Basically, the dc SQUID consists of a superconducting loop with inductance L_{sq}, interrupted by two identical Josephson junctions each with a critical current I_0, as

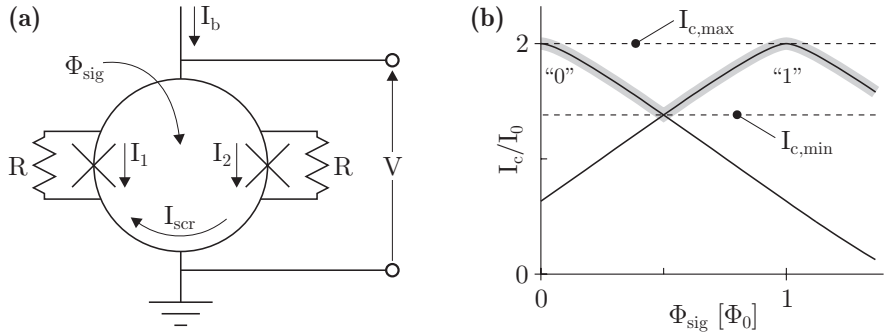

Fig. 2.2 (a) Scheme of a dc SQUID. The crosses represent the Josephson junctions and the shunt resistors can be used to remove the junction hysteresis. **(b)** Threshold characteristics of a dc SQUID for the n = 0 and the n = 1 flux quantum state. The screening parameter of the SQUID is $\beta_L = 2I_0L_{sq}/\Phi_0 = 2$. The gray region represents the energetically favorable values of the critical current.

shown in Fig. 2.2a. In this section, we concentrate on the non-hysteretic dc SQUID in which the junctions are shunted with each a resistor R to remove the hysteresis.

In most practical applications, the dc SQUID is biased with a constant (dc) current $I_b > 2I_0$, hence the name dc SQUID. The bias current is distributed over the two junctions

$$I_b = I_1 + I_2 = I_0 \sin\phi_1 + I_0 \sin\phi_2 \,, \tag{2.10}$$

where ϕ_1 and ϕ_2 are the phase differences across the junctions. If a signal flux Φ_{sig} is applied to the dc SQUID, the bias current is redistributed in such a way that a superconducting screening current I_{scr} is generated which causes a screening flux

$$\Phi_{scr} = L_{sq} I_{scr} = L_{sq} \frac{I_2 - I_1}{2} \,. \tag{2.11}$$

This screening current is the result of the flux quantization condition, as was discussed in section 2.1.1. The single valuedness of the complex wave function Ψ requires that along an arbitrary closed path, the phase difference is $\Delta\varphi = \mathrm{n}2\pi$. Taking the phase differences across the junctions into account, this means that along a closed path through the superconducting SQUID ring and the Josephson junctions and enclosing a flux Φ, the phase difference can be written as

$$\Delta\varphi = 2\pi \frac{\Phi}{\Phi_0} + \phi_1 - \phi_2 = 2\pi \frac{\Phi_{sig} - \Phi_{scr}}{\Phi_0} + \phi_1 - \phi_2 = \mathrm{n}2\pi \,. \tag{2.12}$$

For simplicity, assume that the phase differences of the junctions can be neglected [9]. In the absence of any applied flux or if the signal flux equals $\mathrm{n}\Phi_0$, there is no circulating screening current and the bias current is distributed symmetrically over both junctions: $I_1 = I_2 = I_b/2$. Thus the critical current of the SQUID is just the sum of the critical currents of both junctions: $I_c(\mathrm{n}\Phi_0) = 2I_0$. If a signal flux $\Phi_{sig} < \Phi_0/2$ is applied, a screening current $I_{scr} = \Phi_{sig}/L_{sq}$ is generated. The screening current adds to the bias current flowing through junction 2 and subtracts from the

bias current flowing through junction 1. In this simplified model, the critical current of junction 2 is reached when $I_b/2 + I_{scr} = I_0$ and the critical current of the SQUID is reached when $I_b = 2I_0 - 2I_{scr}$. Consequently, the critical current of the SQUID is suppressed if $\Phi_{sig} \neq n\Phi_0$.

Figure 2.2b shows the I_c-Φ_{sig} characteristics, the so-called threshold curves, of a dc SQUID. In this case, the phase differences of the two junctions were taken into account. The underlying model that was used for the numerical calculation of the threshold curves is based on Eqs. (2.10) to (2.12). When the applied signal flux is increased from 0 to $\Phi_0/2$, the screening current increases and consequently the critical current of the SQUID decreases. As the flux exceeds $\Phi_0/2$, the SQUID switches from the n = 0 flux quantum state to the n = 1 state and the circulating current changes sign. As is represented by the gray region in Fig. 2.2b, the result is a periodic dependence of the critical current of a non-hysteretic dc SQUID on the applied flux with Φ_0 as the period. The modulation depth of the critical current is given by [10]

$$\Delta I_c = I_{c,max} - I_{c,min} \approx \frac{1}{1+\beta_L} 2I_0 \,. \tag{2.13}$$

This approximation is only valid as long as the screening parameter,

$$\beta_L = \frac{2I_0 L_{sq}}{\Phi_0} \,, \tag{2.14}$$

is about 1. In literature, this parameter is also denoted by β.

Since the dc SQUID consists of two Josephson junctions connected in parallel by a superconducting loop, the I-V characteristics of the dc SQUID look like that of a single junction, except for the fact that the critical current I_c of the SQUID can be modulated by the signal flux. In Fig. 2.3a, the I-V characteristics of the two

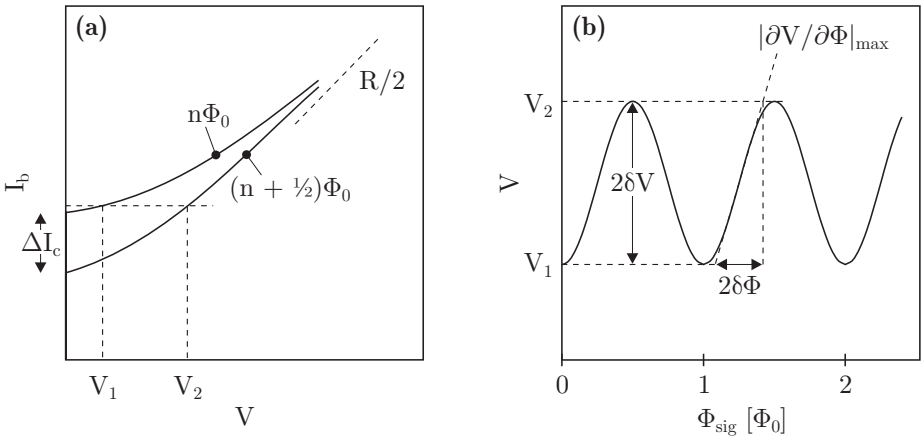

Fig. 2.3 (a) Schematic I-V characteristics of a non-hysteretic dc SQUID. For large currents, the usable voltage swing $2\delta V$ becomes zero and the SQUID shows ohmic behavior with a resistance $R/2$. **(b)** Corresponding V-Φ_{sig} characteristic of the dc SQUID biased with a constant current.

extreme cases are shown: At $\Phi_{sig} = n\Phi_0$ the critical current is maximum, $I_{c,max} = 2I_0$, and at $\Phi_{sig} = (n + ½)\Phi_0$, the minimum critical current, $I_{c,min}$, is reached. Because of the periodic dependence of the critical current on the signal flux, the voltage across a current-biased ($I_b > 2I_0$) non-hysteretic dc SQUID is also periodically dependent on the applied flux with Φ_0 as the period. The dc SQUID is thus a nonlinear flux-to-voltage converter. Figure 2.3b shows the V-Φ_{sig} characteristic of a non-hysteretic dc SQUID. The usable voltage swing, $2\delta V = V_2 - V_1$, is optimum for bias currents just above the maximum critical current of the SQUID. The maximum slope of the V-Φ_{sig} characteristic, the flux-to-voltage transfer, is estimated as [8]

$$\frac{\partial V}{\partial \Phi_{sig}} \approx \frac{2\beta_L}{1+\beta_L}\frac{R}{L_{sq}}\,. \tag{2.15}$$

For conventional resistively shunted low-T_c dc SQUIDs as discussed in this section, the flux-to-voltage transfer is of the order of 100 $\mu V/\Phi_0$ and $2\delta V \approx 30$ μV.

2.2.2 Noise in non-hysteretic dc SQUIDs

Non-hysteretic dc SQUIDs based on Nb/Al,AlO_x/Al/Nb Josephson tunnel junctions are often operated at a temperature $T = 4.2$ K in a ^{4}He bath cryostat. At this temperature, the main noise source is the Johnson noise,

$$S_I = \frac{4k_BT}{R}\,, \tag{2.16}$$

of the shunt resistors. Since in the dc SQUID two shunt resistors are connected in parallel by the SQUID loop, the Johnson noise currents introduce in-phase and out-of-phase components. The out-of-phase components generate a circulating current noise in the SQUID that induces noise into any input circuit coupled to it [11]. However, in most applications this effect is negligibly small compared to the effect of the in-phase components. The in-phase components cause a voltage noise at the output of a non-hysteretic dc SQUID with a spectral density given by [8]

$$S_V = \gamma 2 S_I R_{dyn}^2 \approx \gamma 2 k_B T R\,, \tag{2.17}$$

where the dynamic resistance R_{dyn} of the SQUID was approximated with $R/2$. The factor γ arises from the fact that Johnson noise generated at frequencies around the Josephson frequency f_J is mixed down to the measurement frequency by the Josephson oscillations and the inherent nonlinearity of the junctions. This factor cannot be obtained analytically, but simulations have shown that $\gamma \approx 8$ [8]. Using Eqs. (2.15) and (2.17), the flux noise spectral density can be calculated as

$$S_\Phi = \frac{S_V}{\left(\partial V/\partial \Phi_{sig}\right)^2} \approx \gamma \frac{2k_BTL_{sq}^2}{R}\left(\frac{1+\beta_L}{2\beta_L}\right)^2. \tag{2.18}$$

This equation is only valid for $\beta_L \approx 1$. At 4.2 K, the typical flux noise of a non-hysteretic low-T_c dc SQUID is of the order of $\sqrt{S_\Phi} = 1\ \mu\Phi_0/\sqrt{\text{Hz}}$.

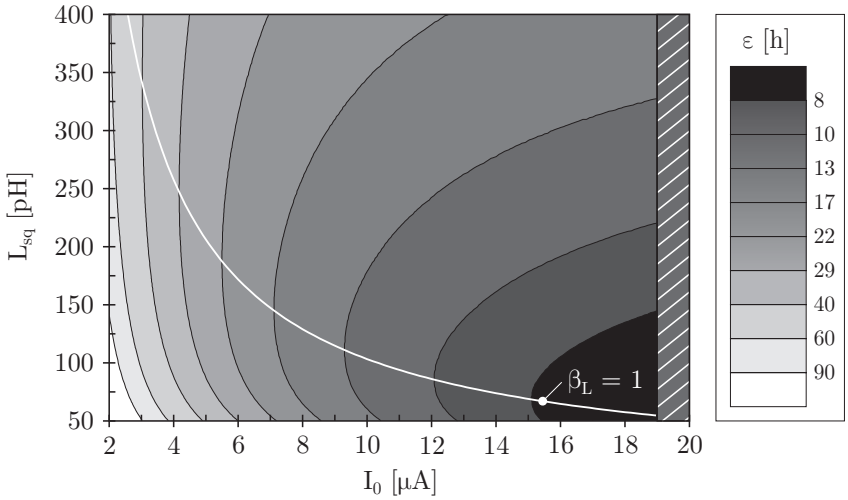

Fig. 2.4 Contour plot of the energy resolution of a dc SQUID as a function of the critical current of the junctions I_0 and the SQUID inductance L_{sq} for $T = 4.2$ K. Each junction is shunted with a resistor $R = 6\ \Omega$ and the junction capacitance is $C_j = 0.48$ pF, which corresponds to a junction area of about 4 x 4 μm^2. The shaded area on the right corresponds to a McCumber parameter $\beta_C > 1$, i.e. $I_0 > 19$ μA. The white line represents $\beta_L = 1$.

A convenient way to compare the sensitivity of different SQUIDs is in terms of the noise energy per unit bandwidth or the energy resolution[iii],

$$\varepsilon = \frac{S_\Phi}{2L_{sq}} \approx \gamma \frac{k_B T L_{sq}}{R} \left(\frac{1+\beta_L}{2\beta_L} \right)^2 . \tag{2.19}$$

According to Eq. (2.19), the energy resolution can be improved by, e.g., decreasing the SQUID inductance L_{sq} [12,13] or the operation temperature T [14,15,16]. Figure 2.4 shows a contour plot of the energy resolution of a resistively shunted dc SQUID at 4.2 K as a function of the critical current of the junctions I_0 and the SQUID inductance L_{sq}. The junction capacitance is $C_j = 0.48$ pF and each junction is shunted with a shunt resistor $R = 6\ \Omega$. The contour plot shows that for a fixed value of the critical current of the junctions, the optimum value of the screening parameter is $\beta_L = 1$. For optimized dc SQUIDs, β_L should thus be close to unity [8]. The energy resolution can also be improved by increasing the critical current of the junctions. In most practical applications however, the junction hysteresis has to be removed, which means that the critical current can only be increased as long as $\beta_C < 1$. For this typical example we find $I_0 < 19$ μA. As is discussed in section 6.1.1, the noise properties of a dc SQUID can also be improved by reducing the junction area [17].

[iii] In this thesis, only devices operating within the classical limit are discussed. However, at very low temperatures for example, zero point fluctuations, the quantum mechanical counter part of Johnson noise, impose a lower limit on the attainable energy resolution and Eqs. (2.16) to (2.19) are no longer valid.

In the discussion above, only the Johnson noise generated in the shunt resistors was considered. Johnson noise is white noise, which means that the spectral density is uniform. However, at low frequencies the noise spectral density of a practical dc SQUID has a 1/f character. Two important mechanisms for the 1/f noise in SQUIDs are critical current fluctuations and the motion of trapped flux lines. These mechanisms are not treated in this thesis but are discussed in, e.g., ref. [9].

2.2.3 The washer-type dc SQUID with tightly coupled input coil

Using a non-hysteretic dc SQUID, any physical quantity that can be converted to a magnetic flux can be measured with extreme sensitivity. In most applications, the quantity that is to be measured is converted to a current, which is passed through a nearby input coil that is coupled to the SQUID with high efficiency. The most effective coupling between the input coil and the SQUID is achieved in the washer-type dc SQUID with tightly coupled input coil proposed by Jaycox and Ketchen [18]. In this concept, a spiral multi-turn input coil is deposited on top of a thin-film SQUID in a square washer configuration, as is shown in Fig. 2.5.

The total SQUID inductance L_{sq} is composed of three contributions

$$L_{sq} = L_h + L_t + L_p \approx L_h + L_t \,. \tag{2.20}$$

Here, L_h is the hole inductance that is related to the square hole in the washer, L_t is the slit inductance and L_p is the parasitic inductance associated with the junction structure. The right-hand approximate expression in Eq. (2.20) is justified by the fact that, generally, $L_p \ll L_h + L_t$. The hole inductance is given by [18]

$$L_h = 1.25\mu_0 d \,, \tag{2.21}$$

where $\mu_0 = 4\pi{\cdot}10^{-7}$ H/m represents the permeability of vacuum. This equation is only valid as long as the outer dimension of the SQUID washer is much larger than the hole width d. Moreover, the thickness of the SQUID washer should be large

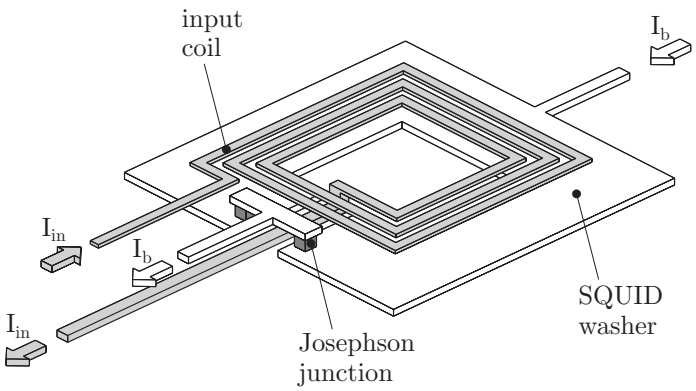

Fig. 2.5 Washer-type dc SQUID with tightly coupled input coil. The input coil is separated from the SQUID with an insulating layer. For simplicity, the shunt resistors are not shown. The return line of the input coil lies in the slit of the washer.

enough, i.e. at least $2\lambda_L$, to ensure a complete Meissner effect. The return line of the input coil lies generally in the slit of the washer. The result is a double-slit structure with an inductance per unit length of the order of 0.4 pH/μm [19]. The inductance of the spiral multi-turn input coil that is deposited on top of the SQUID washer is roughly estimated as [18]

$$L_{in} = n^2 L_h + L_s \,, \tag{2.22}$$

where n is the number of turns of the input coil and L_s is the stripline inductance of the coil. Generally, the contribution of the stripline is negligible. The mutual inductance between the input coil and the SQUID inductance is given by

$$M_{in} = k\sqrt{L_{in} L_{sq}} \,, \tag{2.23}$$

where k is the coupling coefficient, which can have practical values close to unity. The measured SQUID inductances are generally in good agreement with the predicted values. However, the measured parameters of the input coil are often not accurately estimated by Eqs. (2.22) and (2.23). For more accurate estimations, e.g., the 3D numerical inductance extraction software FastHenry [20] can be used. Also more accurate analytical working formulas for specific SQUID layouts are available. Both topics are discussed in section 5.4.1.

In washer-type dc SQUIDs coupled to many-turn input coils, the presence of nonlinear regions in the I-V characteristics can be a serious problem. At these nonlinear regions, the V-Φ_{sig} characteristics and the noise properties of the coupled SQUIDs are considerably degraded compared to uncoupled SQUIDs. It is believed that the degradation of coupled SQUIDs is caused by resonance of the input coil and therefore several methods have been developed to damp the resonance using external resistors, e.g., in parallel with the input coil [21,22] or between the individual turns of the coil [23,24]. Various experiments have shown the positive effect of these damping schemes on the characteristics of coupled SQUIDs.

As was discussed in refs. [25], [26] and [27], taking only the input coil resonance into account cannot explain the degradation of the V-Φ_{sig} characteristics and a combination of the resonance with a feedback path from the SQUID output to the input coil is thought to be the underlying mechanism. In this model, the input coil resonance is pumped by Johnson noise generated in the shunt resistors and occurs at frequencies determined by the resonant circuit formed by the input coil inductance and the capacitance between the input coil and the SQUID washer. As a consequence of the input coil resonance, the voltage V across the SQUID has a large rf component V_{rf}. When the voltage V_{rf} is able to drive a current through the input coil, e.g. due to capacitive coupling at rf frequencies, a 'feedback' flux is generated in the SQUID. This capacitive feedback is the most likely mechanism for the irregularities in the characteristics of coupled SQUIDs [26,27]. Using resistive damping, the quality factor Q of the resonances can be lowered and the effects on the SQUID characteristics can be reduced. In the SQUID designs described in the remainder of this thesis, the SQUID washers are shunted with a damping resistor R_w to avoid L-C resonances between the SQUID inductance and capacitances of the junctions [28,29,30] and the input coil is shunted with an external R_{in}-C_{in} circuit.

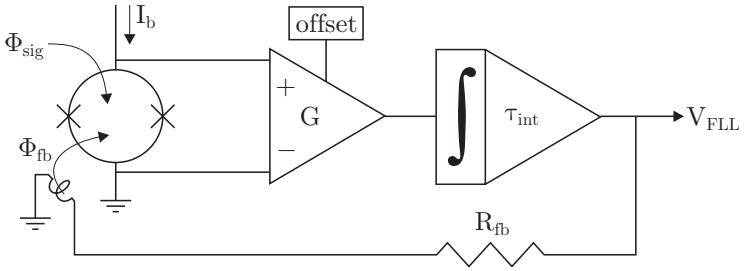

Fig. 2.6 Scheme of the flux locked loop (FLL) configuration for the readout of a dc SQUID. The SQUID is operating at cryogenic temperatures and the FLL circuitry is conventionally implemented using room temperature electronics.

2.2.4 The flux locked loop configuration

As was discussed in section 2.2.1, the voltage across a current-biased non-hysteretic dc SQUID is periodically dependent on the applied signal flux Φ_{sig}. In most cases however, this nonlinear behavior is unwanted and the SQUID is operated in a feedback loop for the magnetic flux to linearize its response [31]. In this so-called flux locked loop (FLL), see Fig. 2.6, the SQUID is operated as a null-detector of magnetic flux and the voltage V_{FLL} at the output of the FLL is linearly dependent on the applied flux. Conventionally, the voltage across the SQUID is amplified and integrated at room temperature and fed back as a feedback flux Φ_{fb} to the SQUID in order to keep the total flux $\Phi_{sig} + \Phi_{fb}$ in the SQUID constant. The transfer function $\partial V_{FLL}/\partial\Phi_{sig}$ of the system shown in Fig. 2.6 is given by

$$\frac{\partial V_{FLL}}{\partial \Phi_{sig}} = \frac{V_\Phi G\left(1/j\omega\tau_{int}\right)}{1 + V_\Phi G\left(1/j\omega\tau_{int}\right)\left(M_{fb}/R_{fb}\right)} = \frac{R_{fb}}{M_{fb}}\frac{1}{j\omega\tau + 1}, \quad \tau = \frac{\tau_{int}R_{fb}}{GM_{fb}V_\Phi}. \quad (2.24)$$

In this equation, $V_\Phi = \partial V/\partial\Phi_{sig}$, G represents the gain of the room temperature dc preamplifier, R_{fb} is the feedback resistance, M_{fb} represents the mutual inductance between the feedback coil and the SQUID inductance and τ_{int} is the time constant of the integrator. Hence, the maximum bandwidth of the dc SQUID operated in FLL is

$$f_{max} = \frac{1}{2\pi\tau} = \frac{GM_{fb}}{2\pi\tau_{int}R_{fb}}\frac{\partial V}{\partial\Phi_{sig}}. \quad (2.25)$$

In Eqs. (2.24) and (2.25), it is assumed that all components of the FLL are ideal: The bandwidth of the preamplifier is infinite, the integrator is an ideal one-pole integrator and the dead-time of the feedback loop is zero. In practice however, the maximum attainable bandwidth in FLL is limited by the finite bandwidth of the FLL electronics, noise and dead-time in the feedback loop.

An important parameter of a SQUID system operating in FLL is the maximum flux slew rate. The maximum flux slew rate is the maximum rate at which the signal flux can be changed without causing the FLL to unlock and is given by [32]

$$\frac{\partial \Phi_{sig}}{\partial t} = 2\pi\delta\Phi f_{max} = \frac{\delta V G M_{fb}}{\tau_{int} R_{fb}}. \tag{2.26}$$

As can be concluded from Eq. (2.26), the maximum flux slew rate is frequency independent and increases linearly with the bandwidth in FLL and the linear flux range $2\delta\Phi = 2\delta V/(\partial V/\partial \Phi_{sig})$ of the SQUID.

In practical systems, the configuration shown in Fig. 2.6 leads to preamplifier limitation of the overall system sensitivity, since the output voltage noise of a dc SQUID is much smaller than the input voltage noise of the dc preamplifier. As was discussed in sections 2.2.1 and 2.2.2, the flux-to-voltage transfer of a conventional resistively shunted dc SQUID operating at 4.2 K is of the order of 100 $\mu V/\Phi_0$ and the white flux noise level is typically around 1 $\mu\Phi_0/\sqrt{Hz}$. This means that the typical output voltage noise of a dc SQUID is 0.1 $nV/\sqrt{Hz}$, which is about one order of magnitude smaller than the input voltage noise of a low-noise room temperature dc preamplifier.

In order to solve the matching problem, ac flux modulation has been used successfully for many years. In an ac flux modulated FLL system, a modulating flux with a peak-to-peak amplitude of $\Phi_0/2$ and a frequency typically between 100 and 500 kHz is applied to the SQUID. The resulting ac voltage across the SQUID is increased by a (resonant) step-up transformer or a resonant L-C circuit and lock-in detected at room temperature [33,34]. Unfortunately, the measurement bandwidth is limited by the modulation frequency, although wideband (but complex) ac flux modulated systems have been successfully operated at a modulation frequency of 16 MHz and with usable bandwidths up to 5 MHz and maximum flux slew rates as high as 10^6 Φ_0/s [35,36].

2.3 Second generation dc SQUIDs

Partly motivated by the need to simplify the SQUID readout electronics of, e.g., multichannel biomagnetic systems, second generation dc SQUIDs with a large flux-to-voltage transfer have been developed. The flux-to-voltage transfer of these SQUIDs is typically around 1 mV/Φ_0, which is large enough to allow a simple direct voltage readout mode with large bandwidths and high slew rates. Various concepts of second generation dc SQUIDs have been developed, such as SQUIDs with additional positive feedback (APF) [37,38], asymmetric dc SQUIDs [39,40], series SQUID arrays [41,42], double relaxation oscillation SQUIDs (DROSs) [43,44] and two-stage SQUID systems [14,45,46]. For example, using APF SQUIDs, a bandwidth of 15 MHz together with a slew rate of $2{\cdot}10^6$ Φ_0/s has been reported [47]. In this section, the latter three second generation dc SQUIDs are briefly discussed.

2.3.1 Series SQUID arrays

The usable voltage swing and the flux-to-voltage transfer of a single dc SQUID can be increased considerably by connecting N identical SQUIDs in series. As a result, the usable voltage swing is increased by a factor N and also, ideally, the flux-to-voltage transfer increases linearly with the number of SQUIDs. The spectral density

of the overall flux noise S_Φ however, is increased by a factor N. Another important practical limitation of the series SQUID array is that all SQUIDs should be modulated coherently, which means that the properties of all SQUIDs, e.g. the mutual inductance between the input coil and each SQUID, should be the same and that there is no random flux offset between the SQUIDs. Trapped flux and parasitic coupling for example, affect the required coherence and can cause severe distortions of the characteristics of series SQUID arrays, which limits the practical versatility of these systems [41,48,49]. The main advantage of a series SQUID array is that its linear flux range is not decreased compared to that of a single dc SQUID. In almost every other second generation dc SQUID, the linear flux range is smaller than that of a conventional resistively shunted dc SQUID.

Welty *et al.* [41] have developed a series SQUID array based on 100 SQUIDs. For their systems, a large voltage swing of $2\delta V \approx 2.5$ mV, i.e. 100 times larger than that of the single dc SQUIDs, and a flux-to-voltage transfer of $\partial V/\partial\Phi_{sig} \approx 7\ \mathrm{mV}/\Phi_0$ were measured. A coupled white energy resolution of $\varepsilon_{coupl} = \varepsilon/k^2 = 56\ h$ [42] and intrinsic bandwidths up to 120 MHz [24] have been reported for similar devices. Series SQUID arrays based on 100 and 200 SQUIDs as developed by Welty *et al.* are commercially available from HYPRES [50].

2.3.2 Double relaxation oscillation SQUIDs

In 1968, Vernon and Pedersen found that when a hysteretic Josephson junction is shunted with an external inductor L_{sh} and a resistor R_{sh}, under certain conditions continuous oscillations appear [51], as is shown in Fig. 2.7. The dynamic behavior of the circuit shown in Fig. 2.7a is given by

$$\begin{aligned} I_b &= I_1 + I_2, \\ V &= L_{sh}\frac{\partial I_2}{\partial t} + R_{sh}I_2. \end{aligned} \tag{2.27}$$

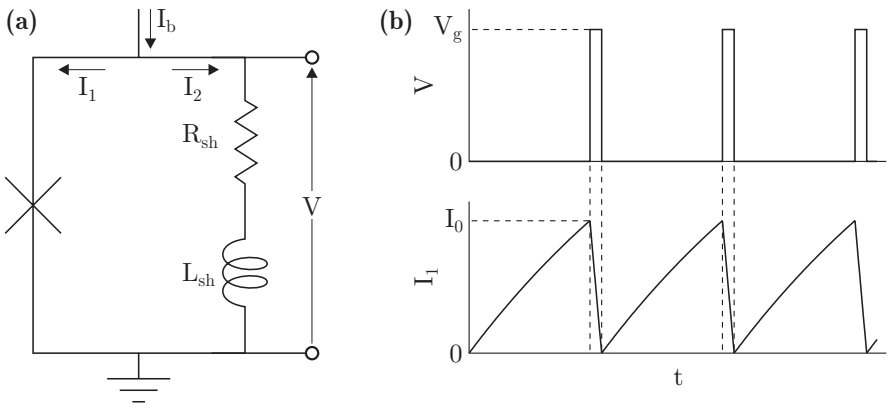

Fig. 2.7 (a) Scheme of a hysteretic Josephson junction shunted with an external inductor L_{sh} and a resistor R_{sh}. **(b)** I_1-t and V-t characteristics of the resulting relaxation oscillations that are generated in the shunted junction.

Here, V is determined by the hysteretic I-V characteristic of the junction. If the bias current I_b is larger than the critical current I_0 of the Josephson junction, relaxation oscillations can occur if $I_b R_{sh} < V_g$ [51]. In a simple model, the voltage across the junction is either zero or equal to the gap voltage V_g. Assume that at $t = 0$ the current I_1 through the Josephson junction is zero, i.e. the junction is in the superconducting state and $V = 0$. According to Eq. (2.27), the current I_2 decays exponentially with a time constant L_{sh}/R_{sh}. Consequently, the current I_1 increases until the critical current of the junction is reached and the junction switches to the voltage state. Hence, a voltage $V = V_g > I_b R_{sh}$ appears across the L_{sh}-R_{sh} shunt and the current I_2 increases and thus the current through the junction decreases. When the current through the junction is decreased to zero, the junction switches back to the superconducting state and the whole process starts again. As a result of these relaxation oscillations, voltage pulses with an amplitude V_g and a frequency f_{RO} are generated across the junction. The relaxation oscillation frequency can be roughly estimated as

$$f_{RO} \approx \frac{R_{sh}}{L_{sh}}, \tag{2.28}$$

although this frequency is also dependent on, amongst other parameters, the bias current I_b and the critical current I_0 of the junction. In this thesis, the discussion of the relaxation oscillations is restricted to the simple model described above. A thorough discussion on this subject can be found in, e.g., refs. [52] and [53].

The operation principle of a double relaxation oscillation SQUID (DROS) is based on relaxation oscillations. The DROS consists of two hysteretic dc SQUIDs, the signal SQUID and the reference SQUID, which are connected in series and shunted with an inductor L_{sh} and a resistor R_{sh}, as is shown in Fig. 2.8a. If an appropriate bias current I_b is applied to the DROS, relaxation oscillations are generated in the same way as discussed above. However, only the SQUID with the smallest critical current participates in the relaxation oscillations. This means that

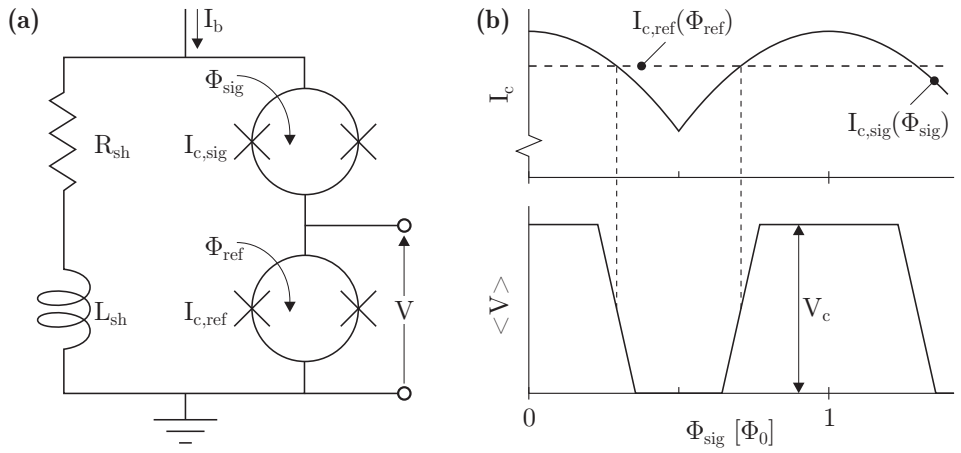

Fig. 2.8 (a) Scheme of a double relaxation oscillation SQUID (DROS). **(b)** I_c-Φ_{sig} graphs of the signal SQUID and the reference SQUID and the $<V>$- Φ_{sig} characteristic of a DROS.

only this SQUID switches back and forth between the zero-voltage state and the voltage state, whereas the other SQUID always remains in the zero-voltage state, i.e. the DROS behaves as a critical current comparator.

The DROS is operated as a flux-to-voltage converter by applying the signal flux Φ_{sig} to the signal SQUID and applying a constant reference flux Φ_{ref} to the reference SQUID. The signal flux modulates the critical current of the signal SQUID $I_{c,sig}(\Phi_{sig})$ and the reference flux is used to tune the critical current of the reference SQUID $I_{c,ref}$, such that it is in the middle of the critical current modulation range of the signal SQUID, see Fig. 2.8b. The output voltage of the DROS is the voltage across the reference SQUID. In a conventional readout scheme, the readout is performed at room temperature using FLL electronics with a bandwidth much smaller than the relaxation oscillation frequency, typically around $f_{RO} \approx 1$ GHz, such that only the time-averaged dc component $<V>$ of the voltage pulses is measured. This voltage is zero when $I_{c,sig}(\Phi_{sig}) < I_{c,ref}$ and when $I_{c,sig}(\Phi_{sig}) > I_{c,ref}$, the time-averaged dc component is $<V> = V_c$. Consequently, the $<V>$-Φ_{sig} characteristic of a DROS shows a large flux-to-voltage transfer at the points where $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$, as is shown in the lower trace of Fig. 2.8b.

The flux-to-voltage transfer of a DROS is typically of the order of 1 mV/Φ_0 and the usable voltage swing is around $2\delta V \approx 100$ μV. This means that the linear flux range is of the order of 0.1 Φ_0. In FLL, white energy resolutions of $\varepsilon = 34\ h$ for uncoupled DROSs [43] and $\varepsilon = 150\ h$ ($\varepsilon_{coupl} = 300\ h$) for DROSs with integrated input coils [54] have been reported. In chapter 5, a digital SQUID based on a DROS, the so-called Smart DROS, is thoroughly discussed and also the operation principle of the DROS is treated in more detail.

2.3.3 Two-stage SQUID systems

As was discussed, a SQUID can be used to measure any physical quantity that can be converted to a magnetic flux with extreme sensitivity. This characteristic is exploited in the two-stage SQUID system in which the output signal of a sensor

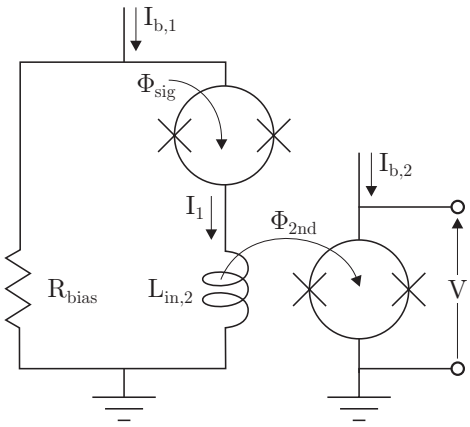

Fig. 2.9 Scheme of a two-stage SQUID system. In this case, the second stage is represented by a conventional dc SQUID, but also a second generation dc SQUID can be used.

SQUID is increased by using a second SQUID as a low-noise cryogenic preamplifier, as is schematically shown in Fig. 2.9. Because of its excellent noise properties, a conventional resistively shunted dc SQUID is generally used as the sensor SQUID and in principle any kind of SQUID, e.g. another second generation dc SQUID, can be used as the second stage. The first two-stage SQUID systems were based on a conventional dc SQUID as the second stage [14,55]. From HYPRES for example, two-stage SQUID systems based on series SQUID arrays as the second stage are available [50]. These SQUID systems were originally developed by Welty *et al.* [45]. At the University of Twente, we have developed two-stage SQUID systems with a DROS as the second stage [46,56].

In order to couple the sensor SQUID to the second stage, the sensor SQUID is biased at a constant voltage V_{bias} using a small bias resistor R_{bias} in parallel to the SQUID. In this voltage bias mode, the SQUID acts as a flux-to-current converter, i.e. the current through the SQUID I_1 is modulated by the signal flux Φ_{sig}. The current I_1 is fed through the input coil of the second stage $L_{in,2}$, thereby introducing a flux gain $G_\Phi = \partial\Phi_{2nd}/\partial\Phi_{sig}$. Here, $\Phi_{2nd} = M_{in,2}I_1$ is the flux coupled to the second stage and $M_{in,2}$ is the mutual inductance between the second stage and its input coil. The flux gain should be sufficiently large, such that the amplified flux noise of the sensor SQUID is larger than the noise contributions of the second stage and the room temperature readout electronics. Hence, in a well-designed two-stage SQUID system, the overall system noise is determined by the sensor SQUID.

For two-stage SQUID systems based on series SQUID arrays, a large flux-to-voltage transfer of $\partial V/\partial\Phi_{sig} = 20\ \mathrm{mV}/\Phi_0$ and a white energy resolution in open loop of $\varepsilon = 30\ h$ ($\varepsilon_{coupl} = 310\ h$) have been reported [45]. The intrinsic bandwidth of these devices was limited to 390 kHz[iv], although bandwidths up to 2 MHz have been reported for similar devices [57]. The voltage swing can be as large as 10 mV [58]. For two-stage SQUID systems with a DROS as the second stage, a flux-to-voltage transfer of 3.6 mV/Φ_0 has been reported [46]. The white energy resolution measured in FLL was $\varepsilon = 27\ h$ ($\varepsilon_{coupl} = 36\ h$) and the FLL bandwidth can be as large as 2.5 MHz [56]. In chapter 4, the two-stage SQUID system is discussed in more detail.

2.4 Digital SQUIDs

In a two-stage SQUID system, the sensor SQUID can be integrated together with a low-noise cryogenic preamplifier, i.e. the second stage SQUID, on one chip. In the digital SQUIDs, the integration of the SQUID and the readout electronics goes one step further. In these systems, the SQUID and the complete FLL circuitry are integrated on one single chip. The key element of these SQUID systems is a digital circuit that supplies the feedback flux to the SQUID. Although also digital room temperature feedback electronics has been developed [59], only the single-chip digital SQUID is discussed here.

[iv] As is discussed in section 4.1.3, the inductance of the input coil of the second stage $L_{in,2}$ and the resistances R_{dyn} and R_{bias} form a first-order low-pass filter which limits the intrinsic bandwidth of two-stage SQUID systems. Here, R_{dyn} is the dynamic resistance of the sensor SQUID.

2.4.1 Digital SQUIDs based on rapid single flux quantum logic

Rapid single flux quantum (RSFQ) logic [60] is the fastest digital technology available. For representing binary values in RSFQ logic, very short (picosecond) voltage pulses, so-called single flux quantum (SFQ) pulses, are used. This concept allows clock frequencies in the sub-THz range. For example, the highest speed of an RSFQ device ever measured is 770 GHz [61]. Besides speed, an important advantage of RSFQ compared to CMOS is the extremely low power consumption, i.e. close to 10^{-18} J/bit, which is 4 to 5 orders of magnitude lower than for advanced CMOS [62]. This opens new possibilities for a wide range of applications, such as a digital SQUID.

A digital SQUID implemented in RSFQ was originally suggested by Likharev *et al.* [60,63]. An all-RSFQ SQUID potentially allows to achieve an overall system noise level close to the intrinsic SQUID noise level, a flux slew rate as high as ~10^9 Φ_0/s and a virtually unlimited dynamic range. However, the layout of such an RSFQ SQUID is complex and requires thousands of Josephson junctions. This large number of junctions is mainly used for implementing a digital counter/filter, which is required to reduce the output signal frequency to a value low enough to allow further data processing by semiconductor electronics. Because of the complexity, no operating RSFQ SQUID has been fabricated yet. Nevertheless, as the low-T_c fabrication technology is improving continuously, the first all-RSFQ SQUIDs are expected in the near future [64].

2.4.2 Digital SQUIDs based on the Fujitsu single-chip SQUID

Contrary to all-RSFQ SQUIDs, several digital SQUIDs based on the concept that was developed at the Fujitsu laboratories by Fujimaki *et al.* [65,66] have been operated successfully [67,68,69,70]. The key elements of the Fujitsu single-chip (digital)

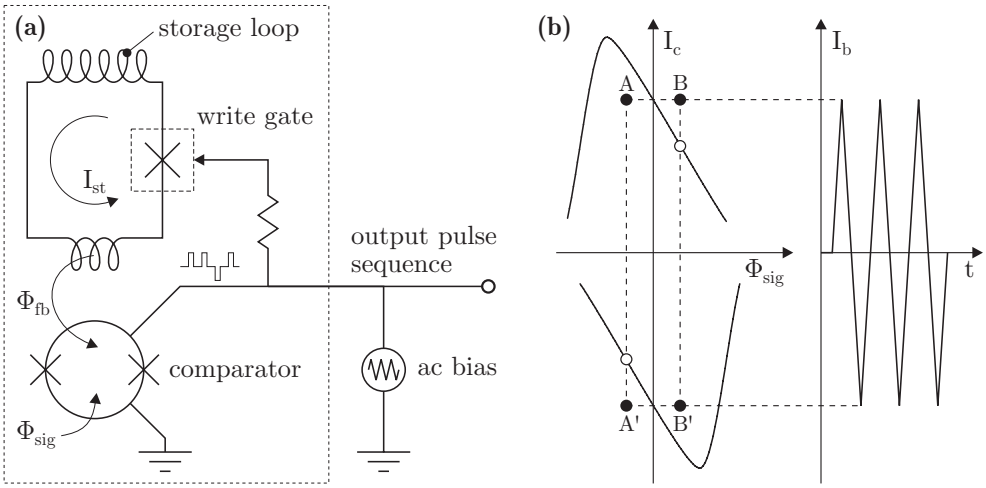

Fig. 2.10 (a) Scheme of the single-chip SQUID developed by Fujimaki *et al.* The elements inside the large dotted block are integrated on one chip. **(b)** Threshold characteristic and the time-dependent bias current of the comparator.

SQUID are a comparator and an up-down counter that supplies the feedback flux, as is shown in Fig. 2.10a. The up-down counter has the role of the integrator in the conventional FLL and consists of a superconducting storage loop with a dc SQUID as a flux-quanta write gate. Although in the RSFQ SQUID the latching logic cells, e.g. the comparator, are replaced by RSFQ cells, the operation principle of an all-RSFQ SQUID is basically similar to that of the Fujitsu single-chip SQUID.

The latching comparator consists of a hysteretic dc SQUID with asymmetric threshold characteristics, as is shown in Fig. 2.10b. The asymmetry is achieved by asymmetric current injection, i.e. the bias current is applied to one of the junctions instead of to the center tap of the SQUID inductance. The comparator is biased with a bipolar alternating clock current with a frequency f_c and an amplitude equal to the critical current of the comparator when no flux is applied. If the bias current exceeds the critical current of the comparator, a voltage pulse is generated. As a consequence of the asymmetric threshold characteristics, the comparator produces negative voltage pulses for $\Phi_{sig} < 0$ and positive voltage pulses for $\Phi_{sig} > 0$, as is indicated by the lines A-A' and B-B' in Fig. 2.10b. When $\Phi_{sig} = 0$, the probabilities of producing a negative or a positive voltage pulse are both 50 %.

The output voltage pulses of the comparator are coupled to the write-gate of the up-down counter. The positive and negative pulses increase and respectively decrease the quantized flux in the storage loop in steps of Φ_0. The flux in the storage loop generates a circulating current with a quantization unit of $\delta I_{st} = \Phi_0 / L_{st}$, where L_{st} is the inductance of the storage loop. The circulating current flows through a feedback coil and supplies the quantized feedback flux Φ_{fb} to the comparator. The quantization unit of the feedback flux is given by

$$\delta\Phi_{fb} = M_{fb}\,\delta I_{st} = \frac{M_{fb}}{L_{st}}\Phi_0\,, \tag{2.29}$$

where M_{fb} is the mutual inductance between the feedback coil and the comparator. The maximum flux slew rate of a digital SQUID depends on the clock frequency and the quantization unit of the feedback flux

$$\frac{\partial\Phi_{sig}}{\partial t} = \delta\Phi_{fb} f_c\,. \tag{2.30}$$

Fujimaki *et al.* reported on a single-chip SQUID operating at a clock frequency of 10 MHz and with a flux noise level of $\sqrt{S_\Phi} = 6.2\ \mu\Phi_0/\sqrt{\text{Hz}}$ ($\varepsilon = 3000\ h$) [66]. The measured flux slew rate, 170 Φ_0/s, was limited by the small quantization unit of the feedback flux, $\delta\Phi_{fb} = 17\ \mu\Phi_0$. An array of 8 of these chips was operated with a Josephson multiplexer at a multiplexer clock frequency of 120 MHz [71]. HYPRES demonstrated high-speed operation of a single-chip SQUID with a clock frequency of 500 MHz [67] and with a flux slew rate of $3.5{\cdot}10^4\ \Phi_0$/s [68]. The design of this single-chip SQUID was similar to that of the Fujitsu single-chip SQUID [72].

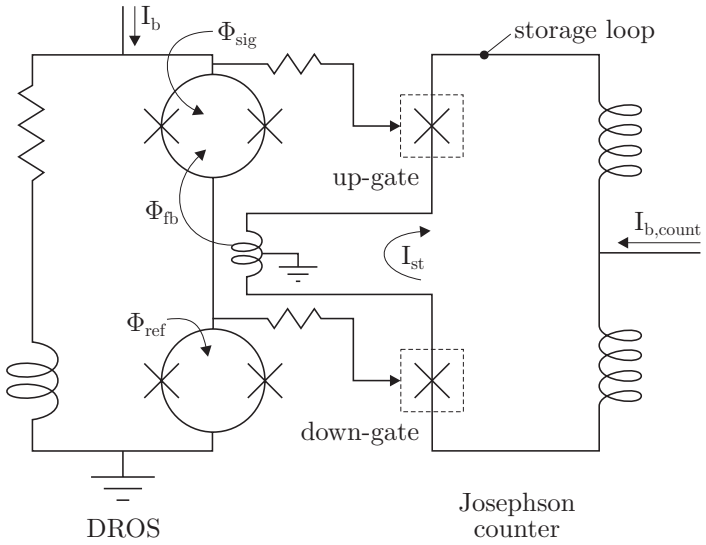

Fig. 2.11 Simplified scheme of the Smart DROS. The DROS and the Josephson counter are integrated on one chip. The counter consists of a superconducting storage loop with two dc SQUIDs as the up-gate and down-gate.

2.4.3 The Smart DROS

As was discussed in section 2.3.2, the readout of a DROS is generally performed at room temperature using FLL electronics with a bandwidth much smaller than the relaxation oscillation frequency, such that only the time-averaged dc component $<V>$ of the voltage pulses is measured. However, the pulsed output of the DROS is particularly suited for digital readout.

At the University of Twente, Van Duuren *et al.* developed the Smart DROS [73], a digital SQUID based on a DROS, as is schematically shown in Fig. 2.11. The key elements of the Smart DROS are a DROS and a superconducting up-down counter, the so-called Josephson counter. The Josephson counter is based on the counters of the Fujitsu and the HYPRES single-chip SQUIDs and consists of a storage loop with two resistively shunted non-hysteretic dc SQUIDs as write gates, i.e. the up-gate and the down-gate. The up-gate is connected to the signal SQUID and the down-gate is connected to the reference SQUID of the DROS. Consequently, a voltage pulse across the signal SQUID increases the quantized flux in the storage loop in steps of Φ_0 and a voltage pulse across the reference SQUID decreases the flux. The circulating current I_{st} flows through the feedback coil of the DROS and generates a feedback flux $\Phi_{fb} = M_{fb}I_{st}$ in the signal SQUID, with M_{fb} the mutual inductance between the feedback coil and the signal SQUID of the DROS.

The feedback loop automatically locks the Smart DROS into the dynamic equilibrium where both the signal SQUID and the reference SQUID have a switching probability of 50 %, i.e. the point where $I_c(\Phi_{sig}) = I_{c,ref}$. If the system is forced out of its equilibrium by changing the signal flux, one of the SQUIDs starts generating voltage pulses and the feedback flux is changed by one quantization unit

per relaxation oscillation cycle, until a new dynamic equilibrium has been reached. The quantization unit of the Smart DROS is given by Eq. (2.29) and the maximum flux slew rate is given by Eq. (2.30), substituting the relaxation oscillation frequency f_{RO} instead of f_c.

The main difference between the Smart DROS and Fujitsu single-chip SQUID is that the relaxation oscillations of the DROS are used as an on-chip clock signal, such that no external clock is required. This is an important advantage, since the noise characteristics of the single-chip SQUIDs based on the Fujitsu concept are very sensitive to deviations from the optimum comparator clock amplitude [69]. Moreover, an on-chip clock enables smooth operation at high clock frequencies, which results in better sensitivity, a larger bandwidth and a higher slew rate.

Van Duuren *et al.* demonstrated a prototype Smart DROS operating at a relaxation oscillation frequency of $f_{RO} = 100$ MHz [73]. The white energy resolution was $\varepsilon = 1150\ h$, after subtraction of the noise of the readout circuitry, and the maximum flux slew rate was limited to $2{\cdot}10^4\ \Phi_0$/s by the small quantization unit of the feedback flux. However, by optimizing the design of the Smart DROS[v], much higher slew rates can be attained [74,75]. For an optimized Smart DROS based on a relaxation oscillation frequency of 100 MHz, a maximum flux slew rate of $5{\cdot}10^6\ \Phi_0$/s has been achieved, as is discussed in detail in chapter 5 of this thesis. By increasing the relaxation oscillation frequency to a few GHz, the flux slew rate can in principle be increased up to $10^8\ \Phi_0$/s [76]. This is discussed thoroughly in chapter 6.

2.5 SQUIDs and their applications

As was discussed in the previous sections, by using a SQUID any physical quantity that can be converted to a magnetic flux can be measured with extreme sensitivity. The operation principles of three different types of SQUID systems were discussed: ac flux modulated SQUID systems based on resistively shunted conventional dc SQUIDs, second generation dc SQUIDs with direct voltage readout and single-chip digital SQUIDs. In this section, some applications of the different SQUID systems are briefly discussed. The aim of this section is not to give an overview of all SQUID applications, but to point out that each application requires its own SQUID system. Roughly, modulated SQUID systems are particularly suited for low to intermediate frequency applications, second generation dc SQUIDs for intermediate to high frequencies and the extremely high slew rates and large measurement bandwidths of digital SQUIDs are required for high-speed applications.

2.5.1 Modulated SQUID systems

Using ac flux modulation together with a step-up transformer or a resonant *L-C* circuit, the voltage across the SQUID can be increased, such that the matching problem between the SQUID and the room temperature electronics can be solved. An additional advantage of using ac flux modulation is that some of the 1/f noise

[v] The operation principle and the optimization of the Smart DROS is discussed in detail in chapter 5.

contributions can be eliminated. First of all, by using ac flux modulation the signal spectrum is shifted towards the sidebands of the modulation frequency, such that the 1/f noise contribution of the room temperature preamplifier can be eliminated. Secondly, ac flux modulation suppresses the in-phase components of the critical current fluctuations [9]. Various alternate modulation schemes, e.g. bias current reversal, have been developed to further reduce the 1/f noise level. The principles of ac flux modulation and bias current reversal are discussed in, e.g., refs. [9] and [77].

The measurement bandwidth of modulated SQUID systems is limited by the modulation frequency, which is generally in the range of 100 to 500 kHz. Moreover, possible crosstalk between the step-up transformers at cryogenic temperatures and the SQUIDs of adjacent channels in multichannel systems and the complexity of the readout electronics generally limit the application of flux modulation to systems operating at low to moderate frequencies and with a small number of channels. On the other hand, the ability to suppress the 1/f noise level considerably makes modulated SQUID systems the systems of choice for low frequency applications. For example, magneto-encephalography (MEG), magneto-cardiography (MCG) [78] and the cryogenic current comparator (CCC) [79] require good resolution at frequencies down to 1 Hz or less.

2.5.2 Second generation dc SQUIDs

Using second generation dc SQUIDs in direct voltage readout mode, it is relatively easy to achieve a large system bandwidth, since no ac (flux) modulation is required. Compared to flux modulated systems, an advantage of using direct voltage readout is that the SQUID can be operated at one well-defined point of operation in the V-Φ_{sig} characteristics, where the noise is very low. Using ac flux modulation, a modulating flux with a peak-to-peak amplitude of $\Phi_0/2$ is applied to the SQUID and the noise at the output is a measure of the averaged noise over this portion of the SQUID dynamics. As a result, the white noise level of ac flux modulated SQUID systems is generally larger than the white noise level of well-designed two-stage SQUID systems, although the difference can be quite small.

The main disadvantage of omitting modulation schemes is that the 1/f noise is not suppressed, which means that the 1/f noise level of second generation dc SQUIDs may be larger than that of ac modulated SQUID systems. Therefore, second generation dc SQUIDs are generally used for intermediate to high frequency applications. For example, two-stage SQUID systems can be applied for the readout of gravitational wave detectors operating at frequencies around a few kHz [80,81]. SQUID systems based on additional positive feedback (APF) have been successfully used for applications like nuclear magnetic resonance (NMR) up to several MHz [82] and broadband picovoltmeters [83].

The relatively high slew rates and large system bandwidths that can and have been achieved using second generation dc SQUIDs are important if not essential for the readout of cryogenic particle detectors [56]. Series SQUID arrays and two-stage SQUID systems for example, are used for the readout of X-ray detectors based on microcalorimeters [84] and superconducting tunnel junctions (STJs) [57]. The high slew rate is also important if one wants to reduce the shielding requirements, e.g.,

for applications in unshielded environments, such as geophysical measurements to investigate the shallow subsoil of the earth [85] or for non-destructive evaluation for detection of corrosion and cracks in metals [86,87].

2.5.3 Digital SQUIDs

By integrating the SQUID and the FLL circuitry on one chip, as is done for the single-chip digital SQUID, the dead-time in the feedback loop can be reduced and thus the maximum attainable bandwidth and the slew rate can be increased compared to analogue SQUIDs. As was discussed above, the output of a single-chip digital SQUID consists of a voltage pulse sequence representing the digitized (over-sampled) time derivative of the feedback flux. The pulses may be digitally integrated (counted) and low-pass filtered to reconstruct the signal that was measured by the digital SQUID. If the clock frequency f_c is higher than the Nyquist frequency for a given bandwidth, the signal is over-sampled and the noise can be improved by averaging the output of the digital SQUID [88]. Using digital SQUIDs, in principle SQUID systems with a low noise level and an extremely high slew rate and large bandwidth can be achieved. Although the first single-chip SQUIDs have been operated successfully, they have not been tested in practical applications yet.

The potential for extremely high slew rates opens new possibilities for the application of digital SQUIDs in unshielded environments, e.g. digital SQUIDs will relax the design constraints of MEG systems, where shielding forms a significant part of the total costs. The high slew rate is also very attractive for the readout of cryogenic particle detectors, as is discussed in chapter 3. An additional advantage of the single-chip SQUID using a comparator biased with a bipolar clock current is that the bipolar clock acts like a bias current reversal scheme for standard dc SQUIDs, which effectively suppresses the out-of-phase components of the critical current fluctuations [66,77]. This means that the digital SQUID might also be suited for low frequency applications.

It has been demonstrated that digital SQUIDs can be multiplexed at cryogenic temperatures without breaking the feedback loop [71]. Several digital SQUIDs may even be integrated with a multiplexer on one chip. By using multiplexing, the number of wires between the SQUIDs and the room temperature electronics can be substantially reduced, which is a big advantage for multichannel systems, such as systems for medical diagnostics and (magnetic) imaging or large arrays of cryogenic particle detectors.

In conclusion, single-chip digital SQUIDs are very attractive candidates to replace conventional analogue dc SQUIDs or second generation dc SQUIDs for low, intermediate and high frequency applications. However, the higher complexity of the digital SQUIDs puts higher demands on the fabrication process. Moreover, in order to surpass the outstanding performance of the best analogue dc SQUIDs currently available, clock frequencies in the GHz range are required. These clock frequencies require complex interfacing electronics between the superconducting electronics and the (room temperature) semiconductor electronics that is used for further data processing. This forms the main disadvantage of the digital SQUID concept compared to, e.g., second generation dc SQUIDs.

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Chapter 3

Coded SQUID arrays

Cryogenic particle detectors [1], such as superconducting tunnel junctions (STJs) [2,3] and electrothermal feedback transition-edge sensor (ETF-TES) microcalorimeters [4], are widely used for astronomical measurements in several wavelength ranges from millimeter waves to X-rays. Traditionally, STJs have been read out by charge sensitive amplifiers (CSA) using a low-noise FET input stage. The main disadvantage of these systems is that their performance is dependent on the input stage capacitance and thus on the size of the STJ. For this reason, the size of high-performance STJ-based X-ray detectors with a FET CSA preamplifier is limited to about 100 x 100 μm^2, which is too small for most practical purposes [5]. Contrary to a FET CSA preamplifier, the impedance at the input of a SQUID system does not affect the noise performance, such that STJs with larger areas can be used. Moreover, SQUIDs can be operated at cryogenic temperatures close to the detector, which reduces the effect of electronic interference. For these reasons, in many cases SQUIDs are currently used for the readout of STJs [4,6]. Because of their low noise, low power and low impedance, also for the readout of ETF-TES microcalorimeters SQUIDs are the preamplifiers of choice [7,8]. The SQUID readout of cryogenic particle detectors is discussed in section 3.1.

Together with the development of large arrays of cryogenic particle detectors, SQUID systems capable of reading out these arrays are required. When using an individual readout system for each pixel, the complexity of the complete readout system is the major limitation on the maximum size of the array. Multiplexing however, is a useful technique to significantly reduce the number of wires from the cryogenic detectors to the SQUIDs and the room temperature electronics, as is discussed in section 3.2. First generation SQUID multiplexers for small arrays have now been developed [9,10,11,12]. At the University of Twente, a SQUID system based on code-division multiplexing, the so-called coded SQUID array, has been developed [13]. In section 3.3, the design of and the experimental results on prototype coded SQUID arrays for the readout of a 7 x 7 array of cryogenic particle detectors are presented.

3.1 SQUID readout of cryogenic particle detectors

The growing interest in high-resolution, high-count-rate cryogenic particle detectors demands a SQUID readout system that is both sensitive enough such that it does not limit the energy resolution and fast enough such that the full signal of the

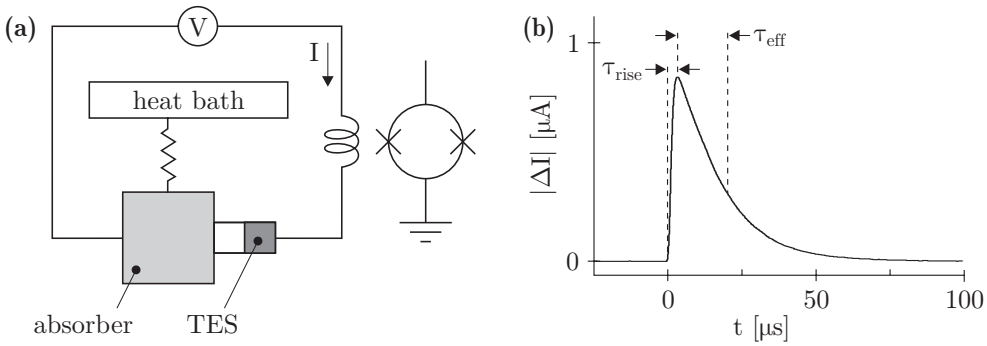

Fig. 3.1 (a) Schematic overview of an ETF-TES microcalorimeter read out by a dc SQUID. **(b)** Typical current pulse measured by the SQUID when a particle is absorbed by the ETF-TES microcalorimeter.

detector can be traced [14]. In this section, the cryogenic particle detectors are more or less treated as black boxes. More details about the operation principles can be found in textbooks on this subject [15].

Basically, the absorption of a particle in an STJ leads to Cooper pair breaking and consequently, the quasiparticle current is increased. The quasiparticle current rise is measured by a SQUID and is a measure for the energy of the particle. For electrothermal feedback transition-edge sensor (ETF-TES) microcalorimeters, see Fig. 3.1a, the absorption of a particle leads to a small temperature rise of the absorber and the TES. This temperature rise results in a significant increase in the resistance R of the TES. Since the TES is voltage biased, this means that the current I that is measured by the SQUID is decreased. As the resistance of the TES increases, the Joule heating $P_{Joule} = V^2/R$ drops and the system returns to its dynamic equilibrium where the Joule heating matches the heat flowing to the heat bath. The reduction in Joule heating compensates for the heat from the particle and the current change ΔI measured by the SQUID is a measure for the energy E of this particle

$$E = \int |\Delta P_{Joule}| dt = V \int |\Delta I| dt \,. \tag{3.1}$$

Using ETF, the speed of response of a TES microcalorimeter is increased by a factor 10^2 or more [1] and the effective time constant or pulse recovery time constant τ_{eff} can be made as small as 10 to 100 μs. Figure 3.1b shows a typical current pulse that is produced by the ETF-TES microcalorimeter when a particle is absorbed.

The amplitude of the current pulses ΔI_{max} produced by an X-ray detector based on an STJ or an ETF-TES microcalorimeter is typically a few μA and the rise time τ_{rise} is of the order of several hundreds of nanoseconds[i] [7,16,17]. Consequently, the current slew rate of the SQUID should be $\partial I/\partial t \approx 10$ A/s. For high-performance cryogenic particle detectors, the input current noise of the SQUIDs should be below

[i] The value of τ_{rise} of a TES for example, is determined by the resistance of the TES and the input coil inductance of the SQUID and possibly an additional inductance.

a few pA/$\sqrt{\text{Hz}}$[ii] [7,18], such that the required current slew rate normalized on the current noise is $(\partial I/\partial t)/\sqrt{S_I} \approx 10^{13}$ s$^{-3/2}$ [19]. These requirements can hardly be met by conventional dc SQUID systems, because of the limited flux slew rate, which is generally smaller than 10^6 Φ_0/s. The typical flux noise of a conventional resistively shunted dc SQUID is about $\sqrt{S_\Phi} \approx 1$ $\mu\Phi_0/\sqrt{\text{Hz}}$, such that the normalized slew rate is around 10^{12} s$^{-3/2}$. However, if SQUID systems with normalized slew rates smaller than 10^{13} s$^{-3/2}$ are used, either the input current noise, $\sqrt{S_I} = \sqrt{S_\Phi}/M_{in}$, or the maximum current slew rate, $\partial I/\partial t = (\partial \Phi_{sig}/\partial t)/M_{in}$, will be compromised, i.e. the input current noise can be improved by increasing the mutual input inductance of the SQUID M_{in}, but this reduces the maximum current slew rate. Digital SQUIDs, e.g. the Smart DROS, allow maximum flux slew rates up to 10^8 Φ_0/s together with a noise performance comparable to that of conventional dc SQUIDs [20]. This means that normalized slew rates up to 10^{14} s$^{-3/2}$ are possible. In chapter 4 and chapter 5, the two-stage SQUID system and the Smart DROS are discussed, respectively. Both systems allow a high slew rate and a low noise level and may be suitable for the readout of cryogenic particle detectors.

3.2 Readout of large arrays of cryogenic particle detectors

Currently, large arrays of cryogenic particle detectors are being developed [21,22] and thus also SQUID systems capable of reading out these arrays are required. The most straightforward approach would be to use one SQUID including readout electronics for each pixel. Thus for an M x N detector array, also M x N SQUIDs would be required. However, the large number of wires from the cryogenic detectors to the SQUIDs and the room temperature electronics would form a major limitation on the maximum size of the array because of, e.g., the large thermal load, the complexity of the readout electronics and the potential unreliability. An elegant way to reduce the number of wires is to use (SQUID) multiplexing. In this section, three SQUID systems based on time-division, frequency-division and code-division multiplexing are discussed.

3.2.1 Time-division multiplexing

At NIST [23], Chervenak *et al.* have developed a SQUID readout system for cryogenic particle detectors based on time-division multiplexing [9,10]. In their circuit, each detector has its own first-stage SQUID, but only one row of SQUIDs is activated at a time. The inactive rows are switched off and do not contribute to the system noise. The bias current is switched from row to row and each multiplexed first-stage SQUID column is read out by a second-stage series SQUID array. A

[ii] The maximum input current noise of the SQUID $\sqrt{S_I}$ required for the readout of an ETF-TES microcalorimeter for example, is determined by the condition that $\Delta I_{max}/\sqrt{S_I}$ should be larger than the dynamic range of the microcalorimeter, $(E_{max} - E_{min})/(\Delta E_{rms}\sqrt{\tau_{eff}})$ [17]. For an energy range from $E_{min} = 0.1$ keV to $E_{max} = 6$ keV with an rms energy resolution of $E_{rms} = 2$ eV for fine spectroscopy, a pulse amplitude of $\Delta I_{max} = 2$ μA and an effective time constant of $\tau_{eff} = 50$ μs, this means that the input current noise of the SQUID should be smaller than $\sqrt{S_I} = 5$ pA/$\sqrt{\text{Hz}}$.

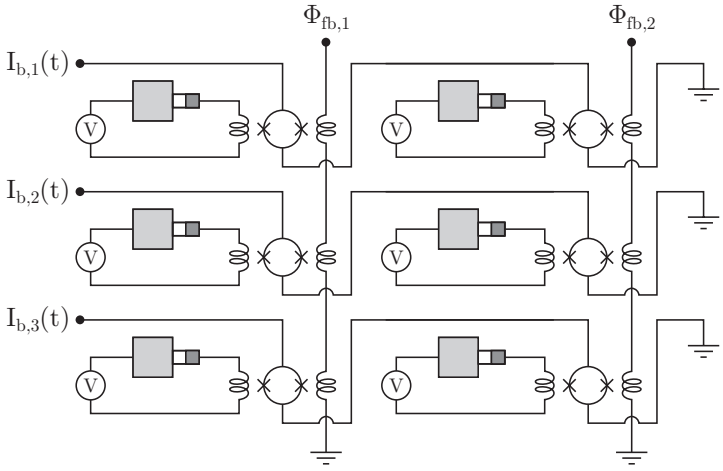

Fig. 3.2 Schematic representation of a time-division SQUID multiplexer for the readout of an array of 6 microcalorimeters. The readout is activated from row to row by switching the bias currents of the SQUIDs. For simplicity, only the first-stage SQUIDs are shown and the voltage biasing circuits of the microcalorimeters are represented by constant voltage sources. All first-stage SQUIDs of one column are coupled to a second-stage series SQUID array (not shown).

feedback flux is applied to the activated first-stage SQUIDs to linearize their output. Since only one SQUID in each column is turned on at a time, one feedback coil can be common to all SQUIDs in the column. Figure 3.2 shows a simplified schematic overview of a time-division SQUID multiplexer for the readout of 6 microcalorimeters.

The sampling frequency that is required to trace the full signal of the particle detector limits the number of rows that can be read out by one SQUID multiplexer. For example, assuming that the maximum switching frequency is 5 MHz and the required sampling rate is 1 MHz per pixel [18], only 5 rows of detectors can be read out by one time-division SQUID multiplexer. For applications requiring smaller bandwidths up to 10 kHz, in principle 32 channels can be multiplexed in a SQUID bandwidth of several MHz [24,25].

First generation time-division SQUID multiplexers have been deployed in 8-pixel ETF-TES microcalorimeters by the NIST group and showed operation without significant additional contribution to the noise of the microcalorimeters [24]. Second generation 32-pixel SQUID multiplexers have now been fabricated at NIST and preliminary low frequency tests showed proper operation [25].

3.2.2 Frequency-division multiplexing

Yoon *et al.* have developed a SQUID readout system based on frequency-division multiplexing [11,12]. A scheme of this system is shown in Fig. 3.3. It uses a single SQUID per row of cryogenic detectors. Each detector of the row is voltage biased using a bias resistor and an alternating current at a separate frequency. The frequencies of the different detectors should be well separated from each other,

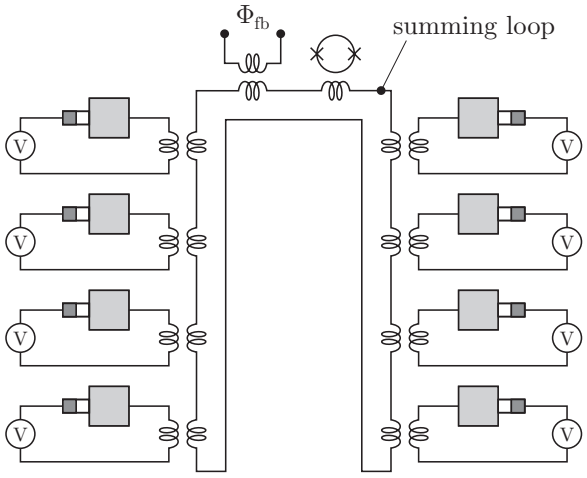

Fig. 3.3 Schematic overview of a frequency-division SQUID multiplexer for the readout of a row of 8 microcalorimeters. All detectors are biased at a separate frequency. For simplicity, the biasing circuits of the ETF-TES microcalorimeters are represented by voltage sources.

which limits the number of detectors per row. All signals are inductively coupled to an output SQUID via a transformer summing loop and are separated again at room temperature by using lock-in detection. In order to linearize the output of the SQUID of each row, a feedback flux is applied to the summing coil. This feedback flux nulls the total current in the summing loop and reduces crosstalk between channels. By using a summing loop however, the coupling inefficiency increases the SQUID current noise referred to the transformer coil primary [11,24]. The total number of SQUIDs in this system is equal to the number of columns.

A drawback of a frequency–division multiplexer is that the wideband noise contributions from the different detectors of each row add, such that the signal-to-noise ratio (SNR) is degraded[iii]. Therefore, an *L-C* tank circuit formed by an inductor and capacitor in the biasing circuit of each pixel has to be used to avoid mixing of noise contributions from different pixels. Thus a different bandpass filter has to be fabricated for each pixel of each row. The implementation of practical *L-C* filters with center frequencies convenient for SQUID readout however, is a technical challenge since the large capacitors that are required (~100 nF) might be difficult to lithographically fabricate without pinholes in the insulating layer [25].

First generation 8-pixel frequency-division multiplexers have been fabricated and tested at low frequencies. The measurements showed that for 8 channels with test signals of bias frequencies ranging from ~2 to ~10 kHz, all signals could be resolved [11]. Measurements on these SQUID multiplexers connected to cryogenic particle detectors have not been reported yet.

[iii] The total noise of an ETF-TES microcalorimeter for example, is almost white and even in the absence of a signal the noise is significant [4]. Consequently, if no filters are used the noise of adjacent channels is mixed and the SNR of each pixel degrades. Using bandpass filters tuned at the biasing frequency, the noise is suppressed outside the bandwidth of the filter.

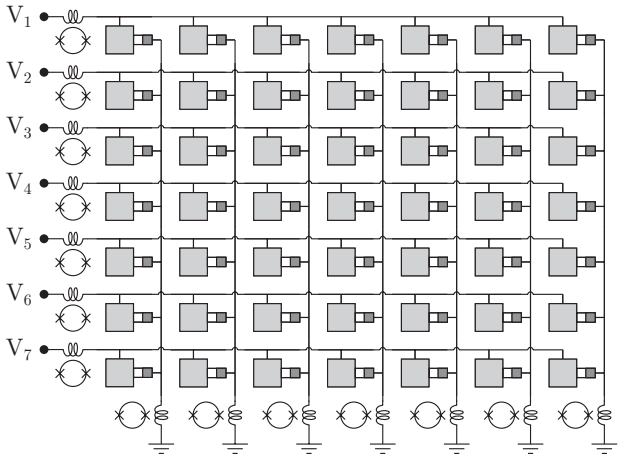

Fig. 3.4 Scheme of an array of 7 x 7 ETF-TES microcalorimeters read out by 14 SQUIDs using the column-row technique. V_1 to V_7 are the bias voltages of the microcalorimeters.

3.2.3 Code-division multiplexing

An important advantage of time-division and frequency-division multiplexing is that using the correct filtering techniques, in principle the noise contributions from the different detectors do not add. Therefore, the SNR does not have to be affected by these readout schemes. The main disadvantage of both schemes however, is that the bandwidth that can be achieved at each pixel is rather limited. Although in several applications a bandwidth of 0.1 to 10 kHz is sufficient [24], high-count-rate cryogenic particle detectors require large bandwidths and high slew rates. If the SNR degradation due to mixing of noise from different pixels is acceptable, e.g. in case of detector arrays of modest size, code-division multiplexing can be applied. In a SQUID readout system based on code-division multiplexing, the bandwidth at each separate pixel is not reduced, such that large bandwidths at each pixel and high count rates can be achieved.

The simplest SQUID readout system based on code-division multiplexing uses the column-row technique [26], shown in Fig. 3.4. In this scheme, one single SQUID is used for reading out one row or one column of particle detectors. Thus for an M x N detector array, the required number of SQUIDs is $M + N$. The row SQUIDs can be used to determine the energy of the absorbed particle, whereas the column SQUIDs are only used for position information. Since the noise contributions from the different detectors add, the number of pixels in the row direction that can be connected to each other is limited. All pixels in the column direction however, can be connected to one single SQUID.

At the University of Twente, the coded SQUID array has been developed [13,14]. This SQUID system for the readout of cryogenic particle detectors is based on code-division multiplexing in which the number of SQUIDs is reduced even more. Figure 3.5 shows the concept for an array of 7 x 7 microcalorimeters. The rows and the columns have their own binary code, i.e. 111, 011, 110, 101, 001, 010 and 100

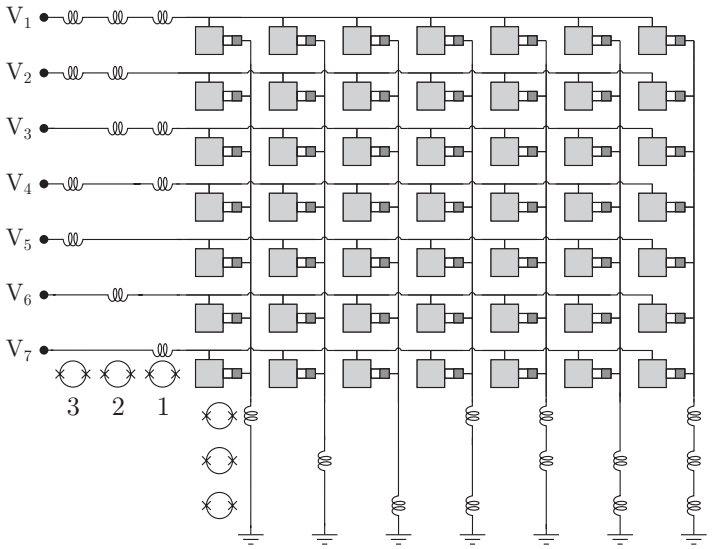

Fig. 3.5 Scheme of a 7 x 7 ETF-TES microcalorimeter array read out by two coded SQUID arrays of each three SQUIDs. V_1 to V_7 represent the bias voltages of the microcalorimeters.

respectively. Thus each pixel in the array has its own unique code representing its position in the array. The bits in this code represent a readout SQUID, e.g. the row with the code 011 is not connected to the first SQUID but it is connected to the second and the third SQUID, as is shown in Fig. 3.5. Using binary codes for the positions of the detectors, $(2^M - 1)$ x $(2^N - 1)$ pixels can be read out by two coded SQUID arrays based on M and N SQUIDs, respectively.

3.3 Prototype coded SQUID arrays

First generation prototype coded SQUID arrays have been developed based on three conventional resistively shunted dc SQUIDs. Two of these systems can be used for the readout of 7 x 7 = 49 cryogenic particle detectors. In this section, the design, the fabrication and the experimental characteristics of these prototype coded SQUID arrays are discussed.

3.3.1 Design and fabrication of coded SQUID arrays

As is discussed in chapters 5 and 6, the Smart DROS can have both a low noise level and a very high maximum flux slew rate. For these reasons, the Smart DROS is an outstanding candidate for the readout of cryogenic particle detectors like STJs and ETF-TES microcalorimeters. For the sake of simplicity however, conventional resistively shunted dc SQUIDs were used in the prototype coded SQUID arrays. Each chip consists of two or three of these dc SQUIDs that are connected to each other to form a coded SQUID array.

As is shown in Fig. 3.5, the SQUIDs that are used in the coded SQUID arrays have multiple input coils. In the design of the SQUIDs, the input coils were spiraled

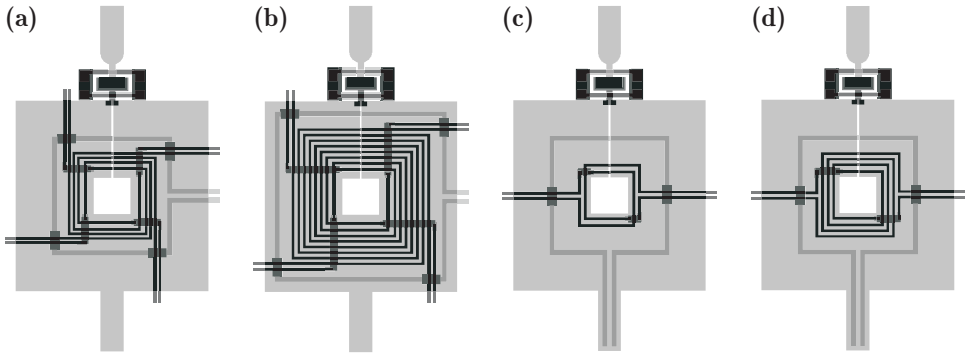

Fig. 3.6 Layout of the four different separate SQUIDs used in the prototype coded SQUID arrays. **(a)** One-turn-four-coil, **(b)** two-turn-four-coil, **(c)** one-turn-two-coil and **(d)** two-turn-two-coil SQUID.

around the SQUID hole into each other to make the layout as symmetric as possible. The only asymmetry is caused by the slit in the washer of the SQUID. Several coded SQUID arrays were designed and fabricated, all based on SQUIDs with an inductance of $L_{sq} = 130$ pH. The number of input coils, two or four, and the number of turns per input coil, one or two, were varied, as is shown in Fig. 3.6. Figure 3.7a shows a micrograph of a SQUID with four input coils of two turns each. The most complex prototype of the coded SQUID arrays consisted of three of these SQUIDs, as is schematically shown in Fig. 3.7b. Using two of these coded SQUID arrays, an array of 7 x 7 = 49 cryogenic particle detectors can be read out.

The coded SQUID arrays were fabricated using standard Nb/Al,AlO_x/Al/Nb technology. In the fabrication process, the definition of the Josephson junctions was performed by reactive ion etching (RIE) in an SF_6 plasma. All other structures, i.e. the first 300 nm thick SiO_2 insulating layer, the Pd resistors, the 300 nm thick Nb wiring layer, the second 350 nm thick SiO_2 insulating layer and the 400 nm Nb top layer, were patterned using the lift-off technique[iv]. The necessary crossovers were made in the top Nb layer to prevent additional holes in the SQUID washers.

The junction size was 4 x 4 μm^2 and the screening parameter was designed to be $\beta_L = 2I_0L_{sq}/\Phi_0 = 1.0$. Here, $I_0 = 8$ μA is the designed critical current of one junction. However, due to fabrication problems related to the AlO_x barrier layer, the experimental critical current was about two times smaller than the design value, which resulted in a lower screening parameter. The estimated junction capacitance is $C_j = 0.48$ pF. In order to remove the junction hysteresis, each junction is shunted with a resistor $R = 6\ \Omega$. To avoid L-C resonances between the SQUID inductance and the junction capacitances, a damping resistor of $R_w = 12\ \Omega$ is placed across the SQUID washer. This resistance is a trade-off between sufficient damping and an acceptable additional flux noise due to the Johnson noise of this resistor.

[iv] In section 5.4.3, the fabrication process at the Low Temperature Division at the University of Twente is described in detail.

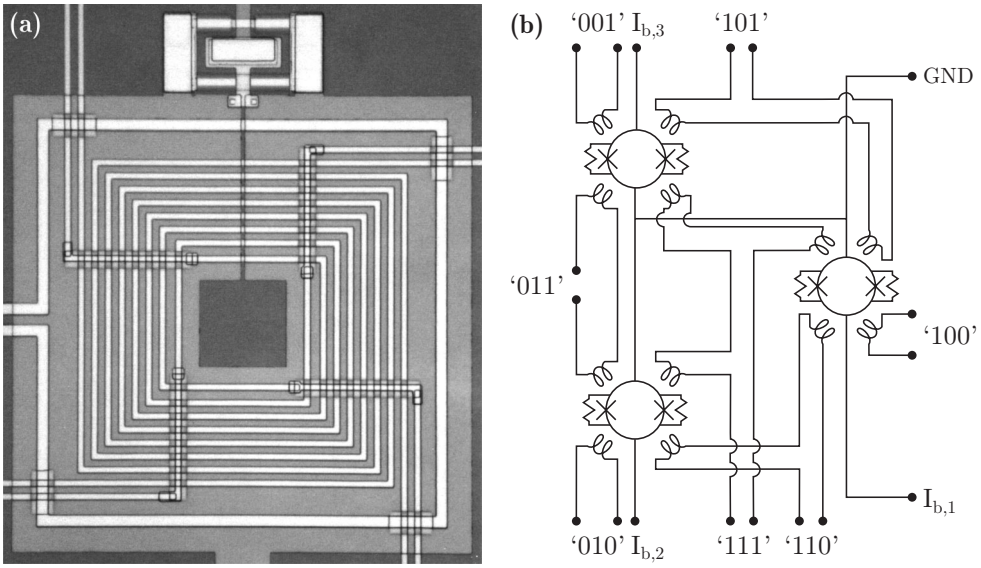

Fig. 3.7 (a) Micrograph of a two-turn-four-coil SQUID used in the coded SQUID arrays. On top of the washer, four input coils and a feedback coil are deposited. The outer dimensions of the SQUID washer are 340 x 340 μm^2. **(b)** Schematic representation of the prototype coded SQUID array based on three SQUIDs with multiple input coils. For simplicity, the feedback coils are not shown.

Crosstalk is an important issue in multiplexed SQUID systems. The unique coding used in the coded SQUID arrays only holds if the parasitic signals due to crosstalk are much smaller than the current pulse that is to be measured when a particle is absorbed. In our design, we considered two types of crosstalk, i.e. direct and indirect crosstalk. Direct crosstalk means that a parasitic signal is coupled from an input coil to a non-addressed SQUID, i.e. parasitic coupling between a SQUID and an input coil on top of another SQUID. Based on the layout of the prototype systems, the parasitic signals caused by direct crosstalk were estimated to be three orders of magnitude smaller than the actual signals.

Direct crosstalk is a frequency independent effect and can be reduced by increasing the distance between the individual SQUIDs of the coded SQUID array. Indirect crosstalk however, is frequency dependent and is caused by inductive coupling between the individual input coils on top of one SQUID. This effect can be estimated as follows. The maximum change in the current through the input coil is of the order of $\partial I/\partial t = 10$ A/s, as was discussed above and the input coil inductance is of the order of $L_{in} = 100$ pH. Assuming that all flux lines are coupled from one input coil to another, i.e. the extreme case that the coupling coefficient is $k = 1$, this would mean a maximum voltage change of $V = L_{in}(\partial I/\partial t) = 1$ nV. This is about three orders of magnitude smaller than the typical bias voltage of an ETF-TES microcalorimeter [6]. For a typical maximum TES resistance of $R = 0.1\ \Omega$, the parasitic current is 0.1 nA. Thus from these estimated values, it can be concluded that signal degradation due to direct or indirect crosstalk is negligibly small when an array of microcalorimeters is read out by a coded SQUID array.

3.3.2 Experimental characteristics of the coded SQUID arrays

For the characterization of the coded SQUID arrays, the chips were glued on an epoxy printed circuit board (PCB) with GE-7031 varnish. The electrical contacts between the chips and the PCB were made by ultrasonic bonding of 25 μm thick Al wires. The devices were cooled down to a temperature of 4.2 K in a stainless steel ^{4}He bath cryostat and were electromagnetically shielded by a superconducting Nb can. For additional shielding, the cryostat was surrounded by a cylindrical μ-metal shielding at room temperature.

All wires between the chips and the room temperature electronics were low pass filtered to prevent radio frequency interference (RFI) [27,28]. The cut-off frequency of the *L-C-R* filters in the voltage lines was about 1 MHz and the bias current lines had a cut-off frequency of about 25 kHz. Standard homemade battery powered *I-V* electronics was used for the characterization of the coded SQUID arrays. An R_{in}-C_{in} shunt of R_{in} = 47 Ω and C_{in} = 1 nF was connected across the input coils of the coded SQUID arrays to damp microwave resonances in the input coil [29,30]. The blocking capacitor C_{in} prevents that low frequency current noise generated by the damping resistor flows directly through the input coil, generating a flux noise.

Figure 3.8a shows the typical experimental *I-V* characteristics of a separate one-turn-two-coil SQUID. The flux was swept via the feedback coil that was deposited on top of the washer. Figure 3.8b shows the corresponding V-Φ_{sig} characteristics for different values of the bias current. At the optimum bias current, $I_b \approx 12$ μA, the voltage modulation depth was ~15 μV and the flux-to-voltage transfer was ~60 μV/Φ_0.

The flux noise spectra of the coded SQUID arrays were measured by using a two-stage SQUID system. In this setup, a DROS was used as a low-noise cryogenic preamplifier for the coded SQUID array, as is discussed in detail in chapter 4. An

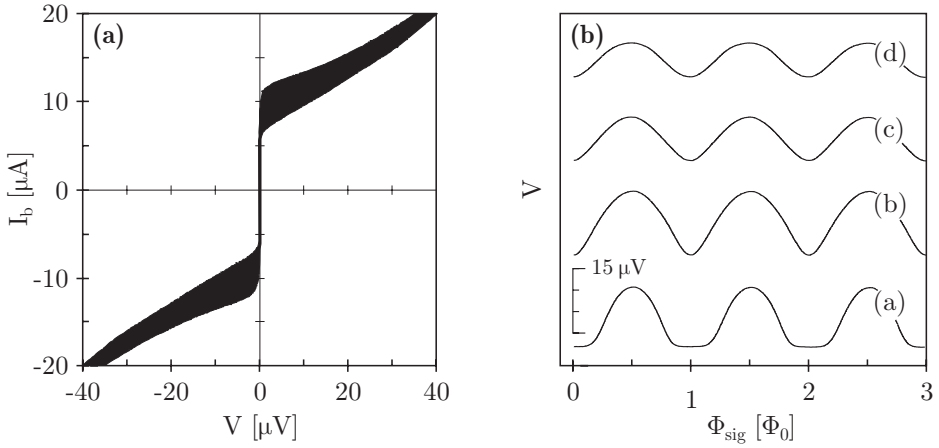

Fig. 3.8 (a) Experimental current vs. voltage (*I-V*) characteristics of a separate one-turn-two-coil SQUID at 4.2 K. The flux was swept via the feedback coil. **(b)** Corresponding voltage vs. flux (V-Φ_{sig}) characteristics for different bias currents. For trace (a), the bias current was I_b = 10 μA, for trace (b) 12 μA, for trace (c) 14 μA and for trace (d) 16 μA. The vertical offsets are arbitrary.

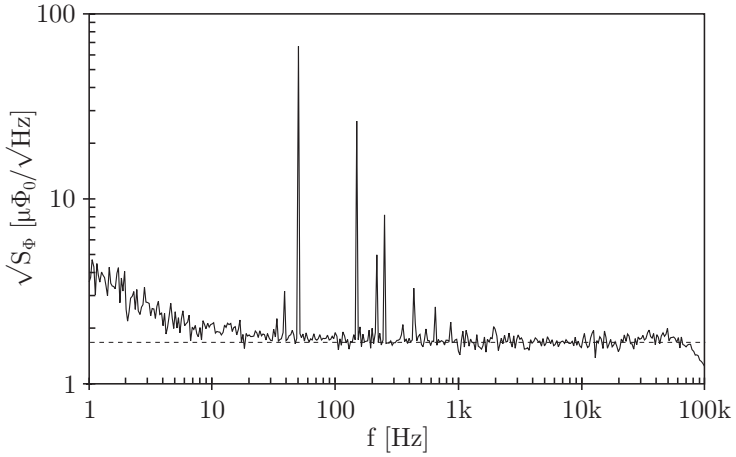

Fig. 3.9 Experimental flux noise spectrum of a separate one-turn-two-coil SQUID at 4.2 K. The measurement was performed in a two-stage setup with a DROS as a low-noise cryogenic preamplifier. The white flux noise level is 1.7 $\mu\Phi_0/\sqrt{\text{Hz}}$. The bias voltage of the SQUID was $V_{bias} \approx 5$ μV.

important advantage of the two-stage SQUID system is that the system allows the intrinsic SQUID flux noise to be measured in a direct voltage readout mode without being limited by the input voltage noise of the room temperature preamplifier. Thus, no ac flux modulation is required. The white flux noise of the separate SQUIDs was measured to be 1.7 $\mu\Phi_0/\sqrt{\text{Hz}}$, as is shown in Fig. 3.9, whereas the design value was 0.9 $\mu\Phi_0/\sqrt{\text{Hz}}$. The discrepancy between the design value and the experimental value is caused by the too low critical current of the junctions, as was discussed above.

Because of the highly symmetric design, the mutual inductances between the input coils and the SQUIDs were all very similar. The mutual input inductances of the simplest one-turn-two-coil SQUIDs were measured to be 94 to 96 pH. As expected, the mutual input inductances of the most complex two-turn-four-coil SQUIDs were measured to be about twice as large, i.e. the values ranged from 189 to 196 pH. The parasitic mutual inductances that could cause direct crosstalk were measured to be 0.1 pH for the one-turn coded SQUID arrays and 0.2 pH for the two-turn coded SQUID arrays. This is indeed three orders of magnitude smaller than the mutual inductances between an input coil and the addressed SQUID. Indirect crosstalk was not measured.

3.4 Conclusion and discussion

The readout systems for cryogenic particle detectors, such as STJs and ETF-TES microcalorimeters, are just one of the many applications for which SQUIDs can be used. Because of their low noise, low power consumption and low impedance, the SQUID is the preamplifier of choice for these particle detectors. In the first section of this chapter, SQUID readout for cryogenic particle detectors was discussed and it was shown that both very sensitive and very fast SQUID systems are required to

trace the full signal of the detector. In the advent of large arrays of particle detectors, also SQUID systems capable of reading out these arrays are required. A useful technique to reduce the complexity of the SQUID readout systems is SQUID multiplexing. In section 3.2, three SQUID multiplexers were discussed: The time-division SQUID multiplexer, the frequency-division SQUID multiplexer and the code-division SQUID multiplexer.

The SQUID system based on code-division multiplexing, the coded SQUID array, which was proposed in section 3.2.3, can be used to read out an array of cryogenic particle detectors. This system allows the arrays to be read out by a significantly reduced number of SQUIDs. The number of SQUIDs that is used in a coded SQUID array can be further reduced in several ways. First of all, positive and negative coupling between the coils and the SQUIDs can be used. In the prototype systems described in this chapter, this difference was not made. Secondly, the number of SQUIDs can be reduced by using weight factors. In that case, one could use a coded SQUID array to read out the rows of the cryogenic particle detector array and a single SQUID to read out the columns. Each column should have a unique mutual inductance with this readout SQUID. The unique ratio between the signals measured by the coded SQUID array and this readout SQUID determines the column of the activated detector and the code generated by the coded SQUID array determines the row. The coded SQUID array can be used to determine the energy of the absorbed particle, whereas the single SQUID is only used for position information.

Although the number of SQUIDs reduces by using code-division multiplexing, an important disadvantage of this concept is that the noise contributions from the different detectors add. The margins in the performance parameters of the cryogenic particle detectors determine the maximum number of pixels that can be connected to each other. The SQUID multiplexer of Chervenak *et al.* does not suffer from this problem, since each detector has its own SQUID. However, the on and off switching of the bias current in their system is disadvantageous for the bandwidth that can be achieved at each pixel in case of, e.g., high-count-rate or large particle detector arrays. Furthermore, dead-time due to this switching reduces the number of channels that can be multiplexed in the available bandwidth [24]. Moreover, this concept requires a large number of SQUIDs, i.e. the number of first-stage SQUIDs is equal to the number of detectors, and the room temperature electronics with switched feedback is rather complex. In the SQUID multiplexer of Yoon *et al.*, each detector has its own ac bias frequency and the signals are separated at room temperature again by lock-in detection. This means that bandpass filters can be used to avoid mixing of noise contributions from different pixels. However, the implementation of practical L-C filters might be difficult and also the complexity of the room temperature electronics to demodulate many high frequency channels in case of large arrays might be a limitation for the number of detectors that can be multiplexed. Moreover, the required frequency spacing between adjacent channels limits the number of channels that can be multiplexed in the available bandwidth. It can be concluded that in choosing the optimum SQUID multiplexer for a certain array, many technical trade-offs have to be made and that no one best solution for all applications exists.

The prototype SQUID arrays that were discussed in section 3.3 were based on three conventional resistively shunted dc SQUIDs. Using two of these SQUID multiplexers, 49 channels can be read out. The calculations and the experiments on these prototype systems showed that both direct and indirect crosstalk can be made negligibly small. For the readout of the individual SQUIDs of the coded SQUID array, a two-stage SQUID system can be used in which a second stage SQUID, e.g. a DROS, is used as a low-noise cryogenic preamplifier. In the next chapter, two-stage SQUID systems based on a DROS as the second stage are discussed in detail.

Using digital SQUIDs, e.g. Smart DROSs, instead of conventional dc SQUIDs in the coded SQUID arrays, has some important advantages. Firstly, the number of wires from the SQUID system to the room temperature electronics can be reduced, since digital SQUIDs can be multiplexed at cryogenic temperatures [31]. Even more important is the high maximum slew rate that can be achieved with a digital SQUID. Especially the combination of a high flux slew rate and low flux noise is advantageous for the readout of cryogenic particle detectors. In chapter 5 of this thesis, the Smart DROS is discussed as a digital SQUID based on a DROS.

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Chapter 4

Two-stage SQUID systems

The flux-to-voltage transfer of standard resistively shunted dc SQUIDs is of the order of 100 $\mu V/\Phi_0$ and the white flux noise is typically around 1 $\mu\Phi_0/\sqrt{Hz}$. This corresponds to an output voltage noise of 0.1 $nV/\sqrt{Hz}$, which is about one order of magnitude smaller than the input voltage noise of a low-noise room temperature dc preamplifier. This leads to preamplifier limitation of the system sensitivity. Flux modulation together with an impedance matching network is often used to solve this problem. Although wideband systems based on ac flux modulation have been demonstrated [1,2], the modulation frequency is in most cases of the order of 100 kHz, which means a small measurement bandwidth and a low slew rate.

Another approach to solve the matching problem is to increase the output of the SQUID itself, which resulted in the so-called second generation dc SQUIDs, e.g. SQUIDs with additional positive feedback (APF) [3,4], double relaxation oscillation SQUIDs (DROSs) [5,6], series SQUID arrays [7,8] and two-stage SQUID systems [9,10,11,12,13]. The flux-to-voltage transfer of the second generation dc SQUIDs is of the order of 1 mV/Φ_0, which is large enough for a direct voltage readout mode without ac flux modulation.

In this chapter, two-stage SQUID systems with a DROS as the second stage are presented [14,15]. The operation principle is described in section 4.1. In section 4.2, some practical aspects of two-stage SQUID systems are discussed and the two-stage SQUID system is compared to a readout scheme using commercial flux modulated electronics. As will be shown, the ac flux modulated electronics limits the sensitivity of the SQUID systems, whereas the intrinsic SQUID noise can be measured using a two-stage setup. Because integration of the sensor SQUID and the second stage SQUID on one chip leads to more reliable systems, integrated two-stage SQUID systems have been designed. The design and the measurements are respectively presented in sections 4.3 and 4.4.

4.1 Operation principle

Basically, a two-stage SQUID system consists of a sensor SQUID and a second stage SQUID that serves as a low-noise cryogenic preamplifier for the sensor SQUID. In Fig. 4.1a, a scheme of a two-stage SQUID system is shown. The sensor SQUID is biased at a constant voltage V_{bias} and the current I_1 through this SQUID is coupled to the second stage in such a way that the flux gain $G_\Phi = \partial\Phi_{2nd}/\partial\Phi_{sig}$ is generally larger than unity. Consequently, the output of the sensor SQUID is

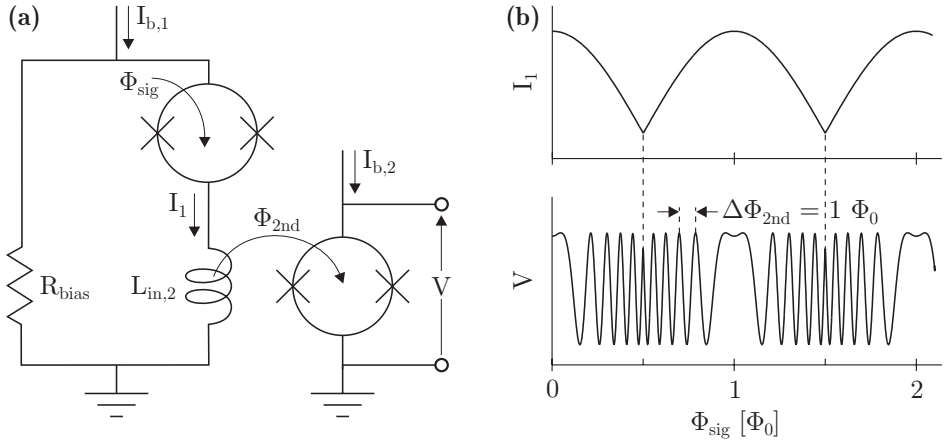

Fig. 4.1 (a) Scheme of a two-stage SQUID system. The second stage SQUID is represented by a conventional dc SQUID but also a second generation dc SQUID, e.g. a DROS, can be used. **(b)** Schematic representation of the I_1-Φ_{sig} characteristic of the sensor SQUID and the resulting V-Φ_{sig} characteristic of the complete two-stage SQUID system.

amplified by the second stage and the sensor SQUID determines the overall system noise. Because of the excellent noise properties of a conventional resistively shunted dc SQUID, this type of SQUID is generally used as the sensor SQUID. The sensor SQUID can be optimized with respect to noise and the second stage can be designed for maximum output. In this section, the operation principle of the two-stage SQUID system is described in detail, starting with the two bias modes of a dc SQUID.

4.1.1 Sensor SQUID biasing

A dc SQUID can be operated in two basic bias modes [16,17,18]. In the current bias mode, a constant current I_b is passed through the SQUID and the SQUID acts as a flux-to-voltage converter. This bias mode is, e.g., used in flux modulated systems. In the voltage bias mode, the voltage across the SQUID is kept constant and the current through it is detected, i.e. the SQUID acts as a flux-to-current converter. The intrinsic energy resolution of the dc SQUID remains unchanged for both bias modes [17]. The effective load impedance of a current-biased SQUID should be high, whereas a voltage-biased SQUID should be connected to a circuit with a very low input impedance, e.g. a superconducting input coil of another SQUID. Therefore, voltage biasing is particularly attractive for two-stage SQUID systems.

In a two-stage SQUID system, the sensor SQUID is usually biased at a constant voltage by means of a small bias resistor $R_{bias} \ll R_{dyn}$, where R_{dyn} is the dynamic resistance of the sensor SQUID at the working point, $\Phi_{sig} = (1/4 + n/2)\Phi_0$ with n an integer. For a screening parameter of $\beta_{L,1} \approx 1$, the dynamic resistance can be estimated as $R_{dyn} \approx R/2$, where R is the shunt resistance to remove the junction hysteresis. By fixing the bias voltage across the sensor SQUID, the current I_1 through it is modulated by the applied signal flux Φ_{sig}, as is shown in Fig. 4.1b.

In a two-stage SQUID system, the current I_1 is fed through the input coil $L_{in,2}$ of a second stage SQUID and is converted to a magnetic flux $\Phi_{2nd} = M_{in,2} I_1$, introducing a flux gain $G_\Phi = \partial\Phi_{2nd}/\partial\Phi_{sig}$. Here, $M_{in,2}$ is the mutual inductance between the second stage SQUID and its input coil. Generally, the second stage SQUID is operated in current bias mode and the output signal of the complete two-stage SQUID system is the voltage across the second stage. As a result of the inductive coupling between the sensor SQUID and the second stage, the voltage across the second stage is indirectly modulated by the signal flux Φ_{sig}. In most cases, the flux gain is larger than unity, which results in a V-Φ_{sig} characteristic for the two-stage SQUID system as shown in Fig. 4.1b. Assuming that the second stage is represented by a single SQUID, as shown in Fig. 4.1a, the maximum flux-to-voltage transfer of the two-stage SQUID system at the working point is given by

$$\frac{\partial V}{\partial \Phi_{sig}} = G_\Phi \frac{\partial V}{\partial \Phi_{2nd}}, \tag{4.1}$$

where $\partial V/\partial\Phi_{2nd}$ is the flux-to-voltage transfer of the second stage SQUID.

In order to analyze the dynamics of a two-stage SQUID system, the I-V characteristics of the sensor SQUID can be approximated by straight lines, i.e.,

$$\begin{aligned} I_1 &= I_{c,max} + \left(I_{b,1} - I_1\right) R_{bias} \big/ R_{dyn} \quad \text{for} \quad \Phi_{sig} = \mathrm{n}\Phi_0, \\ I_1 &= I_{c,min} + \left(I_{b,1} - I_1\right) R_{bias} \big/ R_{dyn} \quad \text{for} \quad \Phi_{sig} = \left(\mathrm{n} + \frac{1}{2}\right)\Phi_0. \end{aligned} \tag{4.2}$$

This approximation is only valid for small bias voltages. From Eq. (4.2), the maximum modulation depth of the current through the sensor SQUID is calculated to be

$$\Delta I_1 = \frac{\partial I_1}{\partial I_{c,1}} \Delta I_{c,1} \quad \text{with} \quad \frac{\partial I_1}{\partial I_{c,1}} = \frac{R_{dyn}}{R_{dyn} + R_{bias}}, \tag{4.3}$$

where $\Delta I_{c,1} = I_{c,max} - I_{c,min}$ is the modulation depth of the critical current of the sensor SQUID. For ideal current biasing, i.e. $R_{bias} \to \infty$, the current modulation depth ΔI_1 becomes zero and for ideal voltage biasing, i.e. $R_{bias} \to 0$, ΔI_1 equals $\Delta I_{c,1}$. In practical systems, the bias mode is non-ideal, i.e. one has a combination of both bias modes and ΔI_1 has a value between zero and $\Delta I_{c,1}$.

To make a choice for the value of the bias resistance, it should be noticed that biasing the sensor SQUID at a constant voltage by using a small bias resistor causes an additional voltage noise of $S_{V,bias} = 4k_B T R_{bias}$. For $R_{bias} \ll R_{dyn}$, this noise contribution becomes much smaller than the Johnson noise generated in the shunt resistors R of the sensor SQUID, $S_{V,1} \approx 16 k_B T R$. However, making the bias resistance unnecessarily small results in a large Joule dissipation V_{bias}^2/R_{bias}. Consequently, a trade-off should be made between a low noise contribution of the bias resistor and a large current modulation depth ΔI_1 on the one hand and a low dissipation on the other hand. Typically, bias resistances of about 5 to 10 % of the shunt resistances are used [12,15,19].

4.1.2 Flux gain and noise properties

An important parameter in the design of a two-stage SQUID system is the flux gain G_Φ. The flux gain has to be sufficiently large, such that the amplified flux noise of the sensor SQUID is much larger than the flux noise related to the second stage SQUID and the readout electronics at room temperature. The total flux noise of a two-stage SQUID system with direct voltage readout can be expressed as

$$S_\Phi = S_{\Phi,1} + \frac{1}{G_\Phi^2}\left(S_{\Phi,2} + \frac{S_{V,amp}}{V_{\Phi,2}^2}\right). \tag{4.4}$$

Here, S_Φ is the flux noise spectral density, $S_{V,amp}$ is the voltage noise of the room temperature preamplifier and $V_{\Phi,2} = \partial V/\partial\Phi_{2nd}$. The indices 1 and 2 refer to the stage numbers: 1 for the sensor SQUID and 2 for the second stage. In Eq. (4.4), it is assumed that $R_{bias} \ll R_{dyn}$, such that the noise contribution of the bias resistor can be neglected.

When using a second generation dc SQUID as the second stage, the noise contribution of the room temperature dc preamplifier can be neglected compared to the noise of the second stage. In that case, the two-stage SQUID system can be operated in a direct voltage readout mode without ac flux modulation, which reduces the complexity of the room temperature readout electronics. If we want the flux noise of the second stage to contribute at most a fraction p to the total noise power, the flux gain should then be at least [15]

$$G_\Phi \geq \sqrt{\frac{1}{p}-1}\,\sqrt{\frac{S_{\Phi,2}}{S_{\Phi,1}}} \;\leftrightarrow\; G_\Phi \geq \sqrt{\frac{1}{p}-1}\,\sqrt{\frac{\varepsilon_2 L_{sq,2}}{\varepsilon_1 L_{sq,1}}}\,. \tag{4.5}$$

In this equation, ε_1 and ε_2 are the energy resolutions and $L_{sq,1}$ and $L_{sq,2}$ are the SQUID inductances of the first and second stage, respectively. The maximum available flux gain at the working point can be estimated as

$$G_\Phi = M_{in,2}\frac{\partial I_1}{\partial\Phi_{sig}} \quad \text{with} \quad \frac{\partial I_1}{\partial\Phi_{sig}} = \frac{\partial I_1}{\partial I_{c,1}}\frac{\partial I_{c,1}}{\partial\Phi_{sig}}\,, \tag{4.6}$$

where $I_{c,1}$ is the critical current of the sensor SQUID. By approximating the $I_{c,1}(\Phi_{sig})$ characteristics of the sensor SQUID by a |cos|-function, the factor $\partial I_{c,1}/\partial\Phi_{sig}$ can be calculated as [20]

$$\left|\frac{\partial I_{c,1}}{\partial\Phi_{sig}}\right|_{\Phi_{sig}=1/4\Phi_0} \approx \frac{4.4}{1+\beta_{L,1}}\frac{I_{0,1}}{\Phi_0}\,, \tag{4.7}$$

where $I_{0,1}$ represents the critical current of one junction of the sensor SQUID and $\beta_{L,1} = 2I_{0,1}L_{sq,1}/\Phi_0$ symbolizes the screening parameter of the sensor SQUID. In practice, the flux gain is dependent on the bias voltage of the sensor SQUID and decreases when the bias voltage increases. Moreover, the available flux gain decreases for frequencies above the cut-off frequency of the first stage.

4.1.3 Bandwidth and slew rate of two-stage SQUID systems

The inductance of the input coil of the second stage $L_{in,2}$ and the resistances R_{dyn} and R_{bias} form a first-order low-pass filter. Consequently, the intrinsic bandwidth of the two-stage SQUID system is limited by the cut-off frequency of the first stage given by

$$f_{c,1} = \frac{R_{dyn} + R_{bias}}{2\pi L_{in,2}} . \tag{4.8}$$

Thus, to achieve a large intrinsic bandwidth, the input coil inductance $L_{in,2}$ should not be made unnecessarily large. However, since $L_{in,2}$ also affects the flux gain, one should compromise between large gain and high cut-off frequency. The maximum bandwidth in flux locked loop (FLL),

$$f_{max} = \frac{GM_{fb,1}}{2\pi\tau_{int}R_{fb}} \frac{\partial V}{\partial \Phi_{sig}} , \tag{4.9}$$

can never exceed the intrinsic bandwidth of the two-stage SQUID system. In Eq. (4.9), G represents the gain of the dc preamplifier at room temperature, $M_{fb,1}$ is the mutual inductance between the feedback coil and the sensor SQUID, τ_{int} is the time constant of a one-pole integrator and R_{fb} is the feedback resistance.

From Eq. (4.9), it can be concluded that the maximum bandwidth in FLL can be enhanced in several ways. Either the electronics can be optimized for maximum bandwidth in FLL, e.g. by increasing G, or the SQUID itself can be optimized, e.g. by increasing $M_{fb,1}$ or $\partial V/\partial \Phi_{sig}$. However, the gain-bandwidth product of an operational amplifier (op-amp) is fixed, which means that the gain G of the preamplifier cannot be increased without reducing its intrinsic bandwidth. In order to increase $\partial V/\partial \Phi_{sig}$, the inductance of the input coil of the second stage $L_{in,2}$ can be increased, but this leads to a smaller intrinsic bandwidth of the two-stage SQUID as was discussed above. Reducing the ratio $M_{fb,1}/R_{fb}$ also increases the maximum bandwidth in FLL, but this changes the $\partial V_{FLL}/\partial \Phi_{sig}$ transfer in FLL. Thus although the maximum bandwidth in FLL can be enhanced in several ways, one should carefully consider the (adverse) effects of changing a parameter.

When using a one-pole integrator, the maximum flux slew rate of the two-stage SQUID system operated in FLL is given by [16]

$$\frac{\partial \Phi_{sig}}{\partial t} = 2\pi\delta\Phi f_{max} . \tag{4.10}$$

The slew rate is frequency independent and increases linearly with the bandwidth in FLL and the linear flux range $2\delta\Phi$. Using Eq. (4.1), the maximum linear flux range of a two-stage SQUID system with a single SQUID as the second stage can be expressed as

$$2\delta\Phi = \frac{2\delta V}{\partial V/\partial \Phi_{sig}} = \frac{2\delta V}{G_{\Phi}\left(\partial V/\partial \Phi_{2nd}\right)} . \tag{4.11}$$

Here, $2\delta V$ is the usable voltage swing of the second stage. Thus the linear flux range decreases when the flux gain is increased. However, the maximum flux slew rate does not decrease but is independent on the flux gain,

$$\frac{\partial \Phi_{sig}}{\partial t} = \frac{\delta V G M_{fb,1}}{\tau_{int} R_{fb}}. \tag{4.12}$$

It should be noted that the maximum value of the flux slew rate is estimated by Eqs. (4.10) and (4.12), i.e. these equations are only valid as long as $f_{max} < f_{c,1}$ and f_{max} is smaller than the bandwidth limits resulting from noise, the finite bandwidth of the room temperature electronics and dead-time in the feedback loop.

4.1.4 The second stage SQUID

In the previous subsections, the second stage was implicitly assumed to be a single dc SQUID. However, for the second stage any type of SQUID can be used. One can distinguish two categories. Firstly, a series SQUID array can be used [12,13,21], as is shown in Fig. 4.2. In a series SQUID array, typically $N = 100$ SQUIDs are connected in series [7,8,22,23] and are modulated coherently, such that a substantial increase of the usable voltage swing $2\delta V = N2\delta V_i$ is realized. Here, the subscript i denotes one SQUID of the array. A two-stage SQUID system with a SQUID array

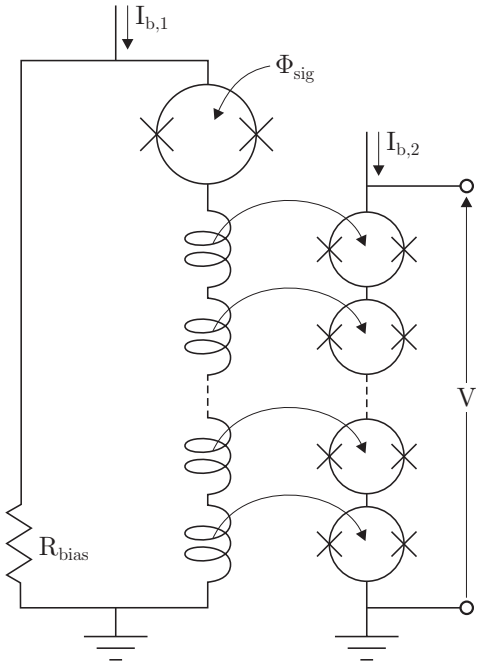

Fig. 4.2 Schematic overview of a two-stage SQUID system with a series array of N SQUIDs as the second stage. All SQUIDs of the array are modulated coherently, such that the usable voltage swing $2\delta V$ is increased by N. The linear flux range of the separate SQUID array is equal to the linear flux range of a single dc SQUID.

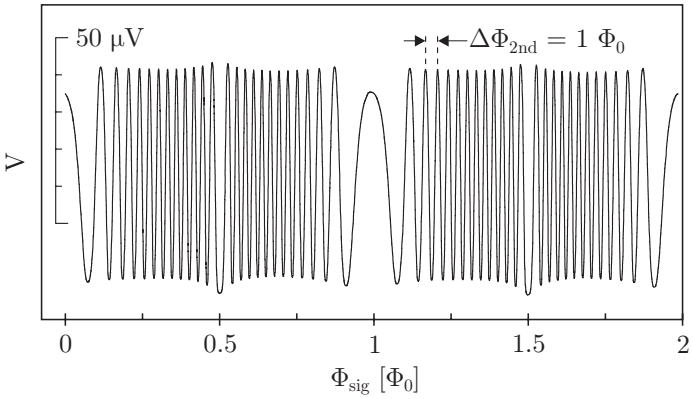

Fig. 4.3 Experimental V-Φ_{sig} characteristic of a non-integrated two-stage SQUID system consisting of a ramp-type dc SQUID as the sensor SQUID and a DROS with reference SQUID as the second stage.

as the second stage can be designed such that the linear flux range[i] is not decreased, since the linear flux range of a separate SQUID array is $2\delta\Phi = 2\delta\Phi_i$. To do so, the flux gain from the sensor SQUID to each individual SQUID should be $G_{\Phi,i} = 1$, i.e. $G_\Phi = N$. Welty and Martinis developed a two-stage SQUID system based on a series array of 100 SQUIDs [12]. A similar device is commercially available from HYPRES [24]. For this two-stage SQUID system however, the linear flux range was decreased because of a flux gain of $G_\Phi > N$.

An important practical disadvantage of a series SQUID array is that all SQUIDs should be modulated coherently. Among other things, this means that the mutual inductance between the input coil and each SQUID should be the same and that there should be no random flux offset between the SQUIDs, e.g. caused by trapped flux or by parasitic coupling. In practice, variations in the mutual inductance from SQUID to SQUID cause amplitude modulation of the V-Φ characteristics and trapped flux can cause severe distortions of the characteristics of the two-stage SQUID systems based on SQUID arrays [7,22,25].

Secondly, a single SQUID can be used for the second stage [11,26,27,28], which is the simplest option. Since the second stage is used as a preamplifier, it is beneficial to use a SQUID with a large flux-to-voltage transfer and a large usable voltage swing. In case of a single second stage SQUID, the linear flux range is decreased as was discussed in section 4.1.3, but the design and the practical use is less complicated than that of a SQUID array. The reduction of the linear flux range is clearly visible in Fig. 4.3, which shows an experimental flux-to-voltage characteristic of a two-stage SQUID system with a DROS as the second stage. For the measurement shown in Fig. 4.3, a DROS designed and fabricated by Van Duuren *et al.* [29] at the University of Twente was used. The SQUID inductance was $L_{sq,2} = 550$ pH, the screening parameter was $\beta_{L,2} = 1.2$ and the mutual inductance between the DROS

[i] The maximum linear flux range of a two-stage SQUID system with a series SQUID array as the second stage is given by $2\delta\Phi = 2\delta\Phi_i / G_{\Phi,i}$.

and its input coil was $M_{in,2} = 6.7$ nH. The flux noise of the DROS was 6 $\mu\Phi_0/\sqrt{\text{Hz}}$ and the flux gain of the two-stage SQUID system was $G_\Phi \approx 25$. The flux-to-voltage transfer of the DROS was large enough, $\partial V/\partial\Phi_{2nd} \approx 1$ mV/Φ_0, such that in a direct voltage readout mode the noise contribution of the room temperature preamplifier could be neglected. The sensor SQUID was based on ramp-type Josephson junctions. These experiments are discussed in more detail in chapter 6.

Assume that instead of the DROS a single resistively shunted dc SQUID with the same SQUID inductance and the same SQUID capacitance, $C_{sq,2} = 0.5$ pF, would be used. Furthermore, assume that the screening parameter is $\beta_{L,2} = 1$ and that the McCumber parameter is $\beta_{C,2} = 0.3$. This means that shunt resistors with a resistance of $R = 15\ \Omega$ should be used. Consequently, the theoretical flux-to-voltage transfer can be estimated as $\partial V/\partial\Phi_{2nd} \approx R/L_{sq,2} = 55\ \mu\text{V}/\Phi_0$. This value is a factor 18 smaller than the flux-to-voltage transfer of the DROS. Thus, when using a single dc SQUID in direct voltage readout mode, the input voltage noise of the room temperature preamplifier would form an important noise contribution. Therefore, to measure the intrinsic flux noise of the sensor SQUID, a single dc SQUID as the second stage requires a much larger flux gain than a DROS as the second stage.

The remaining part of this chapter concentrates on two-stage SQUID systems based on a DROS as the second stage. It is shown that using a DROS allows a simple design of a two-stage SQUID system with excellent noise characteristics.

4.2 Practical aspects of two-stage SQUID systems based on a DROS

In the previous section, the operation principle and the most important parameters of the two-stage SQUID system were discussed. In this section, the problem of multiple working points in FLL caused by the required flux gain in a two-stage SQUID system is discussed and the feasibility of a practical two-stage SQUID system based on a DROS is demonstrated.

4.2.1 Two-stage SQUID systems in flux locked loop

When using a DROS as the second stage, the flux gain causes multiple modulation periods in the flux-to-voltage characteristic of the second stage for only one modulation period in the flux-to-current characteristic of the sensor SQUID, as is shown in Fig. 4.3. Consequently, if the two-stage SQUID is operated in FLL, the system might lock to multiple working points, each with a different working point for the sensor SQUID. However, the noise of the sensor SQUID is the lowest at the working points $\Phi_{sig} = (1/4 + n/2)\Phi_0$ [30]. Moreover, the practical flux gain is the largest at these points. As a result of these multiple working points, the two-stage SQUID system in FLL might lock to a non-optimum state. To prevent degradation of the system noise due to locking to an undesirable working point, the system should be locked either manually or automatically close to the optimum working point. This can be done by applying a flux bias to the sensor SQUID and if necessary also to the DROS. For large flux gains, a flux bias for the DROS is not required. The locking procedure that can be used to lock the two-stage SQUID system to the optimum working point is summarized in Fig. 4.4.

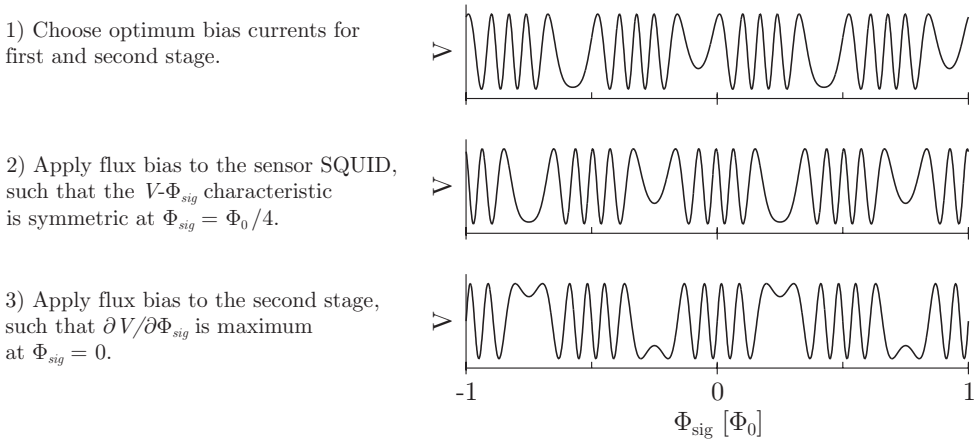

Fig. 4.4 Locking procedure for a two-stage SQUID system with multiple working points using a flux bias for the sensor SQUID and the second stage. After step 3, the FLL locks to the optimum working point when resetting without applying flux. For simplicity, sinusoidal behavior was assumed for the characteristics of the sensor SQUID and the second stage.

For a well-designed two-stage SQUID system based on an N-SQUID array, multiple working points can be avoided when $G_\Phi = N$, as was discussed in section 4.1.4. In two-stage SQUID systems based on a DROS as the second stage, the number of working points can be reduced by decreasing the flux gain. However, the flux gain should be large enough to make the noise contributions of the second stage and the room temperature preamplifier (much) smaller than the intrinsic noise of the sensor SQUID.

4.2.2 Non-integrated and integrated two-stage SQUID systems

The sensor SQUID and the second stage SQUID can either consist of two separate chips or both SQUIDs can be integrated on one single chip. The first configuration will be called the non-integrated two-stage SQUID system and the latter the integrated two-stage SQUID system. In non-integrated systems, the sensor and the second stage are connected on a printed circuit board (PCB) by bonding of Al wires. The disadvantage of this configuration is that it is less reliable than an integrated two-stage SQUID system and that the bonding wires introduce an additional parasitic inductance in the first stage, which leads to a reduced measurement bandwidth. On the other hand, this configuration allows more flexibility in the design of the sensor SQUID and the second stage. Consequently, for low to intermediate frequency applications, e.g. the readout of a cryogenic current comparator (CCC) [31,32] or gravitational wave detectors [33,34], the non-integrated concept might be more suited.

The main advantage of an integrated two-stage SQUID system is that the bandwidth is not limited by Al bonding wires between the sensor SQUID and the second stage, such that large intrinsic bandwidths can be achieved. This means that this configuration is particularly attractive for intermediate to high frequency applications, e.g. the readout of cryogenic particle detectors.

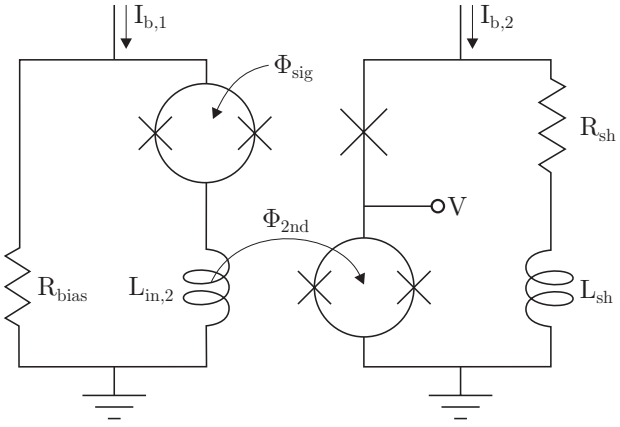

Fig. 4.5 Schematic overview of a two-stage SQUID system with a DROS with reference junction as the second stage. In this scheme, the output signal is the voltage V across the signal SQUID of the DROS. The DROS can either be a separate chip or the DROS can be integrated together with the bias resistor and the sensor SQUID on one single chip.

4.2.3 Two-stage SQUID systems vs. commercial flux modulated electronics

In order to investigate the feasibility of a two-stage SQUID system based on a DROS, dc SQUIDs especially designed for the readout of a CCC [31] were measured both by using a commercial Conductus [35] SQUID controller based on ac flux modulation and in a two-stage setup by a DROS with direct voltage readout [14]. A scheme of the latter configuration is shown in Fig. 4.5. In this section, the results of the measurements performed on a dc SQUID with an inductance of $L_{sq,1} = 100$ pH are discussed.

The SQUIDs were characterized at 4.2 K in an electromagnetic shield of Nb. All wires between the chips and the room temperature electronics were low pass filtered to prevent degradation due to radio frequency interference (RFI). The designed white flux noise of the dc SQUID was $\sqrt{S_{\Phi,1}} = 1.2\ \mu\Phi_0/\sqrt{\text{Hz}}$. The Josephson junctions had a critical current of $I_{0,1} \approx 17\ \mu$A and the junction hysteresis was removed by shunt resistors of $R = 2\ \Omega$. The flux-to-voltage transfer was 70 $\mu\text{V}/\Phi_0$. An HP 3562A spectrum analyzer was used to record the flux noise spectra. Using the Conductus electronics, the white flux noise was measured to be 4.3 $\mu\Phi_0/\sqrt{\text{Hz}}$, see trace (a) in Fig. 4.6. This is much larger than the design value.

The same dc SQUID was measured in a two-stage setup using a DROS with a gradiometric "figure-8" layout [29] as the second stage. The SQUID inductance was $L_{sq,2} = 550$ pH and the screening parameter was $\beta_{L,2} = 1.2$, as was also discussed in section 4.1.4. On top of the double washer of the DROS, a 2 x 25-turns input coil with an inductance of $L_{in,2} = 150$ nH and a mutual inductance with the DROS of $M_{in,2} = 6.7$ nH was deposited. The measured flux noise of this DROS was 7.7 $\mu\Phi_0/\sqrt{\text{Hz}}$ and the flux-to-voltage transfer was $\partial V/\partial\Phi_{2nd} \approx 2$ mV/Φ_0. This DROS was glued on a PCB together with the dc SQUID to form a non-integrated two-stage SQUID system. The sensor SQUID was biased at a constant voltage by

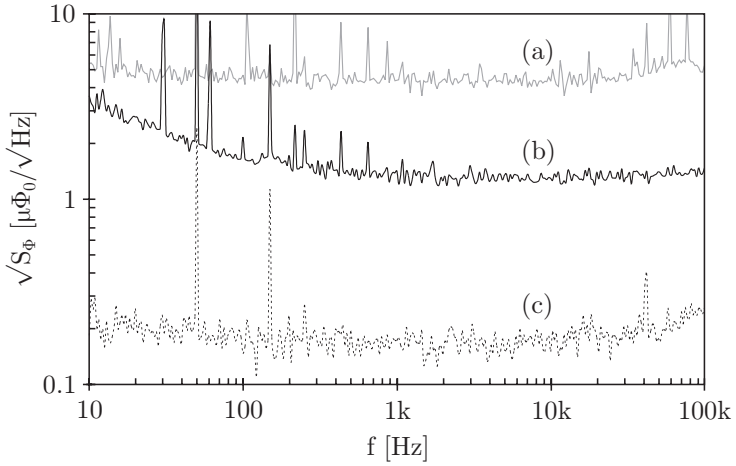

Fig. 4.6 Flux noise spectra of a dc SQUID measured (a) with Conductus electronics, which is based on ac flux modulation and (b) with a DROS as a cryogenic preamplifier and in direct voltage readout mode without flux modulation. Trace (c) represents the equivalent noise contribution of the room temperature preamplifier, $\sqrt{S_{V,amp}}/(\partial V/\partial \Phi_{sig})$, in the two-stage setup. The design value of the white flux noise of the SQUID was $\sqrt{S_{\Phi,1}} = 1.2\ \mu\Phi_0/\sqrt{\text{Hz}}$.

means of a small bias resistor with a resistance of $R_{bias} = 0.5\ \Omega$. At a bias current of $I_{b,1} = 110\ \mu\text{A}$, the flux gain was measured to be $G_\Phi \approx 56$ and the flux-to-voltage transfer was 12 mV/Φ_0 at the working point $\Phi_{sig} = (1/4 + \text{n}/2)\Phi_0$. The flux noise of this non-integrated two-stage SQUID system was $\sqrt{S_\Phi} = 1.3\ \mu\Phi_0/\sqrt{\text{Hz}}$, see trace (b) in Fig. 4.6. Because of the very large flux-to-voltage transfer, it can be concluded that the overall flux noise was completely determined by the intrinsic flux noise of the sensor SQUID and not by the noise contributions of the DROS and the readout electronics. Consequently, the measured flux noise in flux locked loop is very close to the design value of the intrinsic flux noise of the dc SQUID.

In conclusion, using the Conductus SQUID electronics the system sensitivity was limited by the electronics and not by the SQUID[ii]. The voltage noise of the preamplifier of the electronics is about 1 $\text{nV}/\sqrt{\text{Hz}}$. A room temperature 1:25 transformer is used, so the voltage noise referred to the input of the matching transformer is around 40 $\text{pV}/\sqrt{\text{Hz}}$. For the dc SQUID that was used above, this corresponds to an equivalent flux noise of 0.6 $\mu\Phi_0/\sqrt{\text{Hz}}$. However, also other parts of the electronics, e.g. the multiplier and the feedback circuit, introduce additional noise. All these noise contributions of the Conductus electronics add and together they dominate the overall system noise. In the two-stage SQUID system however, the intrinsic noise of the dc SQUID is amplified by the DROS, such that the DROS and readout electronics do not limit the system sensitivity but the dc SQUID determines the overall system noise. Therefore, compared to Conductus electronics, the two-stage SQUID system showed considerable performance improvement.

[ii] Comparable results were achieved using commercial ac flux modulated electronics available from Oxford Instruments and NKT. These SQUID controllers also limited the overall system sensitivity.

4.3 Design and fabrication of integrated two-stage SQUID systems

Based on the promising results that were achieved using non-integrated two-stage SQUID systems, fully integrated two-stage SQUID systems were designed, i.e. the sensor SQUID, the second stage SQUID (DROS) and the bias resistor were integrated on one single chip. Several integrated two-stage SQUID systems were designed for different applications, e.g. for the readout of a CCC, gravitational wave detectors and cryogenic particle detectors. In this section, only the design and the fabrication of the basic integrated two-stage SQUID systems are discussed.

In the fabrication process of the integrated two-stage SQUID systems, the definition of the Nb/Al,AlO_x/Al/Nb Josephson junctions was performed by reactive ion etching (RIE) in an SF_6 plasma, whereas all other structures, i.e. the 300 nm SiO_2 insulating layer, the Pd resistors and the Nb wiring, were pattered using the lift-off technique. The fabrication process as used at the University of Twente is described in detail in section 5.4.3.

4.3.1 The sensor SQUID

The sensor SQUID, a conventional resistively shunted dc SQUID, consists of a washer with a hole diameter of 77 μm, which corresponds to a hole inductance of $L_{h,1}$ = 120 pH. The inductance of the double 5-μm-wide and 231-μm-long slit is estimated to be $L_{t,1} \approx 80$ pH [36], thus the total SQUID inductance is $L_{sq,1} \approx 200$ pH. The 4 x 4 μm^2 Josephson junctions have a critical current of 5.5 to 6 μA each, which means that the screening parameter of the sensor SQUID is $\beta_{L,1} \approx 1.1$. The estimated junction capacitance is 0.48 pF. In order to remove the junction hysteresis, each junction is shunted with a resistor of $R = 7\ \Omega$. This corresponds to a McCumber parameter of $\beta_{C,1} = 0.4$. To avoid L-C resonances between the SQUID inductance and the capacitances of the Josephson junctions, a damping resistor of $R_{w,1} = 14\ \Omega$ is placed across the SQUID washer. This value is a trade-off between sufficient damping and an acceptable additional thermal noise.

At 4.2 K, the white flux noise of the sensor SQUID was designed to be $\sqrt{S_{\Phi,1}} = 1.2\ \mu\Phi_0/\sqrt{\text{Hz}}$, which corresponds to an energy resolution of $\varepsilon_1 = S_{\Phi,1}/2L_{sq,1} = 23\ h$. A 28-turns input coil of $L_{in,1} \approx 115$ nH was deposited on top of the sensor SQUID washer. The mutual inductance between this input coil and the sensor SQUID was measured to be $M_{in,1} = 4.2$ nH. A 1/3–turn feedback coil at the outside of the washer can be used to apply the feedback flux. The coupling with the SQUID was measured to be $M_{fb,1} = 61$ pH.

4.3.2 The second stage SQUIDs

The second stage SQUIDs are based on the DROSs that were designed by Van Duuren *et al.* [29] at the University of Twente. Two different DROSs, labeled A and B, with a gradiometric "figure-8" layout and a reference junction were used.

The inductance of the signal SQUID of the DROS A was measured to be $L_{sq,2} = 550$ pH. The critical current of each 2 x 4 μm^2 Josephson junction of the signal SQUID is 2 to 2.5 μA, corresponding to a screening parameter of $\beta_{L,2} \approx 1.2$. The estimated capacitance of these junctions is 0.24 pF. A 2 x 6 μm^2 Josephson

junction was used as reference junction. This reference junction was dimensioned to have a critical current in the middle of the critical current modulation range of the signal SQUID. On top of the double washer of the DROS, a 2 x 25-turns input coil was deposited, with an inductance of $L_{in,2} \approx 150$ nH and with a mutual inductance with the DROS of $M_{in,2} = 6.7$ nH. A single-turn feedback coil with $M_{fb,2} = 220$ pH can be used to apply the feedback flux or a flux bias, when the DROS is measured separately or in two-stage setup, respectively.

The signal SQUID inductance of DROS B is $L_{sq,2} = 490$ pH and the mutual inductance between the 2 x 19-turns input coil and the SQUID was measured to be $M_{in,2} = 4.7$ nH. The inductance of the input coil had a design value of $L_{in,2} = 87$ nH.

In both designs of the DROSs, the signal SQUID and the reference junction are shunted with an inductor $L_{sh} = 2.1$ nH and a resistor $R_{sh} = 2\ \Omega$, corresponding to a relaxation oscillation frequency of about 1 GHz. The white flux noise of DROS A at 4.2 K was expected to be $\sqrt{S_{\Phi,2}} = 6\ \mu\Phi_0/\sqrt{\text{Hz}}$ [29] and the noise of DROS B was expected to have a similar value. To prevent resonances between the shunt inductance and the SQUID capacitance, each junction of the signal SQUID is shunted with a resistor of 47 Ω. This implies a McCumber parameter of $\beta_{C,2} = 3$, such that the junction hysteresis is not removed. The L-C resonances between the SQUID inductance and the capacitance of the junctions are damped by a damping resistor of $R_{w,2} = 7\ \Omega$.

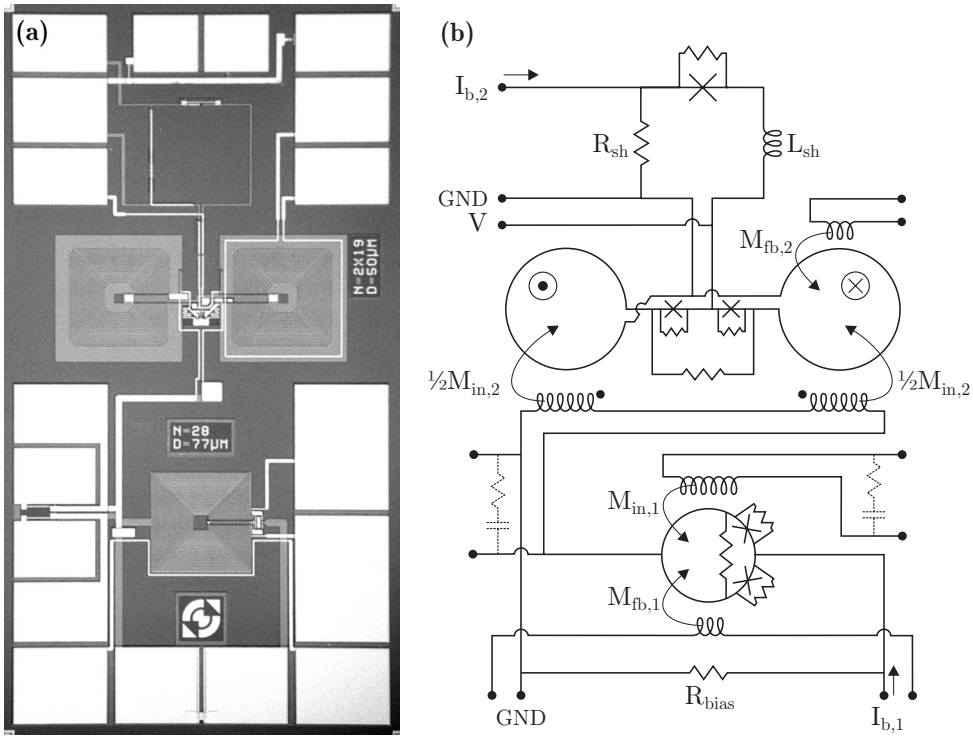

Fig. 4.7 (a) Micrograph and **(b)** scheme of the integrated two-stage SQUID system based on a DROS with reference junction as the second stage. The dotted input coil shunts are not on-chip integrated. The actual chip size including the bonding pads is 2.2 x 4 mm^2.

Table 4.1 Parameters of the integrated two-stage SQUID systems.

Electrical parameter	Sensor SQUID	DROS A	DROS B
L_{sq} [pH]	200 [b)]	550 [b)]	490 [b)]
$I_{c,max} = 2I_0$ [μA]	11-12 [b)]	4-5 [b)]	4-5 [b)]
$\beta_L = 2I_0L_{sq}/\Phi_0$	1.1	1.2	1.1
R [Ω]	7 [b)]	47 [a)]	47 [a)]
C_j [pF]	0.48 [a)]	0.24 [a)]	0.24 [a)]
$\beta_C = 2\pi I_0R^2C_j/\Phi_0$	0.4	3	3
L_{in} [nH]	115 [a)]	150 [b)]	87 [a)]
M_{in} [nH]	4.2 [b)]	6.7 [b)]	4.7 [b)]
$\sqrt{S_\Phi}$ [$\mu\Phi_0/\sqrt{Hz}$]	1.2 [a,b)]	6 [b)]	6 [b)]
$\varepsilon = S_\Phi/2L_{sq}$ [h]	24	$2.1 \cdot 10^2$	$2.4 \cdot 10^2$
$\partial V/\partial\Phi$ [mV/Φ_0]	0.1 [b)]	0.4 [b)]	0.4 [b)]

[a)] Design/calculated value.
[b)] Experimental value.

4.3.3 Layout of the integrated two-stage SQUID systems

In the integrated two-stage SQUID systems, the sensor SQUID is biased at a constant voltage by means of a bias resistor with a resistance of $R_{bias} = 0.5$ Ω. This means that the bias resistance is 7 % of the shunt resistance. Based on the expected noise values of the sensor SQUID and the DROSs and if we require that $p = 5$ %, the flux gain should be at least 22 [from Eq. (4.5)][iii]. According to Eq. (4.6), the maximum available flux gain when using DROS A is $G_\Phi = 36$. The theoretical cut-off frequency of the first stage is $f_{c,1} = 5$ MHz. For the two-stage SQUID systems based on DROS B, the maximum available flux gain is $G_\Phi = 26$ and due to the smaller input coil inductance of the second stage, the cut-off frequency of the first stage is larger, i.e. $f_{c,1} = 9$ MHz. In both cases, the available flux gain is larger than the required flux gain of 22, such that the overall noise of the two-stage SQUID systems is expected to be determined by the intrinsic noise of the sensor SQUID.

Figure 4.7 shows a micrograph and the corresponding schematic overview of the layout of an integrated two-stage SQUID system based on DROS B. The actual size of the chip including the bonding pads is 2.2 x 4 mm^2. The layout of the two-stage SQUID systems based on DROS A is similar. In order to minimize parasitic coupling between the sensor SQUID and the DROS, the design was made as symmetric as possible and the DROS has a gradiometric layout. To minimize the parasitic inductance of the wires between the sensor SQUID and the DROS, these wires are placed on top of each other, separated by the 300 nm thick insulating SiO_2 layer. The parasitic capacitance related to this configuration is much smaller than the SQUID capacitance and can thus be neglected. The important parameters of the integrated two-stage SQUID systems are summarized in Table 4.1.

[iii] In this case, we have chosen $p = 5$ % such that the overall system sensitivity is determined by the sensor SQUID. Obviously, for larger values of p the noise contribution of the second stage increases.

4.4 Experimental characteristics of integrated two-stage SQUIDs

From the test structures that were characterized, it was concluded that the critical current density, $J_c \approx 35$ A/cm^2, and the sheet resistance, $R_\square = 1.2\ \Omega$, agreed with the design values, $J_c = 32$ A/cm^2 and $R_\square = 1.0\ \Omega$. In this section, the experimental characteristics of the integrated two-stage SQUID systems are discussed, starting with the sensor SQUID and the second stage SQUIDs.

4.4.1 Sensor SQUID and second stage SQUIDs

Separate sensor SQUIDs were characterized using standard homemade battery powered *I-V* electronics. The SQUIDs were electromagnetically shielded by a Nb can and all wires between the chips and the room temperature electronics were low pass filtered to prevent radio frequency interference (RFI). Moreover, the cryostat was surrounded by a cylindrical μ-metal shield at room temperature. Since connecting an external R_{in}-C_{in} shunt across the input coil improved the noise characteristics and the flux-to-voltage transfer [6], such an input coil shunt was implemented with surface mounted devices (SMD). This R_{in}-C_{in} shunt effectively damps microwave resonances in the input coil [37,38]. The best results were achieved with $R_{in} \approx 50\ \Omega$ and $C_{in} = 1$ nF.

Figure 4.8 shows the experimental *I-V* characteristics of a sensor SQUID. The flux was swept via the feedback coil. At the optimum bias current, $I_{b,1} \approx 12$ μA, the flux-to-voltage transfer was ~100 μV/Φ_0. Similarly to the measurements described in section 4.2.3, the sensor SQUID was characterized in FLL using a commercial Conductus SQUID controller based on ac flux modulation. The white noise level was measured to be $\sqrt{S_\Phi} = 3.8\ \mu\Phi_0/\sqrt{\text{Hz}}$, which is much larger than the design value of $1.2\ \mu\Phi_0/\sqrt{\text{Hz}}$. Trace (a) in Fig. 4.14, page 75, shows the typical experimental flux noise spectrum of a sensor SQUID. The large white noise level is caused by the electronics and not by the SQUID, as is discussed in section 4.4.4.

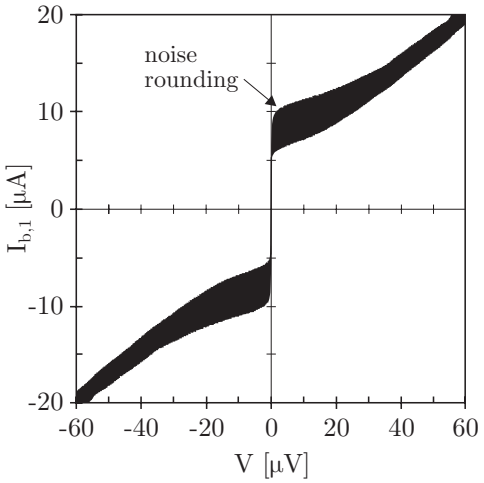

Fig. 4.8 Experimental current vs. voltage (*I-V*) characteristics of a sensor SQUID at 4.2 K. The flux was swept via the feedback coil.

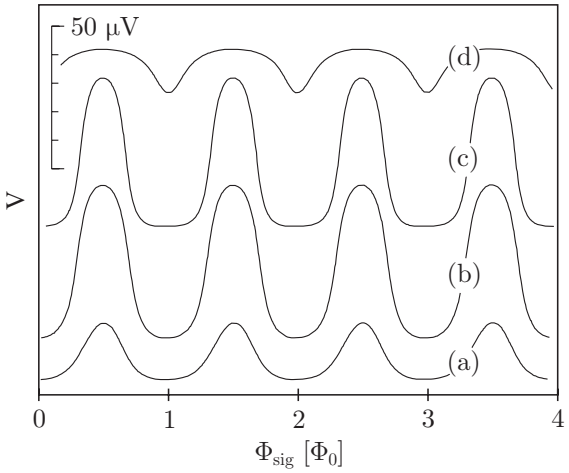

Fig. 4.9 Typical experimental V-Φ_{sig} characteristics of a DROS B, for different bias currents. For trace (a), the bias current was $I_{b,2}$ = 10 μA, for trace (b) 31 μA, for trace (c) 52 μA and for trace (d) 93 μA. The vertical offsets are arbitrary.

Figure 4.9 shows the experimental V-Φ_{sig} characteristics of a separate gradiometric DROS B for different values of the bias current. In these measurements, the flux was applied via the feedback coil and the input coil was shunted with an R-C circuit of R_{in} = 50 Ω and C_{in} = 1 nF. The optimum bias current was around 50 μA for both the DROSs A and the DROSs B. The flux-to-voltage transfer of both types of DROSs ranged from 0.2 to 0.4 mV/Φ_0, which is smaller than the flux-to-voltage transfer functions of similar DROSs, 0.7 to 1 mV/Φ_0, reported in ref. [29]. This discrepancy can be attributed to rounding off of the Josephson junctions. Due to rounding off, the effective area of the Josephson junctions decreases. Obviously, this effect is the largest for the smallest junctions, as was experimentally confirmed by measurements on separate test junctions[iv]. Consequently, the critical current of the 2 x 6 μm^2 reference junction is no longer in the middle of the critical current modulation range of the signal SQUID, which causes the flux-to-voltage transfer to decrease. Due to a different fabrication process of the photomasks of the DROSs reported in ref. [29], the effect of rounding off was smaller for these DROSs.

For the DROSs, both type A and type B, with a flux-to-voltage transfer of ~0.4 mV/Φ_0, the flux noise was measured to be ~6 $\mu\Phi_0/\sqrt{\text{Hz}}$. However, for flux-to-voltage transfer functions of 0.2 to 0.4 mV/Φ_0, the noise contribution of the room temperature amplifier cannot be neglected anymore, e.g. for a flux-to-voltage transfer of 0.2 mV/Φ_0, the amplifier input voltage noise of 1.8 $\text{nV}/\sqrt{\text{Hz}}$ corresponds to an equivalent flux noise of 9 $\mu\Phi_0/\sqrt{\text{Hz}}$. Thus, it can be concluded that the intrinsic flux noise of both types of DROSs is smaller than 6 $\mu\Phi_0/\sqrt{\text{Hz}}$.

[iv] Separate 2 x 4 μm^2 and 4 x 4 μm^2 Josephson junctions were characterized. The measured critical current ratio was $I_{0,4x4}/I_{0,2x4} \approx 2.6$. Without rounding off, the ratio should be 2.0. It can be calculated that both the width and the length of the junctions are effectively ~0.75 μm smaller than expected.

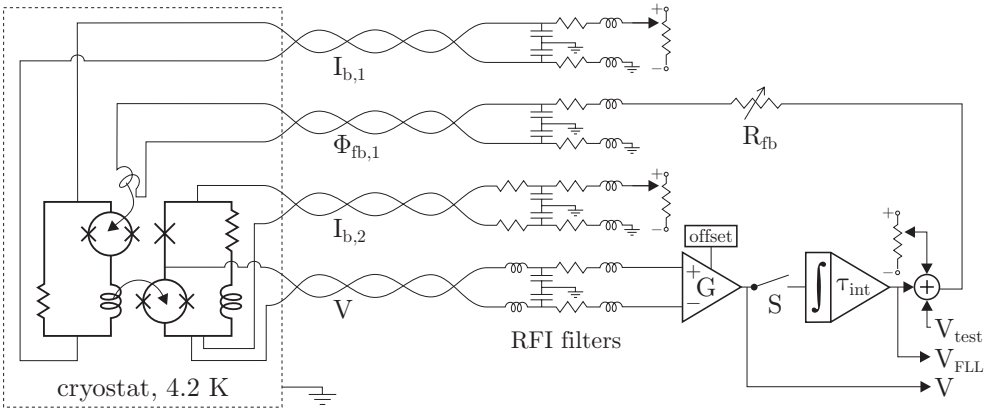

Fig. 4.10 Scheme of the measurement setup for the characterization of the two-stage SQUID systems both in open loop and in flux locked loop. For simplicity, the flux bias that can be applied to the DROS and the resistors on the PCB are not shown.

4.4.2 Measurement setup for integrated two-stage SQUID systems

For the characterization of the integrated two-stage SQUID systems, the chips were glued on an epoxy printed circuit board (PCB) with GE-7031 varnish. The electrical contacts between the PCB and the chip were made by ultrasonic bonding of 25 µm thick Al wires. The shielding of the samples is the same as in the experiments on the separate sensor SQUIDs and the DROSs. An R_{in}-C_{in} shunt of $R_{in} = 68\ \Omega$ and $C_{in} = 1$ nF was connected across the input coil of the sensor SQUID and the input coil of the second stage was shunted with $R_{in} = 50\ \Omega$ and $C_{in} = 1$ nF to damp possible microwave resonances in the input coils.

The measurement setup that was used for the characterization of the integrated two-stage SQUID systems is shown in Fig. 4.10. Besides RFI filters at room temperature, additional (filter) resistors were placed on the PCB in the wires of the bias current of the first stage and the feedback flux lines. For simplicity, these additional resistors are not shown in the schematic overview. The cut-off frequency of the filters in the voltage readout lines was about 1 MHz, whereas the filters in the wires for the bias currents had a cut-off frequency below 25 kHz.

The measurements were performed using homemade electronics, originally developed for the readout of DROSs [29]. In this setup, the output voltage of the two-stage SQUID system is directly measured by a differential room temperature preamplifier based on LT1028 op-amps [39]. The gain of the preamplifier is adjustable between $G = 2{\cdot}10^2$ to $2{\cdot}10^5$. The white input voltage noise is $\sqrt{S_{V,amp}} = 1.8$ nV/$\sqrt{\text{Hz}}$ and the white current noise is $\sqrt{S_{I,amp}} = 2$ pA/$\sqrt{\text{Hz}}$. By using copper wiring and low-ohmic RFI filters for the voltage readout lines, the noise contribution of $\sqrt{S_{I,amp}}$ was negligible.

In FLL mode, i.e. switch S closed, the output of the preamplifier is connected to an integrator with a time constant of $\tau_{int} = 10^{-2}$, 10^{-3} or 10^{-4} s. The integrator supplies a feedback current via an adjustable feedback resistor R_{fb}, which means that the flux locked loop transfer function $\partial V_{FLL}/\partial\Phi_{sig} = R_{fb}/M_{fb,1}$ can be adjusted.

Via the feedback coil of the sensor SQUID, the feedback current is converted to the feedback flux. In order to lock the system to the optimum working point, a flux bias can be applied to the sensor SQUID by adding an offset voltage to the integrator output. For testing purposes, also a test signal V_{test} can be added to the output of the integrator. For simplicity, the flux bias that can be added to the second stage is not shown in the scheme of the measurement setup. With the switch S opened, V_{test} can be used to record the open loop V-Φ_{sig} characteristics of the two-stage SQUID systems and with switch S closed, V_{test} can be used to check the proper operation of the FLL. Moreover, since both the test signal and the feedback flux are applied via the same resistor R_{fb}, V_{test} can be used to adjust the flux locked loop transfer function in open loop.

4.4.3 V-Φ characteristics of integrated two-stage SQUID systems

Figure 4.11 shows the measured V-Φ_{sig} characteristics of one of the integrated two-stage SQUID systems with DROS A as the second stage. Multiple modulation periods in the flux-to-voltage characteristic of the second stage occur for only one modulation period in the first stage, caused by the flux gain. The second stage was biased at a current $I_{b,2} = 54$ μA. The bias current of the first stage and thus the bias voltage of the sensor SQUID was varied. The maximum voltage modulation

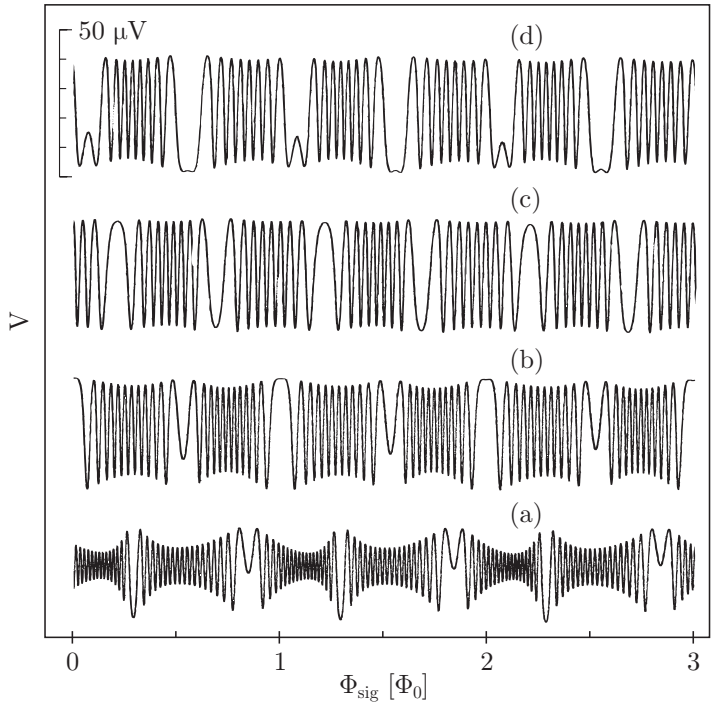

Fig. 4.11 Experimental V-Φ_{sig} characteristics of an integrated two-stage SQUID system with DROS A as the second stage for different bias currents of the first stage. For trace (a) the bias current was $I_{b,1} = 50$ μA, for trace (b) 100 μA, for trace (c) 150 μA and for trace (d) 180 μA. The bias current of the second stage was fixed at $I_{b,2} = 54$ μA.

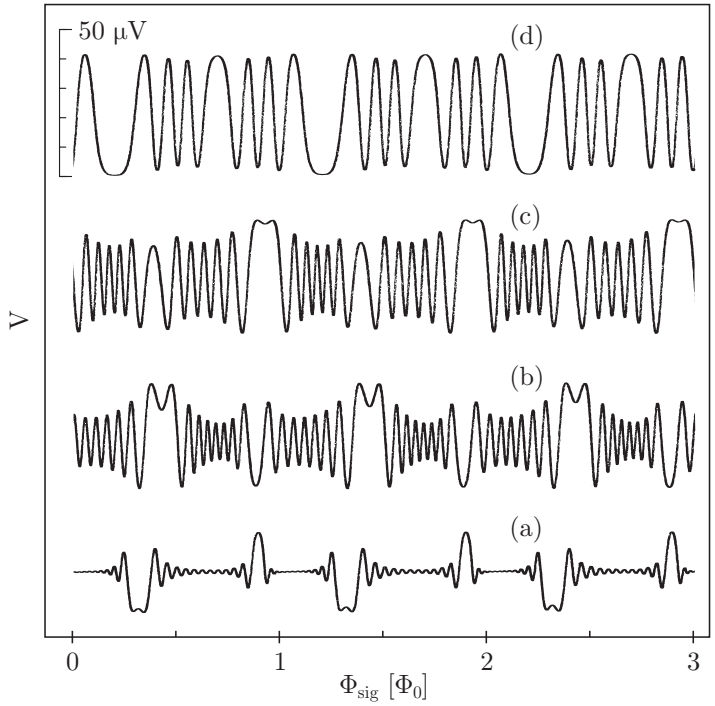

Fig. 4.12 Experimental V-Φ_{sig} characteristics of an integrated two-stage SQUID system with DROS B as the second stage for different bias currents of the first stage. For trace (a) the bias current was $I_{b,1}$ = 50 μA, for trace (b) 100 μA, for trace (c) 150 μA and for trace (d) 180 μA. The bias current of the second stage was fixed at $I_{b,2}$ = 53 μA.

depth was about 40 μV and the maximum flux-to-voltage transfer was ~3.6 mV/Φ_0 at $I_{b,1}$ = 80 μA.

The actual flux gain depends on the bias voltage of the sensor SQUID. The higher the bias voltage, the lower the modulation depth of the current through the sensor SQUID ΔI_1 and the lower the flux gain. At low bias voltages, the designed maximum flux gain could be achieved. Moreover, the flux gain depends on the applied flux. The flux gain is maximum at the working point $\Phi_{sig} = (1/4 + n/2)\Phi_0$. At that point, the largest amount of wideband flux noise is coupled from the sensor SQUID to the second stage, which can cause the voltage modulation depth of the DROS to decrease somewhat as is shown in the V-Φ_{sig} characteristics. This effect was also observed by Kirichenko *et al.* in ref [11].

Figure 4.12 shows the experimental V-Φ_{sig} characteristics of one of the two-stage SQUID systems based on DROS B. Also in these measurements, the DROS was biased at a constant current, $I_{b,2}$ = 53 μA, and the bias current of the first stage was varied. For these wideband two-stage SQUID systems with a designed cut-off frequency of the first stage of $f_{c,1}$ = 9 MHz, the reduction of the voltage modulation depth was larger than for the systems based on DROS A with $f_{c,1}$ = 5 MHz. Because of the decreased voltage modulation depth and the smaller flux gain compared to the two-stage SQUID systems based on DROS A, the flux-to-voltage transfer of the systems based on DROS B was only ~1.7 mV/Φ_0. Figure 4.13 shows

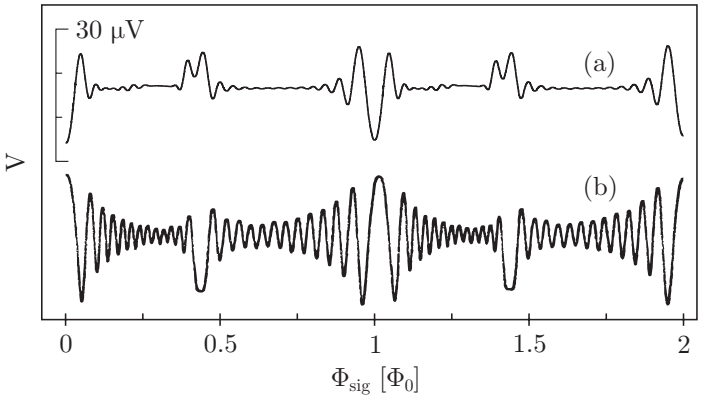

Fig. 4.13 Experimental V-Φ_{sig} characteristics of an integrated two-stage SQUID system with DROS B (a) without and (b) with additional inductance in the first stage. The bias current of the first stage was $I_{b,1} = 50$ μA and the bias current of the second stage was $I_{b,2} = 50$ μA.

the V-Φ_{sig} characteristics of a two-stage SQUID system based on DROS B with, trace (b), and without, trace (a), an inductance of $3L_{in,2}$ added to the first stage. The additional inductance decreased the cut-off frequency of the first stage from 9 MHz to 2 MHz [from Eq. (4.8)]. As a result, the distortion of the DROS characteristics is reduced and the voltage modulation depth of the two-stage SQUID system is increased. This justifies the conclusion that the reduction of the voltage modulation depth is caused by wideband flux noise coupled from the sensor SQUID to the second stage.

The V-Φ_{sig} characteristics of both types of integrated two-stage SQUID systems show some asymmetry. This is probably caused by a small "APF effect" due to parasitic coupling between the input coil of the second stage and the sensor SQUID. In the experiments on non-integrated two-stage SQUID systems, this effect was not observed, see Fig. 4.3, because of the large distance between the sensor SQUID and the second stage.

4.4.4 Noise of integrated two-stage SQUID systems

The noise spectrum of the two-stage SQUID system with DROS A as the second stage measured in FLL at 4.2 K is shown in Fig. 4.14. By applying a flux bias to the sensor SQUID and the second stage, the system was locked to the optimum working point. The bias current of the first stage was $I_{b,1} = 80$ μA and the second stage was biased at $I_{b,2} = 54$ μA. The white flux noise level is $\sqrt{S_\Phi} = 1.3$ $\mu\Phi_0/\sqrt{\text{Hz}}$, corresponding to an energy resolution of $\varepsilon = 27$ h. This corresponds to a white current noise referred to the input coil of the sensor SQUID of 0.64 pA/$\sqrt{\text{Hz}}$. The experimental flux noise level agrees with the theoretical white flux noise of the sensor SQUID, 1.2 $\mu\Phi_0/\sqrt{\text{Hz}}$, which means that the system sensitivity of the two-stage SQUID systems is indeed determined by the sensor SQUID and not by the second stage or the room temperature readout electronics. The 1/f corner frequency is about 50 Hz and at 1 Hz the flux noise is $\sqrt{S_\Phi} \approx 9$ $\mu\Phi_0/\sqrt{\text{Hz}}$.

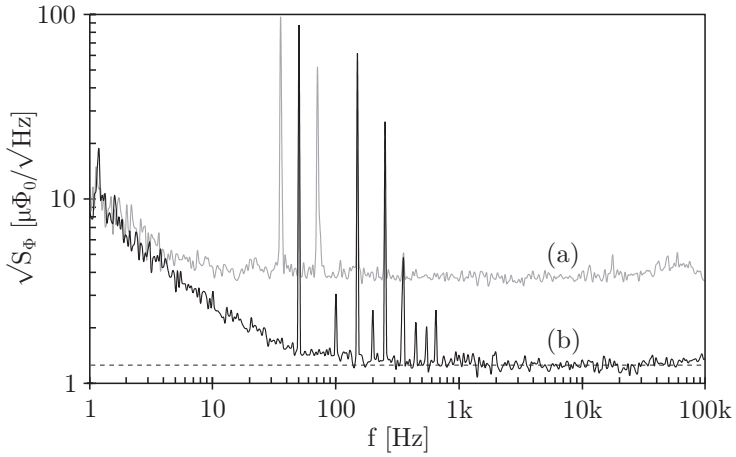

Fig. 4.14 Trace (a): Flux noise spectrum of a sensor SQUID measured with Conductus electronics, which is based on ac flux modulation. Trace (b) represents the overall flux noise spectrum of an integrated two-stage SQUID system based on DROS A. The design value of the white flux noise of the sensor SQUID was $\sqrt{S_{\Phi,1}} = 1.2\ \mu\Phi_0/\sqrt{\text{Hz}}$.

Trace (a) represents the flux noise of a separate sensor SQUID in FLL using the Conductus SQUID controller. As was discussed in section 4.4.1, the white flux noise level using Conductus electronics was $\sqrt{S_\Phi} = 3.8\ \mu\Phi_0/\sqrt{\text{Hz}}$. As for the non-integrated two-stage SQUID system described in section 4.2.3, also in this case the noise of the Conductus electronics dominated the overall system noise and the intrinsic noise level of the sensor SQUID could not be measured. The 1/f noise is the same for the two-stage SQUID system and the separate sensor SQUID characterized using the Conductus controller. This suggests that the 1/f noise is either intrinsic noise of the sensor SQUID or external noise but it is not caused by the readout electronics or the second stage.

The total white flux noise level of the two-stage SQUID system with DROS B was somewhat larger, $\sqrt{S_\Phi} = 2.1\ \mu\Phi_0/\sqrt{\text{Hz}}$. In that case, the noise contribution of the readout electronics was larger than for the two-stage SQUID systems with DROS A. This is caused by the smaller flux-to-voltage transfer due to the smaller flux gain of this system and the reduction in the voltage modulation depth.

4.4.5 Bandwidth of integrated two-stage SQUID systems

The readout electronics that was used for the characterization of the two-stage SQUID systems described above is based on a differential room temperature preamplifier with a bandwidth of about 250 kHz. In order to increase the bandwidth of DROSs and two-stage SQUID systems in FLL, wideband readout electronics based on direct voltage readout was developed [40,41]. The output voltage of the two-stage SQUID system is amplified by a non-differential room temperature preamplifier based on an AD797 op-amp [42] with a gain $G = 10$ and a white input voltage noise of 1.1 $\text{nV}/\sqrt{\text{Hz}}$. The integrator, also based on an AD797 op-amp, has a time constant of $\tau_{int} = 12$ ns. The usable bandwidth of the FLL electronics is

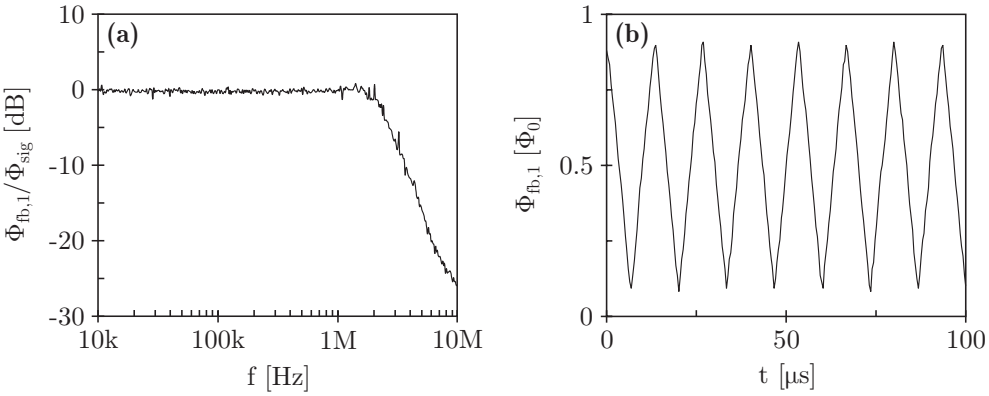

Fig. 4.15 (a) Closed loop gain, $\Phi_{fb,1}/\Phi_{sig}$, as a function of the frequency of an integrated two-stage SQUID system based on DROS A. **(b)** Feedback flux measured in time, from which the slew rate was calculated to be $1.3{\cdot}10^5$ Φ_0/s.

about 3 MHz. The feedback resistance is fixed at R_{fb} = 10 kΩ. Since a non-differential preamplifier is used, the two-stage SQUID system is biased with a symmetric current source.

Using the fast FLL electronics for the readout of the integrated two-stage SQUID system based on DROS A, we have achieved a –3 dB bandwidth of 1.0 MHz. For these measurements, the same two-stage SQUID system was used as for the measurements shown in Fig. 4.11, i.e. $\partial V/\partial\Phi_{sig} \approx 3.6$ mV/Φ_0. The measured bandwidth is close to the value calculated from Eq. (4.9), $f_{max} \approx 1.4$ MHz, but it is well below the cut-off frequency of the first stage, $f_{c,1} = 5$ MHz.

The measurements described above imply that the bandwidth of the two-stage SQUID systems in closed loop can be increased following the suggestions made in section 4.1.3. By decreasing the feedback resistance from 10 to 1 kΩ, the –3 dB bandwidth was increased to 2.5 MHz. Figure 4.15a shows the frequency response of the same integrated two-stage SQUID system measured in FLL with R_{fb} = 1 kΩ. The frequency response was recorded using an HP 4194A impedance/gain-phase analyzer. Because of the limited bandwidth of the FLL electronics, larger bandwidths could not be achieved. The maximum flux slew rate of the two-stage SQUID system operating in FLL was measured to be $1.3{\cdot}10^5$ Φ_0/s, see Fig. 4.15b. This corresponds to the value that can be calculated from the measured linear flux range $2\delta\Phi$ = 13 mΦ_0 and the experimental bandwidth in FLL using Eq. (4.10), $\partial\Phi_{sig}/\partial t = 2\pi\delta\Phi f_{max} = 1.1{\cdot}10^5$ Φ_0/s.

The bandwidth of a two-stage SQUID system in FLL can also be increased by increasing the mutual inductance between the feedback coil and the sensor SQUID. Therefore, two-stage SQUIDs with a larger $M_{fb,1}$ were fabricated. For these systems, the mutual inductance was increased from $M_{fb,1}$ = 61 pH to $M_{fb,1}$ = 340 pH and all other parameters were the same as for the two-stage SQUID systems based on DROS A. Due to rounding off of the Josephson junctions and a fabrication problem, the flux-to-voltage transfer was only ~0.7 mV/Φ_0. For R_{fb} = 10 kΩ, the measured bandwidth in FLL was 1.5 MHz, which agrees with the value calculated from Eq. (4.9).

4.5 Conclusion and discussion

In the first section of this chapter, the operation principle of the two-stage SQUID system was discussed and it was shown that a SQUID can be used as a very low-noise cryogenic preamplifier for a sensor SQUID. In section 4.2, it was shown that a two-stage SQUID system leads to considerable performance improvement compared to commercial ac flux modulated electronics. Moreover, the large flux-to-voltage transfer of a two-stage SQUID system allows a direct voltage readout mode without flux modulation. For the SQUID with an inductance of $L_{sq,1} = 100$ pH that was characterized in that section, the overall noise that was measured using a commercial flux modulated SQUID controller was 4.3 $\mu\Phi_0/\sqrt{\text{Hz}}$, whereas in a two-stage setup using a DROS as a cryogenic preamplifier, the overall noise was 1.3 $\mu\Phi_0/\sqrt{\text{Hz}}$, $\varepsilon = 55\ h$. In the latter case, the overall noise was very close to the theoretical flux noise of the sensor SQUID, 1.2 $\mu\Phi_0/\sqrt{\text{Hz}}$, and the sensitivity was not limited by the second stage or the readout electronics. The commercial SQUID controller however, limited the overall system sensitivity.

In section 4.3, the design of an integrated two-stage SQUID system with a DROS as the second stage was discussed. In this design, the sensor SQUID, the DROS and the bias resistor are integrated on one chip. The experiments on these SQUID systems, discussed in section 4.4, showed that the overall system sensitivity was determined by the sensor SQUID, as was expected. The experimental white flux noise in closed loop was 1.3 $\mu\Phi_0/\sqrt{\text{Hz}}$, $\varepsilon = 27\ h$, and flux-to-voltage transfer functions up to 3.6 mV/Φ_0 were measured. Also for these integrated two-stage SQUID systems, the sensitivity was completely determined by the sensor SQUID and not by the second stage or the readout electronics. Using wideband readout electronics based on direct voltage readout, a closed loop bandwidth of 2.5 MHz was achieved. The slew rate was measured to be $1.3{\cdot}10^5$ Φ_0/s. One of the possibilities to further improve the overall sensitivity of the two-stage SQUID systems is decreasing the area of the Josephson junctions. This is thoroughly discussed in chapter 6.

The first reported two-stage SQUID systems were based on a conventional dc SQUID as the second stage [9,43,44]. However, as was discussed in section 4.1.4, in principle any type of SQUID can be used for the second stage. Because of the small flux-to-voltage transfer and the small voltage modulation depth of conventional dc SQUIDs, the two-stage SQUID systems based on these SQUIDs either still require flux modulation [9] or they require a very large flux gain [11] or a very small SQUID inductance of the second stage [27]. Since flux modulation and a very large flux gain limit the measurement bandwidth and the reduction of the SQUID inductance may be limited by the photolithography, a conventional dc SQUID as the second stage limits the practical versatility.

In our case, we used a DROS as the second stage because of the large flux-to-voltage transfer and the large voltage modulation depth compared to conventional resistively shunted dc SQUIDs. The disadvantage of using a DROS is that the (large) flux gain from the first stage to the second stage leads to a reduced linear flux range. Using a series SQUID array [12], it is possible to make a design of a two-stage SQUID system without reducing the linear flux range. However, the required

coherent modulation in a series SQUID array results in practical complications, which favors the DROS as a second stage.

In a two-stage SQUID system, the flux gain has to be sufficiently large, such that the amplified flux noise of the sensor SQUID is much larger than the flux noise related to the second stage SQUID and the readout electronics. However, a large gain also requires a large mutual inductance between the second stage and its input coil. Thus a trade-off should be made between a low noise contribution of the second stage and the readout electronics on the one hand and a large intrinsic bandwidth on the other hand. In a two-stage SQUID system based on a series SQUID array, the total flux gain should be about equal to the number of SQUIDs, i.e. $G_\Phi \approx N$, which is generally much larger than the required flux gain for two-stage SQUID systems based on a DROS. Since the input noise of the series SQUID array increases with the number of SQUIDs, in many cases SQUIDs with rather small inductances are used. As a result, the inductance of the input coil of the second stage has to be quite large, which may result in a small intrinsic bandwidth. This undoes the advantage of the possible large linear flux range when using a series SQUID array as the second stage [45].

If we compare the measured characteristics of our integrated two-stage SQUID system with the experimental results that were reported for two-stage SQUID systems with a SQUID array as the second stage, we can conclude the following. Welty *et al.* [12] developed a two-stage SQUID system with a sensor SQUID inductance of $L_{sq,1} = 10$ pH and a series array of 100 SQUIDs as the second stage. The energy resolution in open loop was measured to be $\varepsilon = 30\ h$, after subtracting the noise of the room temperature preamplifier. In our systems based on DROS A, the preamplifier noise was negligible. Due to the large inductance of the input coil of the second stage, the intrinsic bandwidth of Welty's two-stage SQUID system was only 390 kHz, which is much smaller than the experimental FLL bandwidth, 2.5 MHz, of our integrated two-stage SQUID systems. New chips based on series SQUID arrays were designed with an energy resolution as high as $\varepsilon = 400\ h$ and an intrinsic bandwidth of about 2 MHz [46,47]. However, for both designs of the two-stage SQUID systems based on a SQUID array, the linear flux range was decreased because of a total flux gain of $G_\Phi > N$. Cantor *et al.* [13] reported on a design of a wideband two-stage SQUID system based on a series SQUID array with a designed cut-off frequency of the first stage of $f_{c,1} = 9.6$ MHz, but no experimental data are reported for this system. This is comparable to the designed cut-off frequency of the integrated two-stage SQUID systems based on DROS B, i.e. $f_{c,1} = 9$ MHz.

In conclusion, using a DROS as the second stage allows a simple design of a two-stage SQUID system with excellent noise characteristics and a large bandwidth in FLL. Further improvement of the bandwidth in FLL may be possible by improving the room temperature readout electronics. Moreover, the flux gain might be reduced to improve the linear flux range and the intrinsic bandwidth of the two-stage SQUID systems. This is for example useful when using the two-stage SQUID systems for the readout of cryogenic particle detectors and for other high-speed applications.

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Chapter 5

Smart DROSs

In the previous chapter, the two-stage SQUID system was discussed as a SQUID with an on-chip integrated low-noise preamplifier. Using this concept, SQUID systems with a large bandwidth can be achieved quite easily, without using complex readout electronics. A digital SQUID incorporates a SQUID and the complete FLL circuitry on one single chip, which allows even larger bandwidths and higher flux slew rates without affecting the intrinsic sensitivity of the SQUID [1,2]. Together with a low flux noise level, this makes the digital SQUID an outstanding candidate for the readout of cryogenic particle detectors or for applications in an unshielded environment [3]. Another important advantage is the possibility to use multiplexing for the readout of multiple digital SQUIDs at cryogenic temperatures without breaking the feedback loop [4,5].

Our concept of the digital SQUID, the Smart DROS, is based on a DROS and a superconducting up-down counter. In section 5.1, the operation principles of the DROS, the Josephson counter and the Smart DROS are presented. The Smart DROS concept was originally developed by Van Duuren *et al.* at the University of Twente [6]. The developed prototype showed the principle of operation, but the design was not optimized with respect to, e.g., the quantization unit of the feedback flux, the coupling scheme and the output range of the Josephson counter. In section 5.2, the optimization process is discussed and in section 5.3 the Smart DROS is numerically analyzed. Based on these numerical simulations, an optimized Smart DROS with a relaxation oscillation frequency of 100 MHz was designed and fabricated, as is described in section 5.4. The design was experimentally verified using low frequency and high frequency measurement techniques. These measurements are discussed in section 5.5.

5.1 Operation principle

Basically, the Smart DROS consists of a double relaxation oscillation SQUID (DROS) and a superconducting up-down counter, the Josephson counter [7]. The relaxation oscillations of the DROS serve as an on-chip clock signal, such that no external clock is required, which is an important advantage compared to other concepts of the digital SQUID. The DROS is used to transform the analog input signal, i.e. the signal flux Φ_{sig}, to the digital domain, whereas the Josephson counter is used to supply the feedback flux.

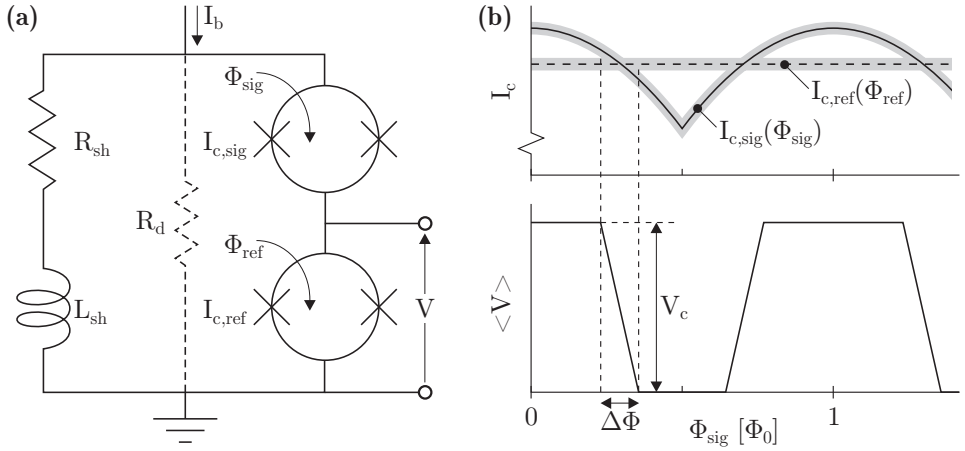

Fig. 5.1 (a) Scheme of a DROS with reference SQUID. An optional damping resistor R_d can be used to suppress parasitic resonances [1]. **(b)** I_c-Φ_{sig} characteristics of the signal SQUID and the reference SQUID and the $<V>$-Φ_{sig} curve of a DROS. The gray regions represent the thermal spreads in critical currents.

5.1.1 Double Relaxation Oscillation SQUIDs

As was discussed in section 2.2.1, the junctions of a conventional dc SQUID are shunted with low-ohmic resistors to remove the hysteresis. Consequently, the usable voltage swing and the flux-to-voltage transfer of a non-hysteretic dc SQUID are rather small. In order to improve the voltage swing and the flux-to-voltage transfer, the DROS has been developed. In section 2.3.2, the operation principle of the DROS was briefly discussed. In this section, the operation principle of the DROS is treated in more detail.

As is shown in Fig. 5.1a, a DROS consists of two hysteretic dc SQUIDs, which are connected in series and shunted with an external inductor L_{sh} and a resistor R_{sh}. The signal flux Φ_{sig} is applied to the signal SQUID and a constant reference flux Φ_{ref} is applied to the reference SQUID[i]. If the DROS is biased with an appropriate bias current I_b, relaxation oscillations are generated. The theoretical maximum bias current at which a DROS still operates is given by [8]

$$I_{b,max} = \frac{1}{R_{sh}} \sqrt{\frac{I_0 \Phi_0}{\pi C_{sq}}} \,. \tag{5.1}$$

Here, $C_{sq} = 2C_j$ is the SQUID capacitance and C_j is the capacitance of one junction. However, thermal fluctuations in the junctions can increase the maximum bias current at which a DROS can operate [1]. The output voltage of a DROS is the voltage across the reference SQUID. The time-averaged $<V>$-Φ_{sig} characteristic of a

[i] Instead of a reference SQUID, also a reference junction can be used. In that case, no reference flux is necessary, which reduces the number of wires from the chip to the room temperature electronics. The disadvantage of using a reference junction is that the critical current $I_{c,ref}$ cannot be tuned anymore.

DROS shows a large flux-to-voltage transfer at the points where $I_c(\Phi_{sig}) = I_{c,ref}$, as is shown in the lower part of Fig. 5.1b. Assuming a linear transition between the $<V> = 0$ and the $<V> = V_c$ state, the flux-to-voltage transfer can be expressed as

$$\frac{\partial V}{\partial \Phi_{sig}} = \frac{V_c}{\Delta\Phi}, \tag{5.2}$$

where $\Delta\Phi$ is the width of transition between the two states. At 4.2 K, the transition width is limited by thermal spreads in the critical currents of the signal SQUID and the reference SQUID, as is represented by the gray regions in the upper part of Fig. 5.1b. The maximum flux-to-voltage transfer at this temperature is given by [9,10]

$$\frac{\partial V}{\partial \Phi_{sig}} \approx g \frac{I_0^{2/3}}{1+\beta_{L,sig}} \frac{V_c}{\Phi_0}, \tag{5.3}$$

with $g \approx 7{\cdot}10^4$ A$^{-2/3}$, $\beta_{L,sig}$ the screening parameter of the signal SQUID and I_0 the critical current of one junction. Typical values for the maximum flux-to-voltage transfer are of the order of 1 mV/Φ_0. At the point where $I_c(\Phi_{sig}) = I_{c,ref}$, i.e. where the flux-to-voltage transfer is maximum, both SQUIDs have a switching probability of 50 %, which results in an output voltage noise of [9,10]

$$S_V = \frac{V_c^2}{4 f_{RO}}. \tag{5.4}$$

Combining Eqs. (5.3) and (5.4), the equivalent flux noise at 4.2 K can be written as

$$S_\Phi = \frac{S_V}{\left(\partial V / \partial \Phi_{sig}\right)^2} \approx \frac{1}{4g^2} \frac{\left(1+\beta_{L,sig}\right)^2 \Phi_0^2}{f_{RO} I_0^{4/3}}. \tag{5.5}$$

The characteristics of a DROS can be strongly affected by parasitic resonances between the shunt inductance L_{sh} and the SQUID capacitance C_{sq}. These resonances can be prevented by using an additional damping resistor R_d [11], as is shown in Fig. 5.1a. The damping resistor should be chosen such that the damping parameter [8]

$$D = \frac{L_{sh}}{4 C_{sq} R_d^2} \geq 1. \tag{5.6}$$

If this requirement is fulfilled, the system is overdamped and L-C resonances cannot occur, although numerical simulations have shown that for $D = 0.1$ the L-C resonances may be sufficiently suppressed [11]. However, the smaller the damping parameter, the higher the output voltage and the smaller the Johnson noise generated by the damping resistor. Thus a trade-off has to be made between sufficient damping of the resonances on the one hand and acceptable additional flux noise due to the Johnson noise of R_d and a high output voltage on the other hand.

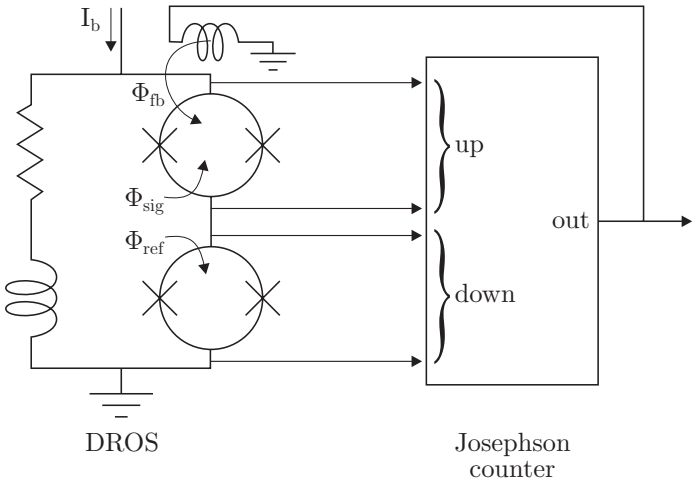

Fig. 5.2 Schematic overview of the Smart DROS.

5.1.2 The Smart DROS

The large flux-to-voltage transfer of the DROS is an important advantage when using room temperature FLL electronics based on direct voltage readout. On the other hand, the pulsed output of the DROS is particularly suited for digital readout schemes. The pulsed output opens the possibility to integrate the DROS and the complete (digital) FLL circuitry on one single chip.

In the Smart DROS, Fig. 5.2, the voltage pulses of the DROS serve as the input for a superconducting up-down counter, the so-called Josephson counter. The Josephson counter counts the effective number of voltage pulses, generated across the signal SQUID and the reference SQUID. The output of the counter is fed back to the signal SQUID, closing the flux locked loop and supplying the feedback flux Φ_{fb}. Thus the counter has the role of the integrator in the conventional FLL. Each relaxation oscillation of either the signal SQUID or the reference SQUID causes the feedback flux to increase or decrease respectively, by an amount of $\delta\Phi_{fb}$, the quantization unit of the feedback flux. The feedback loop automatically locks the system to the dynamic equilibrium where both the signal SQUID and the reference SQUID have a switching probability of 50 %, i.e. the point where $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$. In that point, both SQUIDs generate voltage pulses in turn. If the signal flux is changed, the system is forced out of its equilibrium and one of the SQUIDs starts generating voltage pulses. The feedback flux is changed by one quantization unit per relaxation oscillation cycle, until a new dynamic equilibrium has been reached.

The signal can be reconstructed from the effective number of pulses generated by the DROS, since the change in the feedback flux is simply given by

$$\Delta\Phi_{fb} = \left(N_{sig} - N_{ref}\right)\delta\Phi_{fb}\,, \tag{5.7}$$

where N_{sig} represents the number of pulses across the signal SQUID and N_{ref} is the number of pulses across the reference SQUID. This is also discussed in section 5.5.3.

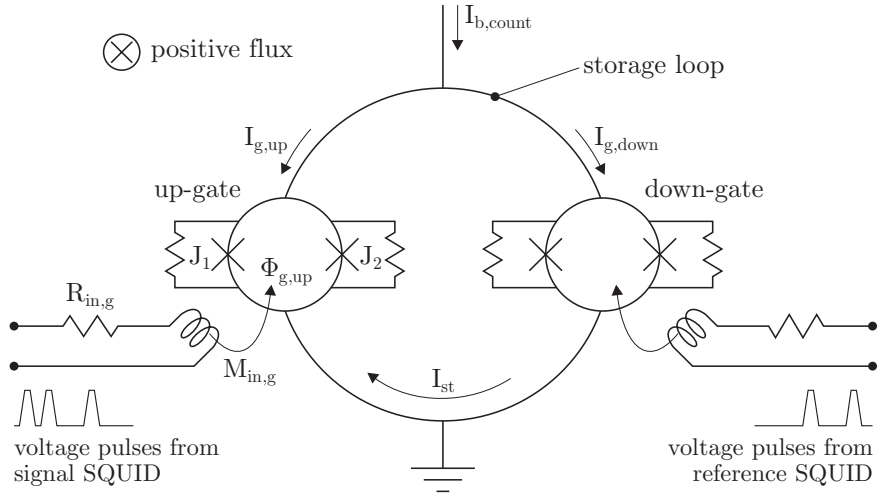

Fig. 5.3 Scheme of the Josephson counter.

5.1.3 The Josephson counter

The key element of the FLL circuitry of the Smart DROS, the Josephson counter, is shown in Fig. 5.3. This relatively simple up-down counter is based on the counters of the Fujitsu [12] and HYPRES [13,14] digital SQUIDs. The Josephson counter is implemented in superconducting electronics and it is integrated on the same chip as the DROS. It consists of a superconducting storage loop of inductance L_{st}, interrupted by two write gates, the up-gate and the down-gate. These write gates are resistively shunted non-hysteretic dc SQUIDs through which flux quanta are added to or extracted from the storage loop.

The Josephson counter is biased at a constant current $I_{b,count}$. This bias current is distributed over the up-branch and the down-branch of the storage loop and the circulating current in the counter is thus given by

$$I_{st} = \frac{I_{g,down} - I_{g,up}}{2}. \tag{5.8}$$

The circulating current can be decreased or increased by extracting flux quanta from the storage loop or adding flux quanta to the storage loop, respectively. In the Smart DROS, the up-gate of the counter is connected to the signal SQUID and the down-gate is connected to the reference SQUID of the DROS and the voltage pulses that are generated by the DROS increase or decrease the number of flux quanta in the storage loop. In the write gates, the voltage pulses are converted to flux pulses by means of input coils which have a mutual inductance $M_{in,g}$ with the gates. The values of $M_{in,g}$ and $R_{in,g}$ are dimensioned such that the amplitude of the flux pulses is about 1 Φ_0. This is discussed in more detail in section 5.2.1.

Figure 5.4 shows the threshold characteristic of the up-gate for a screening parameter $\beta_{L,g} = 2I_0L_{sq,g}/\Phi_0 = 2$ and explains the flux writing process. Here, I_0 is the critical current of one junction of the gate and $L_{sq,g}$ is the gate inductance. Since

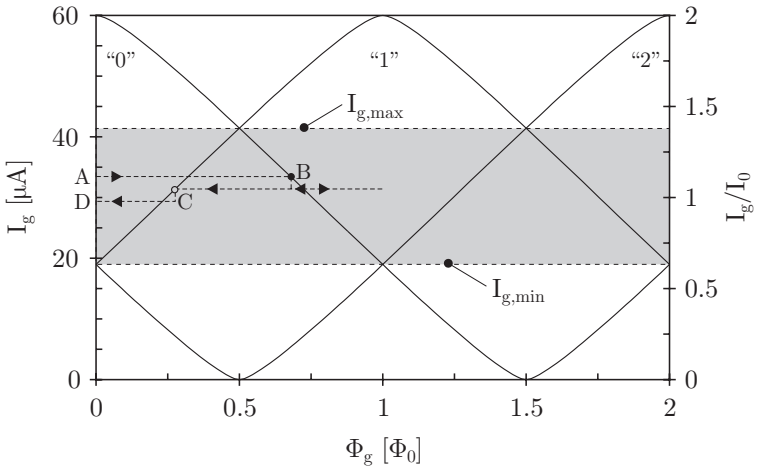

Fig. 5.4 Threshold characteristics of the up-gate for $\beta_{L,g} = 2$. When a flux quantum is added to the Josephson counter, the path A-B-C-D is followed. The black and open circles, i.e. points B and C, correspond to the points where junction J_1 respectively J_2 makes a 2π phase leap. The gray area represents the working range.

both write gates are identical, only the up-gate is considered. When a positive flux pulse $\Phi_{g,up}$ is applied to the up-gate, path A-B-C-D is followed. Starting from point A, the applied flux is increased from 0 and a counter-clockwise screening current will be induced in the SQUID loop of the write gate. As a result, an imbalance between the currents through both junctions will arise: The current through junction J_1 is increased, whereas the current through junction J_2 is decreased. In point B, the current through junction J_1 reaches its critical value and by crossing the threshold curve, this junction switches transiently to the voltage state. However, since the junction is non-hysteretic, the junction does not stay in the normal state and it switches back to the superconducting state, generating a single flux quantum (SFQ) pulse. This SFQ-pulse causes a quantized leap of the phase across the junction of $\Delta\phi_1 = 2\pi$ and consequently one flux quantum enters the write gate, i.e. the write gate switches from the n = 0 flux quantum state to the n = 1 state.

When the flux in the up-gate decreases again, a clockwise screening current keeps the gate in the n = 1 state, until point C is reached. At this point, the threshold curve is crossed and now the current through junction J_2 reaches its critical value. The phase across this junction makes a 2π phase leap and the write gate switches back to the n = 0 state. By doing so, the flux quantum that entered the SQUID loop is transferred from the write gate to the superconducting storage loop of the counter. Since the flux quantization condition,

$$I_{st}L_{st} + \frac{\phi_{down} - \phi_{up}}{2\pi}\Phi_0 = 0\,, \tag{5.9}$$

has to be fulfilled, the increase in the phase difference across the entire up-gate, ϕ_{up}, by 2π causes the circulating current in the storage loop to increase by an amount of

$$\delta I_{st} = \frac{\Phi_0}{L_{st}}\,, \tag{5.10}$$

during this flux writing process. On the other hand, an increase in the phase difference across the down-gate by 2π, i.e. extracting one flux quantum from the storage loop, causes the circulating current to decrease by the same amount.

In the Smart DROS, the circulating current in the storage loop is led through the feedback coil of the DROS. In this way, the counter supplies the feedback flux with a quantization unit of

$$\delta\Phi_{fb} = M_{fb}\,\delta I_{st} = \frac{M_{fb}}{L_{st}}\Phi_0\,, \tag{5.11}$$

where M_{fb} represents the mutual inductance between the feedback coil and the signal SQUID of the DROS.

Figure 5.5 shows a numerical simulation of the process described above. The flux in the up-gate is increased from zero, point A, to 1 Φ_0. By crossing the threshold curves, point B, the phase ϕ_1 across junction J_1 is increased by 2π and the phase across the entire up-gate is increased by π. Consequently, the current through the gate $I_{g,up}$ is decreased by an amount of $\delta I_{st}/2 = \Phi_0/2L_{st}$ and according to Eq. (5.9) the circulating current is increased by the same amount. When junction J_2 makes the 2π phase leap, point C, the circulating current is again increased by $\Phi_0/2L_{st}$. In this simulation, the inductance of the storage loop is $L_{st} = 4$ nH, such that the quantization unit of the circulating current is $\delta I_{st} = 0.52$ μA.

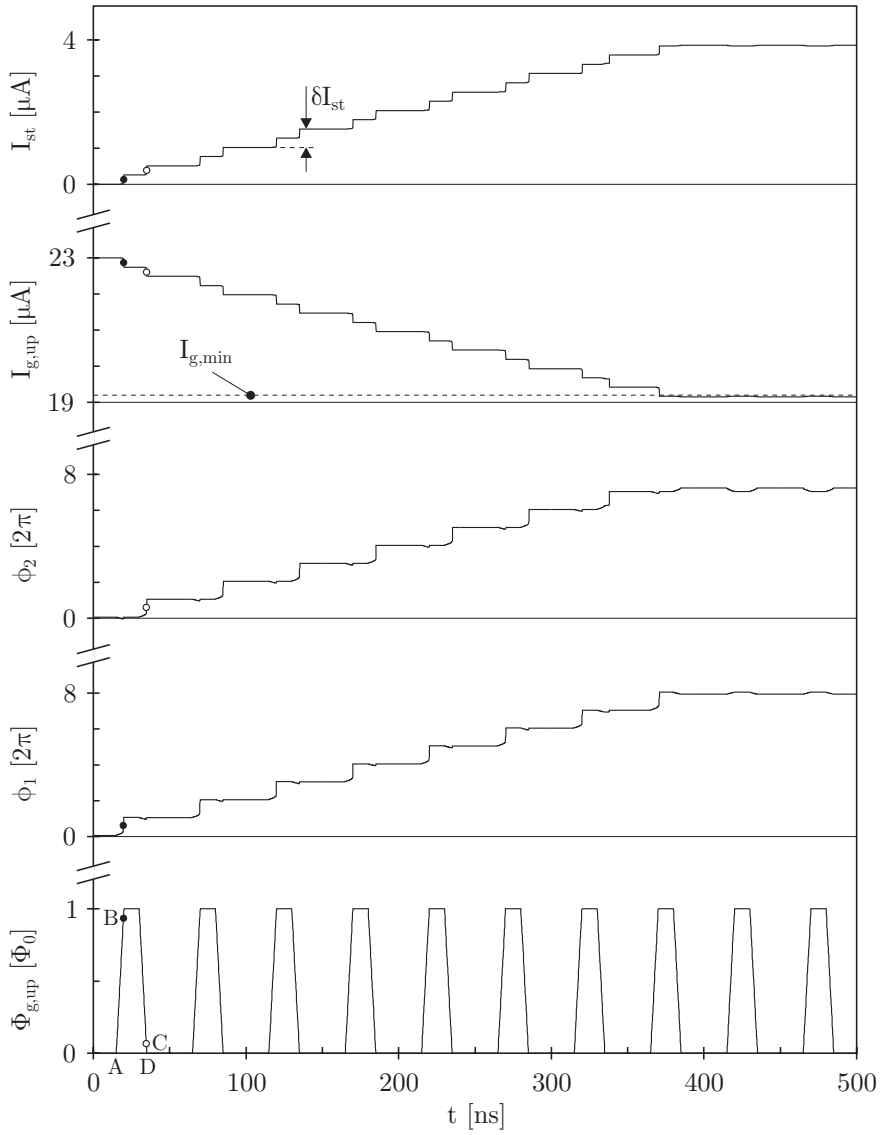

Fig. 5.5 Numerical simulation of the response of a Josephson counter to variations in the flux applied to the up-gate. $\Phi_{g,up}$ is the applied flux, ϕ_1 and ϕ_2 are the phases across the junctions of the gate, $I_{g,up}$ is the current through the gate and I_{st} is the circulating current in the storage loop. The screening parameter is $\beta_{L,g} = 2$, as in Fig. 5.4, and the inductance of the storage loop is $L_{st} = 4$ nH. The bias current of the counter is $I_{b,count} = 46$ μA. The Josephson counter stops operating when the current through the up-gate becomes smaller than the minimum allowed current, $I_{g,min} = 19.2$ μA.

5.2 Optimization of the Smart DROS

In the previous section, the operation principles of the key elements of the Smart DROS, the DROS and the Josephson counter, were discussed. In this section, the Smart DROS is optimized [15], starting with the output range of the Josephson counter.

5.2.1 Output range of the Josephson counter

In section 5.1.3, the operation principle of the Josephson counter was discussed. It should be clear that in order to operate properly, the write gates should be in the superconducting state and that they are only allowed to switch transiently to the normal state when switching from one flux quantum state to the other. Therefore, the maximum allowed current $I_{g,max}$ through the write gates is limited by the current at which the threshold curves of the n = 0 flux quantum state and the n = 1 state cross each other, i.e. the critical current at Φ_g = ½ Φ_0 for the n = 0 state. This is indicated in Fig. 5.4. The maximum allowed current is given by

$$I_{g,max} \approx \frac{\beta_{L,g}}{1+\beta_{L,g}} 2I_0 \,, \tag{5.12}$$

where $\beta_{L,g}$ is the screening parameter of the write gate and I_0 is the critical current of one junction. If the current is larger than $I_{g,max}$, for certain values of the applied flux the gate is not in the superconducting state and thus it will not operate.

Besides this upper limit for the current through the gate, one can also find a lower limit. Two situations can be distinguished. Firstly, for $\beta_{L,g} \leq 1$ the minimum allowed current through the write gate is $I_{g,min} = 0$. If the current is smaller, i.e. negative, the junction will make a -2π phase leap, such that the up-gate will

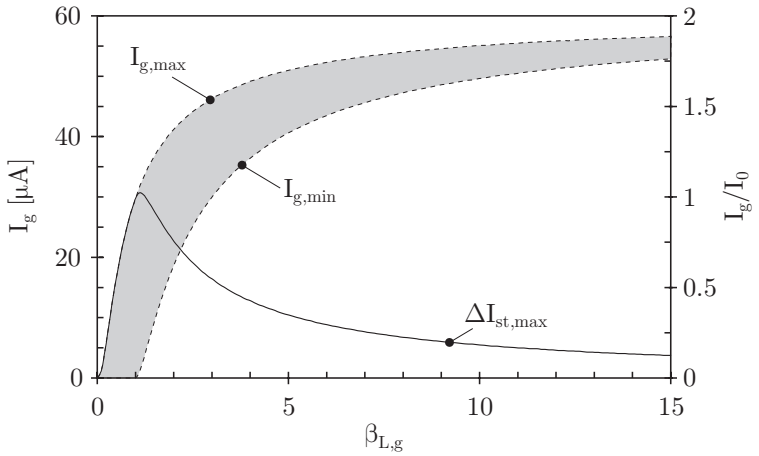

Fig. 5.6 Maximum and minimum allowed currents through the write gate as a function of the screening parameter. The write gate will only work properly when the current is in the gray area. $\Delta I_{st,max}$ is the corresponding maximum range of the circulating current in the counter. The critical current of the junctions of the gate is 30 μA.

extract a flux quantum from the storage loop instead of adding one and the down-gate will add a flux quantum instead of extracting one.

Secondly, for $\beta_{L,g} > 1$ the minimum allowed current through the write gate is determined by the point where the threshold curves of the n = 0 state and the n = 2 state cross each other, i.e. the critical current at $\Phi_g = 1\ \Phi_0$ for the n = 0 state. In this case, the maximum flux in the write gate is assumed to be $\Phi_g = 1\ \Phi_0$. If the current is smaller than $I_{g,min}$, the write gate stays in the n = 0 flux quantum state for all values of the applied flux and the gate will not make a 2π phase leap. This is exactly what happens in the simulation shown in Fig. 5.5. By adding flux quanta to the storage loop, the current through the up-gate is decreased. The bias current of the counter is $I_{b,count} = 46$ μA, such that at $t = 0$ s, the current through the up-gate is 23 μA, which is within the working range of the gate. However, when about 8 flux quanta are added to the counter, the current through the write gate becomes smaller than the minimum allowed current, $I_{g,min} = 19.2$ μA, and no more flux quanta are added to the storage loop.

Figure 5.6 shows the maximum and minimum allowed currents through the write gate as a function of the screening parameter $\beta_{L,g}$. In this case, the critical current of the junctions of the gate is 30 μA and it is assumed that $\beta_{L,g}$ is varying with $L_{sq,g}$. The working range of the Josephson counter is represented by the gray area, bounded by $I_{g,max}$ and $I_{g,min}$. The underlying model is based on the theory of ref. [16]. The maximum range of the circulating current for a certain value of the screening parameter $\beta_{L,g}$ is given by

$$\Delta I_{st,max} = I_{g,max} - I_{g,min}\,. \tag{5.13}$$

From Fig. 5.6, it can be concluded that the optimum value for the screening parameter is $\beta_{L,g} = 1$. To achieve the maximum output range given by Eq. (5.13), the bias current of the counter should be such that when no flux Φ_g is applied, the current through both write gates is exactly in the middle of the working range

$$I_{b,count} = I_{g,max} + I_{g,min}\,. \tag{5.14}$$

When the bias current of the Josephson counter does not have its optimum value, given by Eq. (5.14), the output range can be calculated as follows: The current through the write gates should always satisfy the conditions

$$I_{g,min} < I_{g,up} < I_{g,max} \text{ and } I_{g,min} < I_{g,down} < I_{g,max}\,. \tag{5.15}$$

Using

$$I_{b,count} = I_{g,up} + I_{g,down}\,, \tag{5.16}$$

and Eq. (5.8), these conditions can be rewritten as

$$\left|I_{st}\right| < \min\left(\frac{I_{b,count}}{2} - I_{g,min}, I_{g,max} - \frac{I_{b,count}}{2}\right), \tag{5.17}$$

which implies that the peak-to-peak range of the circulating current is

$$\Delta I_{st} = \min\left(I_{b,count} - 2I_{g,min}, 2I_{g,max} - I_{b,count}\right), \tag{5.18}$$

since the current can have both positive and negative values. Substituting Eq. (5.14) into Eq. (5.18) gives again the maximum range of the circulating current, as is given by Eq. (5.13).

For $\beta_{L,g} > 1$, one could try to enlarge the working range of the Josephson counter by increasing the amplitude of the flux pulses coupled to the write gates, i.e. larger than 1 Φ_0. In that case, the threshold curve for the n = 0 flux quantum state can be crossed for currents lower than the minimum allowed current $I_{g,min}$ that is shown in Fig. 5.6. However, when a junction switches from the n = 0 state in this case, it can jump to the n = 1 flux quantum state, but also to the n = 2 state. The state with the largest critical current is energetically favorable and thus that state is more likely to occur. For $\beta_{L,g} > 2$, there are even situations possible in which it is favorable to switch from the n = 0 state to a state higher than n = 1. This not uniquely defined switching would mean quantization errors and thus a possible rise in the noise of the Smart DROS. Thus flux pulses with an amplitude much larger than 1 Φ_0 should be avoided, i.e. the amplitude of the flux pulses in the Smart DROS should be designed to be ~1 Φ_0. For flux pulses with an amplitude smaller than 1 Φ_0, the maximum working range of the Josephson counter will be compromised.

5.2.2 Quantization unit of the feedback flux

An important advantage of the integration of a DROS and the FLL circuitry on one single chip is that the bandwidth and the flux slew rate can be much larger and higher, respectively, than those of conventional dc SQUID systems. The –3 dB bandwidth of the Smart DROS can be calculated as

$$f_{-3\mathrm{dB}} = \frac{\delta\Phi_{fb}}{\pi\,\Delta\Phi} f_{RO}\,. \tag{5.19}$$

The bandwidth of the on-chip FLL circuitry can be much smaller than the relaxation oscillation frequency when $\delta\Phi_{fb} \ll \Delta\Phi$. The maximum flux slew rate of the Smart DROS can be expressed as

$$\frac{\partial\Phi_{sig}}{\partial t} = \pi\,\Delta\Phi\, f_{-3\mathrm{dB}} = \delta\Phi_{fb} f_{RO}\,. \tag{5.20}$$

A large quantization unit of the feedback flux leads to both a large bandwidth and a high flux slew rate. However, to prevent the sensitivity of the Smart DROS to be limited by quantization errors, the quantization unit of the feedback flux should not exceed the broadband flux noise of the DROS [17]. In the ideal case, the quantization unit of the feedback flux is equal to the broadband flux noise of the DROS,

$$\delta\Phi_{fb} = \sqrt{S_\Phi f_{RO}}\,. \tag{5.21}$$

A larger quantization unit leads to quantization errors, whereas a smaller value means that the system unnecessarily compensates for its own noise, such that the

maximum bandwidth and the flux slew rate will be compromised [15,18,19,20]. In the prototype Smart DROS, $\delta\Phi_{fb} \ll \Delta\Phi$ and therefore bandwidth and slew rate were indeed compromised [6].

5.2.3 Coupling schemes

In order to achieve a large quantization unit of the feedback flux, the coupling scheme to apply the signal flux Φ_{sig} to the Smart DROS has to be investigated. The coupling schemes we consider are shown in Fig. 5.7. For simplicity, the DROS in this scheme is depicted as a single SQUID. The signal flux can be coupled either directly to the DROS or indirectly via the counter. Optionally, an intermediate flux transformer can be used to make coupling between the rather large feedback coil L_{fb} and the signal SQUID inductance $L_{sq,sig}$ of the DROS easier. However, the main disadvantage of using a transformer is that a part of the signal energy is stored in the transformer, so that coupling to the signal SQUID is less efficient.

Let us first consider the coupling scheme with the intermediate flux transformer. Assuming that the coupling coefficient k has in all cases the same value, the effective mutual inductance between the feedback coil and the signal SQUID of the DROS is given by

$$M_{fb,eff} = \frac{M_{fb,1}M_{fb,2}}{L_{t,1}+L_{t,2}} = k^2\,\frac{\sqrt{L_{fb}L_{t,1}L_{t,2}L_{sq,sig}}}{L_{t,1}+L_{t,2}}\,, \tag{5.22}$$

where $L_{t,1}$ and $L_{t,2}$ are the transformer inductances. When $L_{t,1} = L_{t,2}$, the effective inductance of the storage loop of the counter can be expressed as

$$L_{st,eff} = L_p + \left(1-\frac{k^2}{2}\right)L_{fb}\,. \tag{5.23}$$

In this expression, L_p is the inductance of the pickup coil of the Josephson counter. The quantization unit of the feedback flux can thus be expressed as

$$\delta\Phi_{fb} = \frac{M_{fb,eff}}{L_{st,eff}}\Phi_0 = k^2\sqrt{\frac{L_{sq,sig}}{L_p}}\,\frac{\sqrt{\alpha}}{2+\alpha\left(2-k^2\right)}\Phi_0\,. \tag{5.24}$$

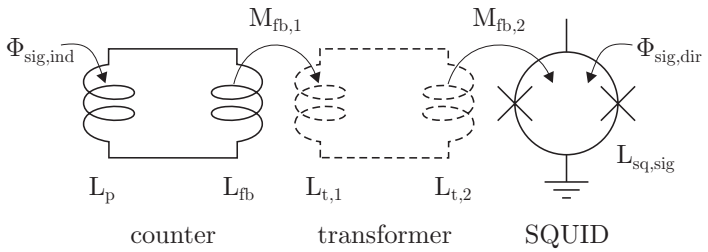

Fig. 5.7 Possible coupling schemes of the Smart DROS. The dotted intermediate flux transformer is optional and the DROS is represented by a single dc SQUID. The signal flux can be coupled either directly to the signal SQUID of the DROS or indirectly via the pickup coil L_p of the Josephson counter.

Here, $\alpha = L_{fb}/L_p$. Taking $\partial\Phi_{fb}/\partial\alpha = 0$, it can be shown that the quantization unit of the feedback flux is maximum for $\alpha = 2/(2-k^2)$, i.e. for this value of α, the coupling between the pickup coil and SQUID inductance is optimum.

On the other hand, when no intermediate flux transformer is used, the quantization unit of the feedback flux is given by

$$\delta\Phi_{fb} = k\sqrt{\frac{L_{sq,sig}}{L_p}}\,\frac{\sqrt{\alpha}}{\alpha+1}\,\Phi_0\,, \tag{5.25}$$

and the quantization unit of the feedback flux is maximum for $\alpha = 1$. The adverse effect of the transformer on the quantization unit of the feedback flux is clear. For example, if the SQUID inductance is $L_{sq,sig} = 250$ pH, the pickup coil inductance is $L_p = 15$ nH and the coupling coefficient is $k = 0.8$, the quantization unit is $\delta\Phi_{fb} = 52$ mΦ_0 when no transformer is used. However, with a transformer, the quantization unit is $\delta\Phi_{fb} = 25$ mΦ_0. Although this is only a factor 2, this means that the SQUID inductance should be a factor $2^2 = 4$ larger if we want to achieve the same quantization unit of the feedback flux as for the case without transformer. Since a larger SQUID means more noise, the coupling scheme without the intermediate flux transformer is to be preferred, as long as this is allowed within the practical limitations of the layout.

As was discussed in section 5.2.1, the output range of a Josephson counter is limited, since the circulating current in the storage loop has to fulfill the condition of Eq. (5.17). If this condition is not fulfilled, the counter will not operate. When the Smart DROS is operating and a signal flux is applied to the signal SQUID of the DROS, the Josephson counter cancels the applied signal flux by generating a circulating current in the storage loop. Because of the limited output range of the counter, this means that the Smart DROS has a linear response over a range of the signal flux of

$$\Delta\Phi_{sig,max} = \frac{\Delta I_{st,max} L_{st}}{\Phi_0}\,\delta\Phi_{fb}\ . \tag{5.26}$$

The equation gives the maximum linear range, i.e. if the bias current of the counter does not have its optimum value given by Eq. (5.14), the linear Φ_{sig} range will be smaller. However, the intrinsic linear range of the Smart DROS can be made very large by coupling the signal flux to the storage loop of the counter instead of coupling it to the signal SQUID of the DROS. For this purpose, the pickup coil L_p was introduced in the coupling scheme. When applying the signal flux via the pickup coil, the circulating current in the storage loop is continuously nulled, which makes the linear range virtually infinite.

5.3 Numerical analysis

The main goal of optimizing the Smart DROS is to achieve a high flux slew rate and a large dynamic range. In this section, the numerical analysis of an optimized Smart DROS with a maximum flux slew rate of $5{\cdot}10^6$ Φ_0/s is discussed [21].

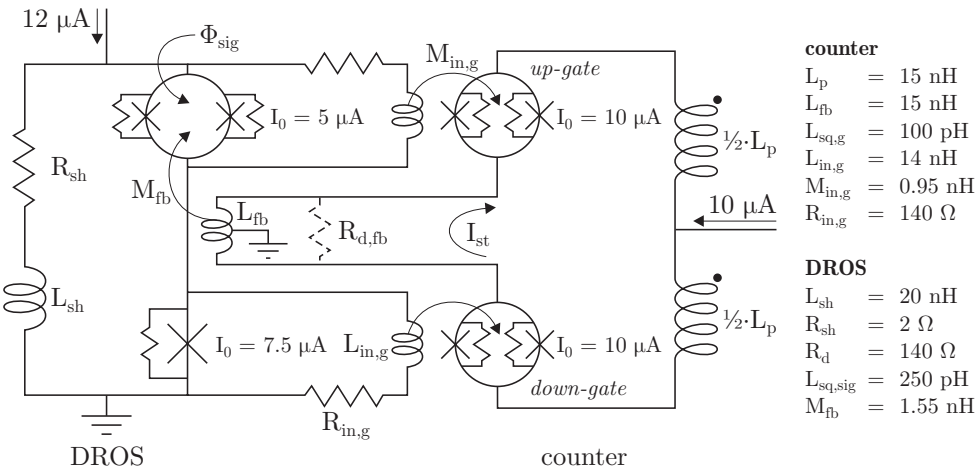

Fig. 5.8 Simulation scheme used to investigate the dynamic behavior of the Smart DROS. The coupling coefficient is in all cases $k = 0.8$. The SQUID inductance of the DROS is 250 pH and the inductance of the write gates is 100 pH. The quantization unit of the feedback flux is 52 $m\Phi_0$.

5.3.1 Simulation model

The dynamic behavior of the Smart DROS was investigated by means of the numerical simulation software JSIM [22]. The simulation scheme is shown in Fig. 5.8. For simplicity, a reference junction instead of a reference SQUID was used.

Based on the optimization process discussed in the previous section, the flux slew rate was maximized by adapting the quantization unit of the feedback flux to the broadband flux noise of the DROS. The inductance of the signal SQUID of the DROS is $L_{sq,sig} = 250$ pH and the critical current of the junctions of the signal SQUID is $I_0 = 5$ μA, corresponding to a screening parameter of $\beta_{L,sig} = 1.2$. The junctions are assumed to have a size[ii] of $A = 4$ x 4 μm^2. Consequently, the practical junction capacitance is $C_j = 0.5$ pF, assuming that the capacitance per junction area is $C/A = 0.03$ pF/μm^2. The *R-L* shunt of the DROS consists of a resistor $R_{sh} = 2\ \Omega$ and an inductor $L_{sh} = 20$ nH. The time constant $L_{sh}/R_{sh} = 10$ ns implies a relaxation oscillation frequency of about 100 MHz. The relaxation oscillation frequency was limited to 100 MHz to make a possible digital readout scheme easier. The theoretical white flux noise is calculated to be 5.4 $\mu\Phi_0/\sqrt{\text{Hz}}$. Consequently, the quantization unit of the feedback flux has to be about 50 $m\Phi_0$. When no intermediate flux transformer is used, this can be established with a pickup coil inductance of $L_p = 15$ nH. Since the ratio L_{fb}/L_p should be 1 [from Eq. (5.25)], the

[ii] The fabrication process determines the minimum size of the junctions. For the standard fabrication process at the University of Twente based on planar junctions, this is about 4 x 4 μm^2. Since the junctions in the signal SQUID are the smallest junctions of the Smart DROS, the size of these junctions is fixed at 4 x 4 μm^2. The minimum junction area and the smallest critical current in the design determine the critical current density J_c.

feedback coil should also have an inductance of $L_{fb} = 15$ nH. From these values and assuming a coupling coefficient of $k = 0.8$ the actual quantization unit of the feedback flux can be calculated to be $\delta\Phi_{fb} = 52$ mΦ_0 [from Eq. (5.25)]. The maximum flux slew rate of the Smart DROS is thus $\partial\Phi_{sig}/\partial t = \delta\Phi_{fb} f_{RO} = 5{\cdot}10^6\ \Phi_0$/s.

Since the circulating current in the Josephson counter should supply the feedback flux to the DROS, the storage loop of the counter is connected to the DROS via the feedback coil L_{fb}, having a mutual inductance with the signal SQUID of $M_{fb} = k(L_{fb}L_{sq,sig})^{1/2} = 1.55$ nH. Here, the coupling coefficient is assumed to be $k = 0.8$. During the relaxation oscillations, the net flux in the signal SQUID fluctuates, which causes high frequency oscillations in the circulating current of the counter via this mutual inductance. This effect can cause large current spikes in the counter [1]. By shunting the feedback coil with a damping resistor $R_{d,fb}$, these spikes can be reduced. However, to prevent phase shifts, the time constant $L_{fb}/R_{d,fb}$ should be much smaller than $1/f_{RO}$. In this design, $R_{d,fb} = 50\ \Omega$.

The L-C resonances between the shunt inductance L_{sh} and the SQUID capacitance C_{sq} are damped by an effective damping resistor of $R_{d,eff} = 70\ \Omega$. This results in a damping parameter $D = 1$, such that the requirement of Eq. (5.6) is fulfilled and the output voltage is as large as possible within this requirement, i.e. since the amplitude of the voltage pulses generated by the DROS is of the order of $\frac{3}{2} I_0 R_{d,eff}$, the effective damping resistance should be as large as possible. The effective damping resistance is the parallel resistance of the damping resistance $R_d = 140\ \Omega$ and $R_{in,g} = 140\ \Omega$. Since both R_d and $R_{in,g}$ contribute to the damping of the L-C resonances, the effective damping resistance should be used in Eq. (5.6). The expected amplitude of the voltage pulses generated by the DROS is about 0.4 mV.

As was discussed in section 5.2.1, the coupling between the DROS and the Josephson counter should be such that the amplitude of the flux pulses coupled to the write gates is about 1 Φ_0. Furthermore, the time constant $L_{in,g}/R_{in,g}$ has to be smaller than the typical pulse duration. Here, $L_{in,g}$ is the inductance of the input coils of the write gates. Thus, in designing the write gate, the required amplitude of the flux pulses and this time constant should be taken into account. In this Smart DROS, the inductance of the coils of the write gates is $L_{in,g} = 14$ nH and the SQUID inductance of the gates is $L_{sq,g} = 100$ pH. This results in a time constant of $L_{in,g}/R_{in,g} = 0.1$ ns, which is smaller than the expected pulse duration[iii]. Assuming that the coupling coefficient between the input coil and the SQUID inductance is 0.8, the mutual inductance of the input coils with the gates is $M_{in,g} = 0.95$ nH. This means that the amplitude of the flux pulses is $\Phi_g = (0.4\ \text{mV}/R_{in,g})M_{in,g} \approx 1.3\ \Phi_0$. The critical current of the junctions of the write gates is $I_0 = 10$ μA, resulting in a screening parameter of $\beta_{L,g} = 1.0$. Since the critical current of these junctions is two times larger than that of the signal SQUID, the area and thus the capacitance of these junctions are also twice as large, i.e. $C_j = 1$ pF. Shunt resistors of 2 Ω are used to remove hysteresis: The McCumber parameter is $\beta_C = 0.12$.

[iii] The pulse duration is typically of the order of 10 % of the duration of one complete relaxation oscillation cycle. Since $f_{RO} = 100$ MHz, the expected pulse duration is of the order of 1 ns.

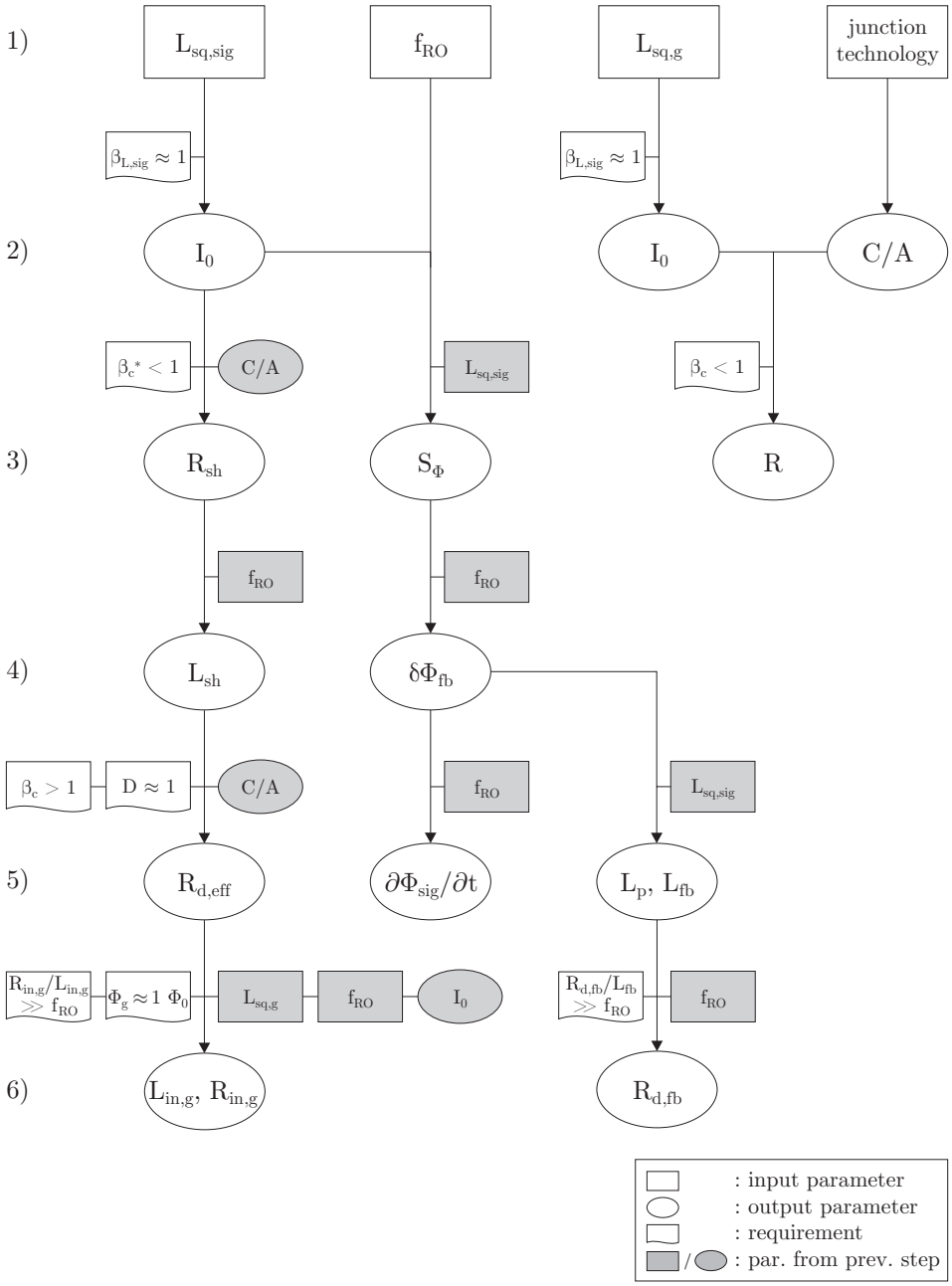

Fig. 5.9 Design scheme of the Smart DROS. The input parameters are chosen, step 1, and the output parameters are calculated from the requirements, steps 2 to 6. The parameters in the gray rectangles and ellipses are extracted in or known from a previous step in the design. If one of the requirements or boundary conditions cannot be fulfilled, parameters in previous steps have to be adapted. The $\beta_C{}^* = 4\pi I_0 {R_{sh}}^2 C_{sq}/\Phi_0$ parameter is the effective McCumber parameter for relaxation oscillation SQUIDs and should be smaller than 1 [11,8,23]. In most practical DROSs, $\beta_C{}^*$ is designed to be much smaller than 1 to ensure proper operation [1].

Figure 5.9 shows the interrelationships between the different parameters of the Smart DROS and summarizes the design considerations that were made in this section. It clearly shows that changing one parameter may affect many parameters. However, by fixing only a few input parameters, all the parameters can be calculated using the requirements and the boundary conditions that have to be fulfilled. In this scheme, the signal SQUID inductance of the DROS $L_{sq,sig}$, the relaxation oscillation frequency f_{RO}, the gate inductance $L_{sq,g}$ and the junction technology are chosen, i.e. these parameters are the input parameters from which the other parameters are extracted. The relaxation oscillation frequency is fixed at 100 MHz to make a possible digital readout scheme easier. The fabrication process at the University of Twente determines the minimum Josephson junction area and reasonable SQUID inductances are required to enable good signal coupling. One can use other input parameters, but then the design scheme changes of course.

5.3.2 Numerical simulations of the Smart DROS

The scheme of the Smart DROS shown in Fig. 5.8 was implemented in JSIM and was simulated. The relaxation oscillations of the signal SQUID and the reference junction are investigated in detail in Fig. 5.10. The plasma oscillations have faded completely before the next relaxation oscillation starts and the system is well damped by the effective damping resistor of $R_{d,eff} = 70\ \Omega$, i.e. L-C resonances do not occur and the switching process to the zero-voltage state occurs in a controlled way. The amplitude of the voltage pulses is about 0.4 mV.

Figure 5.11a shows the result of a numerical simulation of the Smart DROS in operation. In this case, the signal flux, which is represented by the dotted line, is coupled directly to the signal SQUID of the DROS. At $t = 0$, the system is in its dynamic equilibrium and the signal SQUID and the reference junction oscillate in turn, i.e. the circulating current in the counter oscillates around an average value. At $t = 100$ ns, the signal flux is increased with a slew rate close to the maximum

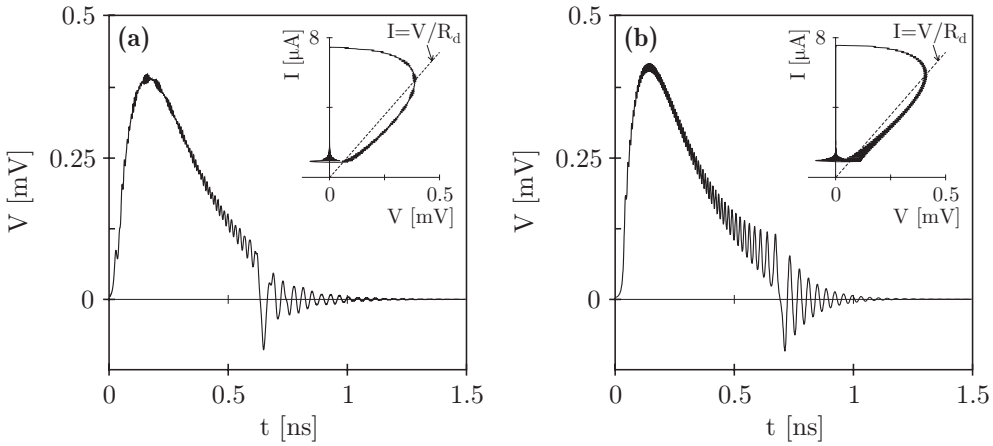

Fig. 5.10 (a) Detailed view of one of the relaxation oscillations of the signal SQUID of the Smart DROS. **(b)** Relaxation oscillation of the reference junction. The insets show the I-V paths that are followed during the oscillations.

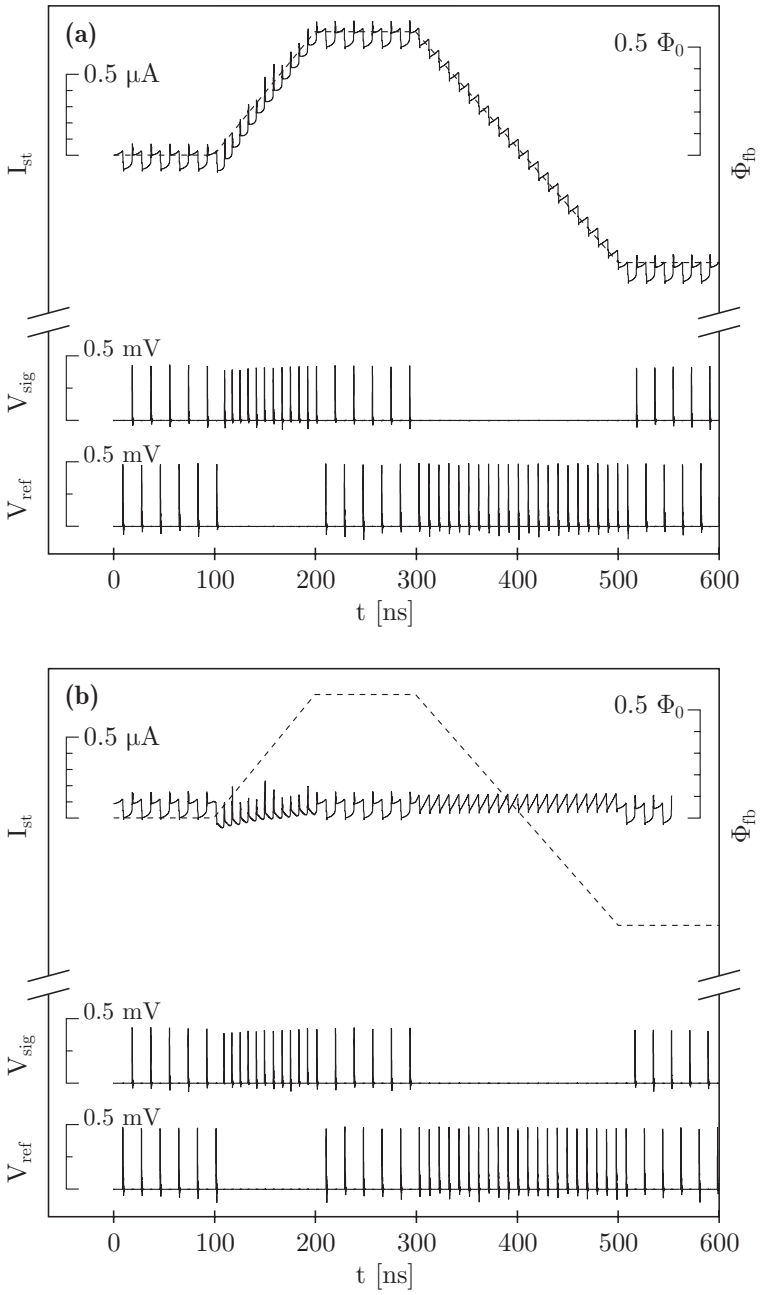

Fig. 5.11 (a) Numerical simulation of the response of the optimized 100 MHz Smart DROS to variations in the input flux. The signal flux is directly applied to the signal SQUID of the DROS. V_{sig} is the voltage across the signal SQUID of the DROS and V_{ref} is the voltage across the reference junction. The current spikes in the circulating current I_{st} are caused by fluctuations in the net flux of the signal SQUID, see section 5.3.1. **(b)** As **(a)** except for the fact that in this case the flux is indirectly applied via the storage loop of the counter.

slew rate of the Smart DROS, $\partial\Phi_{sig}/\partial t = 5{\cdot}10^6\ \Phi_0$/s. As a result, only the signal SQUID participates in the relaxation oscillations and the feedback flux is increased, following the input signal, until a new dynamic equilibrium is established. At $t = 300$ ns, the applied flux is decreased and only the reference junction generates voltage pulses in order to restore the dynamic equilibrium.

In the simulation described above, the applied flux was such that the circulating current that is required to compensate the input signal is within the output range of the Josephson counter. However, by applying the flux to the signal SQUID of the DROS, the dynamic range of the Smart DROS is limited because of the limited output range of the Josephson counter, as was discussed in section 5.2.3. For this design, the maximum range of the Josephson counter is $\Delta I_{st,max} = 10$ μA [from Eq. (5.13)], corresponding to a linear response over a Φ_{sig} range of 7 Φ_0 [from Eq. (5.26)]. By coupling the signal flux indirectly to the DROS, via the storage loop of the counter, the linear range is virtually infinite. Figure 5.11b shows a simulation similar to Fig. 5.11a but now the signal flux is coupled to the storage loop of the Josephson counter via the pickup coil L_p. In this case, the circulating current is continuously nulled and it only oscillates around a constant value, such that the circulating current is always within the output range of the Josephson counter.

5.4 Layout design and fabrication of an optimized Smart DROS

The design of the optimized Smart DROS is based on the numerical simulations that were discussed in the previous section. In this section, the inductance extraction, the layout of the fabricated Smart DROS and the fabrication process are presented [24].

5.4.1 Inductance extraction

For proper operation of the Smart DROS, it is important that the design values and the experimental values of the SQUID inductances and the coil inductances agree. For example, the voltage pulses of the DROS that are applied to the write gates should induce flux pulses with an amplitude of ~1 Φ_0, see section 5.2.1. This means that the mutual inductance $M_{in,g}$ between the SQUID inductance of the write gate and the input coil on top of it has to be estimated rather accurately. Another important parameter in the design of an optimized Smart DROS is the M_{fb}/L_{st} ratio, since it determines the quantization unit of the feedback flux.

We have estimated the inductances both analytically and numerically. The two most important contributions to the SQUID inductance are the hole inductance L_h and the slit inductance L_t. Generally, the return line of the input coil lies in the slit. This results in a double slit structure with an inductance per unit length of [25]

$$\frac{L_t}{l_t} = 3600\pi\varepsilon_0 \ln\left(2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right), \quad k = \sqrt{1-\left(\frac{s}{s+2w}\right)^2}\ , \tag{5.27}$$

where $\varepsilon_0 = 8.854187{\cdot}10^{-12}$ F/m is the permittivity of the vacuum, s the width of the return line, w the width of the slits and l_t the length of the double slit. In practical

situations, the slit inductance is of the order of 0.4 pH/μm [26], e.g. for $s = 10$ μm and $w = 5$ μm, $L_t/l_t = 0.4$ pH/μm. The inductance of an N-turns input coil completely covering the SQUID washer is estimated as [26,27]

$$L_{in} = N^2 \left(L_h + \frac{L_t}{3} \right) + L_s \,, \tag{5.28}$$

where L_s is the stripline inductance of the coil. Generally, the contribution of the stripline is negligible compared to the contributions associated with the hole and the slit. The mutual inductance between the coil and the SQUID is given by

$$M_{in} = N \left(L_h + \frac{L_t}{2} \right). \tag{5.29}$$

Using these working formulas, the inductances can be estimated rather accurately only if the input coil is completely covering the washer of the SQUID.

In case of the gate SQUIDs, the mutual inductance $M_{in,g}$ between the SQUID inductance and the input coil on top of it is fixed, such that the amplitude of the flux pulses is ~1 Φ_0, i.e. the required value for $M_{in,g}$ forms a boundary condition that has to be fulfilled. Together with the SQUID inductance and the design rules following from the fabrication process, all other parameters can be extracted. The design rules determine the minimum values of s, w, the width of the turns of the input coil and the distance between turns. In case of the gate SQUID, $s = 10$ μm and $w = 5$ μm. The width of input coil turns is taken to be 4 μm and the distance between turns is 6 μm. For the signal SQUID, the M_{fb}/L_{st} ratio forms the boundary condition. The width of the input coil turns and the distance between the turns is the same as for the write gates and $s = 15$ μm and $w = 5$ μm.

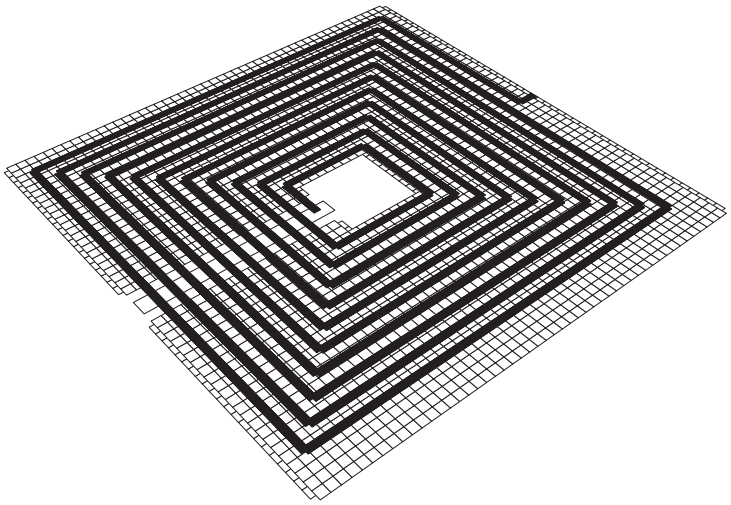

Fig. 5.12 Discretization of the gate SQUID to numerically extract the SQUID inductance, the input coil inductance and the mutual inductance between them. The washer is implemented as a ground plane, whereas the input coil on top of the washer consists of straight segments connected together.

For real 3D numerical inductance extraction, several software packages are available [28,29,30]. We used FastHenry 2.0S, which is a free 3D inductance extraction software package [31]. Using FastHenry, inductances can be extracted in two ways. Firstly, a conductor can be defined as straight segments with a certain width and height, connected together at nodes. A node is a point in 3D-space. The segments can then be broken into a number of parallel, thin filaments. Each filament is assumed to carry a uniform current density along its length. Secondly, a rectangular ground plane can be defined. In this ground plane, a grid of nodes is made, which defines a mesh of segments. Each segment is given a height equal to the specified thickness of the ground plane and a width equal to the node spacing, such that the space between segments is completely filled. In the ground plane, holes can be defined as missing segments. The accuracy of the calculations is determined by the discretization level of the ground plane and the filaments and thus by the processor speed and the memory of the computer that is used.

For the numerical inductance extraction, the SQUID washer was implemented as a ground plane, as is shown in Fig. 5.12. The coil on top of the SQUID consists of segments. The inductances of the SQUID washer, the input coil and the mutual inductance between them were numerically calculated by using FastHenry.

5.4.2 Layout of the Smart DROS

The layout of the optimized Smart DROS is based on the numerical simulations that were discussed in section 5.3. This means that the parameters of the Smart DROS were designed to meet the parameters summarized in Fig. 5.8 closely. The layouts of the SQUID washers and the input coils were designed using the analytical working formulas that were presented in the previous section, taking into account that the amplitude of the flux pulses coupled to the write gates should be ~1 Φ_0 and that the quantization unit of the feedback flux is equal to the broadband flux noise of the DROS. From this layout, the inductances were also numerically extracted.

The designed mutual inductances between the write gates and their input coils were analytically calculated to be $M_{in,g} = 907$ pH. The numerically extracted mutual inductance is marginally smaller: 853 pH. This means that the expected amplitude of the flux pulses is $\Phi_g = (0.4\ \mathrm{mV}/R_{in,g})M_{in,g} \approx 1.2\ \Phi_0$, based on a resistance in the write gates of $R_{in,g} = 140\ \Omega$. The effective damping resistance, which is the parallel resistance of the damping resistance R_d and $R_{in,g}$, to prevent L-C resonances between the shunt inductance and the SQUID capacitance is $R_{d,eff} = 70\ \Omega$. Since the amplitude of the voltage pulses that are generated by the DROS strongly depends on the critical current of the junctions, the proper operation of the optimized Smart DROS is strongly dependent on the correctness of the critical current density. This design is based on a critical current density of $J_c = 31\ \mathrm{A/cm^2}$. However, the critical current density is not exactly controllable. Therefore, several designs were made in which the ratio between $R_{in,g}$ and R_d was varied in such a way that the effective damping resistance was in all cases $R_{d,eff} = 70\ \Omega$. As was discussed above, for the standard design, $\Phi_g \approx 1.2\ \Phi_0$. Two other designs based on this design were made with $\Phi_g \approx 1.7\ \Phi_0$ and $\Phi_g \approx 2.4\ \Phi_0$.

Table 5.1 Calculated and experimental inductances.

	Analytical	Numerical	Experimental
$L_{sq,g}$ [pH]	110	105	100
$M_{in,g}$ [pH]	907	853	820
$L_{sq,sig}$ [pH]	281	279	280
L_{st} [nH]	43.2	44.0	43.0
M_{fb} [nH]	2.3	2.0	2.1

The optimized Smart DROS is based on a DROS with a SQUID inductance of $L_{sq,sig} = 280$ pH and $I_0 = 5$ μA. According to theory [from Eq. (5.5)], this would mean a white flux noise of $\sqrt{S_\Phi} = 5.7\ \mu\Phi_0/\sqrt{\text{Hz}}$. The quantization unit of the feedback flux calculated from the extracted inductances is ~50 $m\Phi_0$. Together with a relaxation oscillation frequency of 100 MHz, this results in a maximum flux slew rate of $5{\cdot}10^6\ \Phi_0$/s. In Table 5.1, the analytically calculated and numerically extracted values of the inductances of the designed SQUID washers, the input coils and the mutual inductances between them are summarized. The SQUID inductances and the mutual inductances deviate slightly from the inductances used in the simulations[iv], so that all other parameters in the design, e.g. shunt resistances, can have the same values as in the simulation. Only the damping resistance in the storage loop was changed compared to the simulation model. In the final design, $R_{d,fb} = 70\ \Omega$, because of the larger inductance of the storage loop.

Figure 5.13 shows a micrograph and the corresponding schematic overview of the layout of the complete Smart DROS. For the layout design, the layout software CleWin was used [32]. The Josephson junctions in the design have a minimum size of 4 x 4 μm^2. The chip was designed such that it can be read out by either a readout SQUID, measuring the circulating current in the storage loop of the Josephson counter, or by a differential counter at room temperature, counting the voltage pulses. However, the intrinsic slew rate and bandwidth of the Smart DROS can only be measured using a counter, since a readout SQUID requires its own external FLL circuitry. The limitations of using a readout SQUID and a proposal for a digital readout scheme are discussed in section 5.5.3. Both the intermediate flux transformer between the readout SQUID and the Josephson counter and the signal SQUID of the DROS have a gradiometric "figure-8" layout. This reduces parasitic coupling and eliminates flux variations in the DROS or in the readout SQUID caused by fluctuations in the bias current of the counter.

Several Smart DROSs were designed. For some of the chips the readout SQUID is connected to the counter and for other chips the readout SQUID is not connected. In principle, the readout SQUID can be disconnected or connected respectively, by removing or adding small Nb blocks in the intermediate flux transformer, represented by the small gray areas in Fig. 5.13b. When the readout

[iv] These deviations are the result of using the working formulas described in section 5.4.1 and the numerical inductance extraction using FastHenry for the layout design of the Smart DROS, whereas for the numerical simulation model in section 5.3.1, no layout information was used, i.e. in the simulation model, it was simply assumed that $M_{in} = k(L_{in}L_{sq})^{1/2}$, see also section 2.2.3.

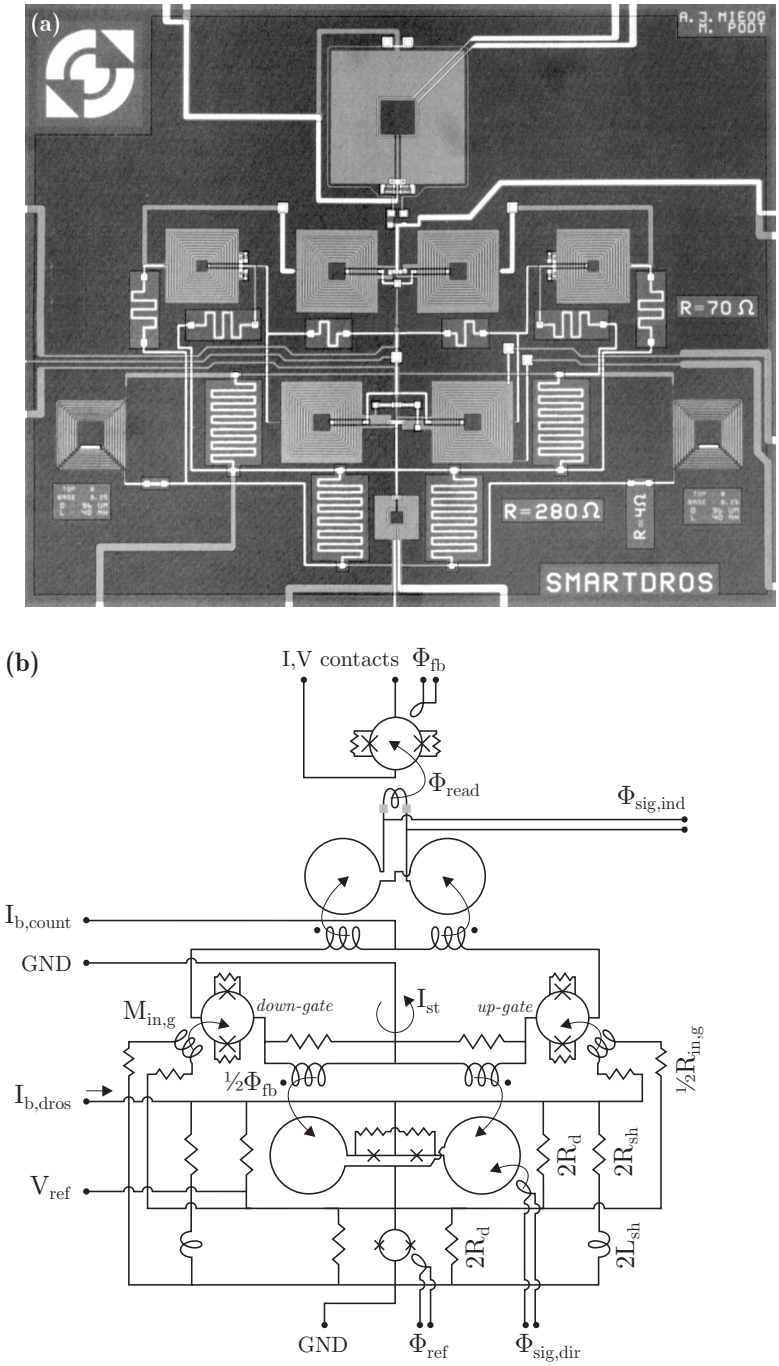

Fig. 5.13 (a) Micrograph and **(b)** scheme of the optimized 100 MHz Smart DROS based on a gradiometric DROS with reference SQUID. The readout SQUID in the upper part of the chip can be used to measure the circulating current in the Josephson counter. The size of the complete chip including bonding pads, not shown in the micrograph, is 3.6 x 3.2 mm^2.

SQUID is not connected, the signal flux can be applied indirectly to the Smart DROS via the pickup coil, which is part of the intermediate flux transformer. On the other hand, the signal flux can always be applied directly to the DROS via a one-turn coil on top of the signal SQUID washer.

For testing purposes, also chips with separate elements of the Smart DROS, e.g., Josephson junctions, resistors, the separate DROS, the write gates, the readout SQUID and the Josephson counter, were fabricated on the same wafer as the complete Smart DROSs. In the separate Josephson counters, a readout SQUID is connected to the storage loop, since this is the only way to check its operation. Similarly to the complete Smart DROSs with a readout SQUID, this means that only low frequency measurements can be performed on the counter.

5.4.3 Fabrication process

The Smart DROSs were fabricated using the fabrication process developed at the Low Temperature Division at the University of Twente, which is based on standard photolithography using chromium photomasks and dc/rf sputtering [33,34,35,36].

All patterning is done by a lift-off process, except for the junction definition, which is done by reactive ion etching (RIE) in a fluorine containing plasma of SF_6. The first step in the lithography process is ultrasonic cleaning of the thermally oxidized Si wafers in acetone and ethanol. Then the wafer is coated with a photosensitive layer (photoresist), Shipley S1813. This layer is soft baked in an oven to improve adhesion and to remove solvent from the photoresist. In the next step, the photoresist is exposed through a photomask with ultraviolet light with an intensity of 10 W/cm^2. In order to produce an overhang structure in the photoresist mask for better lift-off properties, chlorobenzene soaking can be used and the baking time and the exposure time can be decreased and increased, respectively. In the developing process, the exposed portions of the photoresist are washed away in diluted Microposit 351 developer. Subsequently, a thin film of material is deposited and in the last step, the remaining photoresist together with the material on top of it is removed in acetone. In Table 5.2, the parameters of the lithography process are given and in Fig. 5.14, the lift-off process is briefly summarized.

For the fabrication of the Smart DROSs, five photomasks are used. The first mask is used for patterning of the trilayer, which basically consists of two superconducting Nb layers and an insulating AlO_x barrier layer in between. This layer is fabricated in a Nordiko system by subsequently dc magnetron sputtering of

Table 5.2 Parameters of the lithography process for the Smart DROSs. Explanation of the terms: (A) = acetone, (E) = ethanol, (1:5) and (1:35) = ratio of developer in water.

Mask	Cleaning [min]	Spinning [rpm, s]	Baking [min, °C]	Exposure [s]	Soaking [s]	Developing [s]
1	(A) 5, (E) 3	4000, 43	23, 90	30	90	(1:5) 23
2	(A) 5, (E) 3	4000, 43	30, 90	8	-	(1:5) 14, (1:35) 60
3	(A) 5, (E) 3	4000, 43	23, 90	30	90	(1:5) 20
4	(A) 5, (E) 3	4000, 43	30, 90	8	-	(1:5) 18
5	(A) 5, (E) 3	4000, 43	25, 90	30	90	(1:5) 23

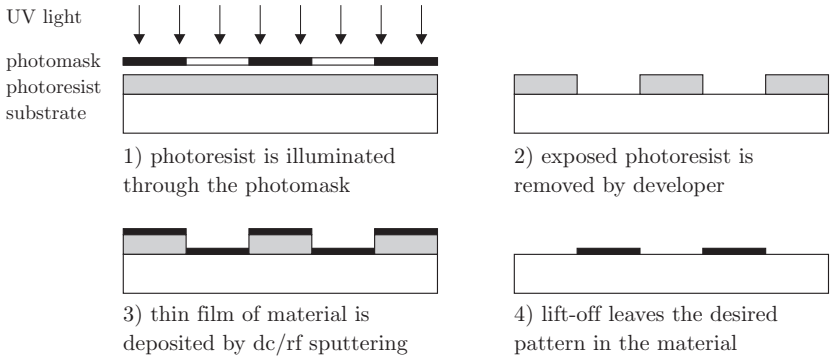

Fig. 5.14 Simplified representation of the lift-off process used for patterning the trilayer, the SiO_2 insulating layers, the Pd resistors and the Nb wiring layer, using positive photoresist.

a 150 nm thick Nb bottom electrode, a 5 nm Al layer, which is oxidized at room temperature to form the barrier layer, a second 5 nm Al layer and a 150 nm thick Nb counter electrode. Finally, a 5 nm protective Al layer is deposited on top of the trilayer. The first Al layer is used to reduce the roughness of the bottom electrode, i.e. Al can form a closed layer on top of Nb, which is known as wetting [37]. The second Al layer is used to prevent the reaction of the Nb counter electrode with the AlO_x barrier layer. The critical current density is dependent on the AlO_x thickness, which can be controlled by the O_2 pressure at which the Al layer is oxidized. Water vapor in the system is a catalyst for the oxidation process and since the partial water vapor pressure is not exactly controllable, the critical current density may vary from run to run. To prevent extreme variations in the fabrication process, the system is heated overnight at around 70 °C, to thermally degas the vacuum chamber. Presputtering is used to clean the targets and to further decrease the background pressure. Because of the getter effect [38], presputtering of Nb leads to a reduced amount of residual O_2. This has a positive effect on the quality of the deposited Nb thin films.

In the second step, the Josephson junctions are defined by RIE. Before selectively etching the Nb counter electrode in an SF_6 plasma, the Al protective layer is removed by wet etching in 1:35 diluted developer. Since in this plasma the etch rate of Al is much smaller than the etch rate of Nb, the Al layer can be used as a stopping layer. A spectrometer is used for monitoring the RIE process and for endpoint detection. When the Nb has been etched, the remaining Al,AlO_x/Al is patterned by wet etching in 1:25 diluted developer. After the junction definition, the exposed Nb layer and the junction edges are insulated by a 100 nm layer of SiO_2 using a Perkin Elmer sputtering system. The SiO_2 is rf sputtered at room temperature in a 1:10 O_2 to Ar pressure ratio using the same photoresist mask as used for RIE, so it is self-aligned. Since one layer of 100 nm SiO_2 does not give sufficient insulation, a second layer of 200 nm SiO_2 is deposited. For this step, the third photomask is used.

The fourth photomask for the fabrication is the mask in which the Pd resistors are defined. The sheet resistance of the 75 nm Pd layer is $R_\square = 1\ \Omega$. To improve the adhesion of the Pd layer to the substrate, a thin 2 nm Al layer is deposited

Table 5.3 Parameters of the sputtering, Al oxidation and RIE etching process for the Smart DROSs. Explanation of the terms: dc/rf = dc or rf sputtering/etching, rate = sputter/etch rate, t = process duration, P_b = background pressure, P_g = pressure of the gas (Ar for sputtering of Nb, Al and Pd, Ar/O_2 for SiO_2, O_2 for the Al oxidation and SF_6 for RIE etching), P = sputtering/etching power, V = negative self-bias voltage, i.e. target voltage, V_b = negative bias voltage of the substrate in case of bias sputtering.

Mask	Mat./process [nm]	dc/rf	rate [nm/min]	t [min]	P_b [mbar]	P_g [mbar]	P [W]	V [V]	V_b [V]
1	Nb, 150	dc	80	1:55	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	250	325-350*	-
	Al, 5	dc	26	0:12	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	75	395	-
	Al oxidation	-	-	60	$\leq 1{\cdot}10^{-7}$	100**	-	-	-
	Al, 5	dc	26	0:12	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	75	395	-
	Nb, 150	dc	80	1:55	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	250	325-350	-
	Al, 5	dc	26	0:12	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	75	395	-
2	RIE etching	rf	60	8:30	$\leq 7{\cdot}10^{-7}$	$5.0{\cdot}10^{-2}$	20	100	-
	SiO_2, 100	rf	3.3	30	$\leq 2{\cdot}10^{-6}$	$2.9{\cdot}10^{-2}$	350	250-330	-
3	SiO_2, 200	rf	3.3	60 + 5	$\leq 2{\cdot}10^{-6}$	$2.9{\cdot}10^{-2}$	350	250-330	90***
4	Al, 2	dc	26	0:05	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	75	395	-
	Pd, 75	rf	21	3:30	$\leq 1{\cdot}10^{-7}$	$1.3{\cdot}10^{-2}$	450	1100	-
5	Nb, 350	dc	80	4:20	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	250	325-350	-
	Al, 5	dc	26	0:12	$\leq 1{\cdot}10^{-7}$	$7.3{\cdot}10^{-3}$	75	395	-

* Due to ageing of the Nb-target, this voltage decreases in time.
** The O_2 pressure at which the Al is oxidized determines the critical density J_c.
*** To improve the step coverage, an additional 5 minutes bias sputtering step is used.

prior to the Pd deposition. Finally, the wiring layer of 350 nm Nb is deposited. In this layer, e.g., the input coils are defined. A thin 5 nm layer of Al protects this layer. In Table 5.3, the parameters of the processes are summarized.

Compared to single dc SQUIDs and two-stage SQUID systems, the complexity of the Smart DROS is much higher. The large number of coils on top of the washers results in a large area in which the Nb bottom layer and the Nb wiring layer are lying on top of each other. Because of the large area, the probability of shorts through the insulating SiO_2 layers is for the Smart DROS much higher than for simple dc SQUID designs. Therefore, an important step in the fabrication is the insulation of the junctions and the Nb bottom layer. During the fabrication of the first wafers, it turned out that the quality of the rf sputtered SiO_2 was not high enough to give sufficient insulation.

It is well known that for sputtering high quality SiO_2 besides Ar additional O_2 has to be introduced to prevent the formation of SiO. High-quality films can be grown using O_2 mixing ratios, $O_2/(O_2+Ar)$, typically larger than 5 % [39,40]. For these mixing ratios, the breakdown field of SiO_2 films sputtered in an O_2-Ar mixture can reach the same level as thermal dioxide films [41,42]. For O_2 mixing ratios larger than 5 %, the quality of the SiO_2 does not really improve anymore. However, for large O_2 mixing ratios, the probability of burning the photoresist mask increases. Especially for the self-aligned mask that has to withstand several process

steps, this can cause a problematic lift-off. The insulating quality of the SiO_2 layers that were rf sputtered at the University of Twente in a 1:10 O_2 to Ar ratio, i.e. 9 % O_2 mixing ratio, was not sufficient for the Smart DROSs. To improve insulation, bias sputtering has been used. In this case, the substrate is negatively biased, which provides an acceleration zone for the plasma ions close to the sample. This causes a mixture of sputtering and etching, i.e. deposition and redeposition, and results in better step coverage, thus smoother layers without pinholes. Using an additional 5 minutes bias sputtering step, SiO_2 films with high insulating quality were deposited which were used in the fabrication of the Smart DROSs.

For the formation of SiO_2 also other techniques can be used, such as thermal oxidation of Si or chemical vapor deposition (CVD) [43]. However, these techniques cannot be used at room temperature. Thermal oxidation is achieved by heating the wafer to a high temperature, typically 900 to 1200 °C, in an atmosphere containing either pure oxygen or water vapor. CVD is based on thermal decomposition and/or reaction of gaseous compounds. The desired material is deposited directly from the gas phase onto the wafer. The use of relatively high temperatures results in excellent step coverage for this technique. There are different types of CVD, of which plasma-enhanced CVD (PECVD) has the advantage that it can be used at relatively low temperatures, 100 to 400 °C. The photoresist and the Josephson junctions however, cannot withstand temperatures higher than roughly 150 °C, so that these techniques cannot be used for the fabrication of SQUIDs.

When the deposited SiO_2 layers have good insulating quality with good step coverage, problems in the lift-off can still cause shorts between the Nb bottom layer and the Nb wiring layer. Even when using an overhang structure in the photoresist, lift-off is often not complete, i.e. so-called rabbit ears remain along the edges of the photoresist. To remove the rabbit ears and to prevent shorts through the insulating layers, mechanical cleaning with a lens tissue and acetone is often needed.

5.5 Experimental characteristics of the Smart DROS

Because of problems in the fabrication of high quality SiO_2 layers, many non-operating chips were fabricated. Only a few Josephson counters and Smart DROSs were free of shorts and were operating properly. In this section, the measurements on these devices are presented. The test elements, such as Josephson junctions, the resistors and the separate write gates, were characterized using the same measurement techniques and setup as used for the measurements described in the chapters 3 and 4. The measured SQUID inductance of the write gate and the mutual inductance with its input coil are summarized in Table 5.1. The estimated SQUID inductances and the experimental values correspond quite well. Using FastHenry however, the mutual inductance is estimated more accurately.

5.5.1 Experimental characteristics of the Josephson counter

The critical current of the 4 x 8 μm^2 Josephson junctions of the write gates in the Josephson counter was measured to be $I_0 \approx 18$ μA, which is about twice the design value. The sheet resistance was about 20 % smaller than the design value.

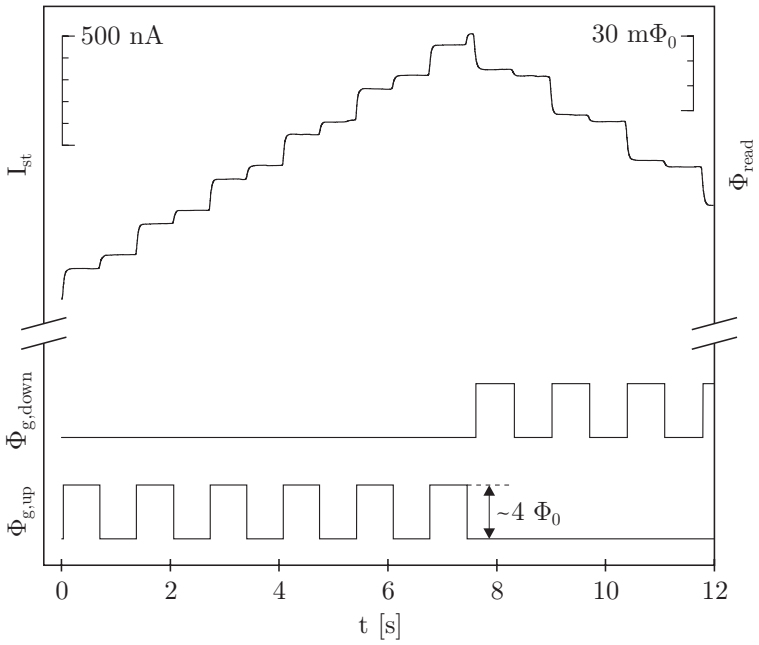

Fig. 5.15 Measured response of a Josephson counter to flux pulses applied alternately to the up-gate and the down-gate. The bias current of the counter was $I_{b,count} \approx 15$ μA. Φ_{read} is the flux induced in the readout SQUID. The vertical offsets are arbitrary.

The Josephson counters were tested by applying test voltage pulses to the write gates and monitoring the circulating current in the storage loop with the readout SQUID. The readout SQUID with a single-turn feedback coil was operated with direct voltage readout FLL electronics. In this case, the sensitivity was limited by the preamplifier noise, but this was not a problem for characterizing the Josephson counters. The counters were electromagnetically shielded by a Nb can and all the wires between the room temperature electronics and the chips at 4.2 K were low pass filtered to prevent radio frequency interference (RFI) [44,45].

In order to generate voltage pulses that can be applied to the write gates, three function generators were used. One function generator served as a trigger for the two other function generators, i.e. when the output voltage of the 'trigger' function generator was positive, the 'up' function generator produced voltage pulses and when the output voltage was negative, the 'down' function generator produced voltage pulses. The voltage pulses of the 'up' and 'down' function generators were coupled to the up-gate and the down-gate respectively, generating flux pulses in the write gates.

Figure 5.15 shows the experimental response of a Josephson counter to voltage pulses with a peak-to-peak amplitude of 18 mV. The total resistance in the wires to the input coils of the write gates was 1.67 kΩ and the measured mutual inductance of the input coils with the write gates was $M_{in,g} = 820$ pH, thus the peak-to-peak amplitude of the flux pulses was (18 mV/1.67 kΩ)(820 pH) $\approx 4\ \Phi_0$. Each flux pulse produced a flux change in the storage loop of the counter of exactly $4\ \Phi_0$.

Comparing the measurements with the simulations shown in Fig. 5.5, one can see a remarkable difference. The step in the circulating current corresponding to writing a flux quantum (or multiple flux quanta) to the write gate and the step that is related to transferring the flux quantum from the write gate to the storage loop are equal in the simulations, i.e. $\delta I_{st}/2$. In the measurements, the steps are not equal and small and large steps alternate. The discrepancy is caused by crosstalk between Φ_g and the readout SQUID. Hence, a parasitic signal was measured by the readout SQUID even when the bias current of the Josephson counter was zero. By subtracting this parasitic signal from the measurements shown in Fig. 5.15, the proper operation of the counters could be verified. In a Smart DROS, this crosstalk does not harm the flux writing process of a flux quantum to the storage loop, since during this process the flux Φ_g increases from zero and decreases to zero again. In other words, during the flux writing process of a flux quantum to the storage loop, the change in the circulating current δI_{st} is not influenced by the crosstalk.

The circulating current in the storage loop of the Josephson counter can be calculated from $I_{st} = \Phi_{read}/M_{in,read}$, where Φ_{read} represents the flux that is induced in the readout SQUID and $M_{in,read}$ is the effective mutual inductance between the readout SQUID and the storage loop. This mutual inductance was measured to be $M_{in,read} = 182$ pH. From the experimental quantization unit of the circulating current, $\delta I_{st} = 48$ nA, and using Eq. (5.10), the inductance of the storage loop of the counter was calculated to be $L_{st} = 43$ nH. This value is only marginally smaller than the analytically calculated and the numerically extracted values, see Table 5.1.

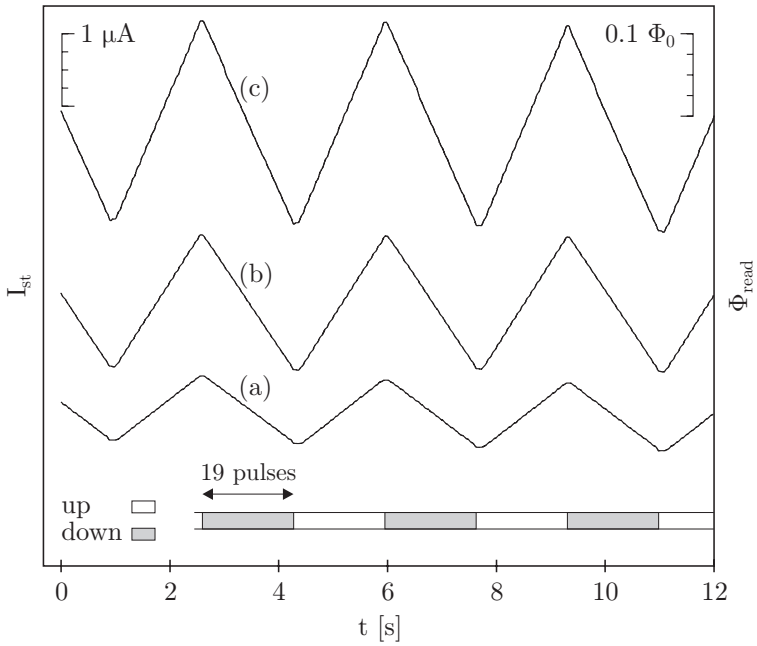

Fig. 5.16 Measured response of a Josephson counter to pulse trains of 19 flux pulses applied alternately to the up-gate and the down-gate: For trace (a), the peak-to-peak amplitude of the flux pulses was ~1 Φ_0, for trace (b) ~2 Φ_0 and for trace (c) ~3 Φ_0. The vertical offsets are arbitrary.

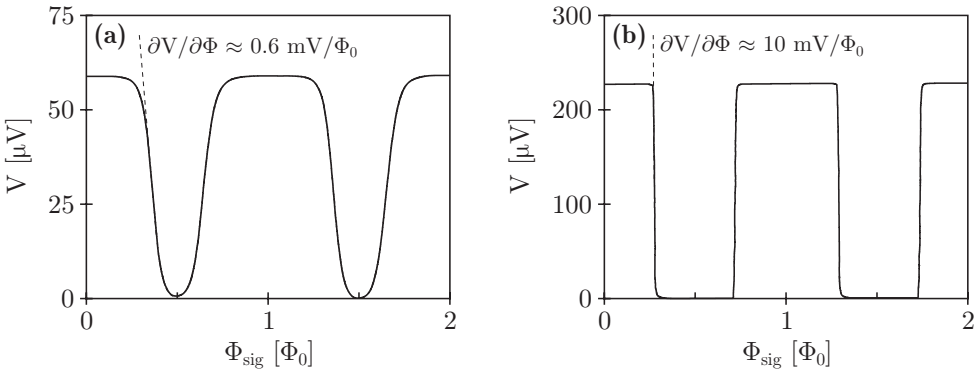

Fig. 5.17 Experimental flux-to-voltage characteristics of a Smart DROS operated in open loop, i.e. the Josephson counter was not operating. The bias current of the DROS was **(a)** $I_{b,dros} \approx 29$ μA and **(b)** $I_{b,dros} \approx 108$ μA. The critical current density and the sheet resistance corresponded to the design values[v].

Figure 5.16 shows the experimental response of the Josephson counter to pulse trains of 19 pulses applied to the up-gate and the down-gate. The frequency of the function generator that supplied the trigger signal was 0.3 Hz and the pulses were applied at a frequency of ~11 Hz. The peak-to-peak amplitude of the voltage pulses was 5 mV for trace (a), 10 mV for trace (b) and 15 mV for trace (c). This corresponded to a peak-to-peak amplitude of the flux pulses of ~1 Φ_0 for trace (a), ~2 Φ_0 for trace (b) and ~3 Φ_0 for trace (c). This means that the gates wrote respectively one, two and three flux quanta to the storage loop at each pulse. The fine structure that can be seen in the measurements is caused by the flux writing process of the individual pulses to the storage loop, i.e. zooming in gives the same result as is shown in Fig. 5.15. Both measurements show that the Josephson counters operated as expected and that the measured inductance of the storage loop L_{st} corresponds to the analytically calculated and the numerically extracted values.

5.5.2 Low frequency characteristics of the (Smart) DROS

Separate test DROSs and complete Smart DROSs were characterized at 4.2 K in an electromagnetic shield of Nb. All wires between the room temperature electronics and the chips were low pass filtered to prevent radio frequency interference.

From the flux-to-voltage characteristics of the separate test DROSs, the mutual inductance between the 2 x 9½-turns feedback coil and the signal SQUID of the DROS was calculated to be $M_{fb} = 2.1$ nH, which is very close to the design value. In Fig. 5.17a, the experimental flux-to-voltage characteristic of a Smart DROS is shown. The bias current of the DROS was $I_{b,dros} \approx 29$ μA, i.e. the theoretical

[v] Due to fabrication problems related to the SiO_2 layers, several wafers were fabricated. These Smart DROSs are from a wafer with the correct critical current density and sheet resistance, but the quality of the SiO_2 layers was too low, such that the Josephson counters did not operate. The operating counters and complete Smart DROSs are from a different run, for which the critical current density was about twice the design value and the sheet resistance was 20 % smaller than the design value.

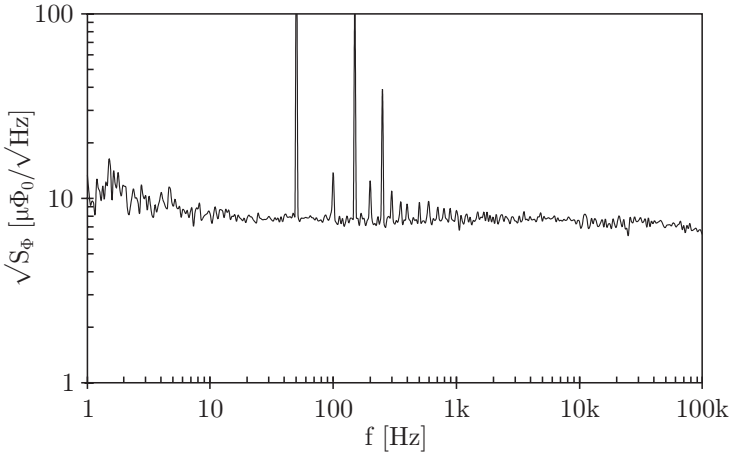

Fig. 5.18 Experimental flux noise spectrum of a Smart DROS at $T = 4.2$ K, operated in FLL using room temperature electronics. The Josephson counter did not supply any feedback flux to the DROS.

maximum operation current given by Eq. (5.1). The bias current of the Josephson counter was zero. Moreover, shorts through the insulating SiO_2 layers prevented proper operation of the Josephson counter, such that no feedback flux was supplied to the DROS [46]. The voltage modulation depth was $2\delta V = V_c \approx 60$ μV and the experimental flux-to-voltage transfer was ~0.6 mV/Φ_0. This agrees with the value that is predicted by Eq. (5.3). At larger bias currents, the DROSs still operated and the flux-to-voltage transfer increased to ~10 mV/Φ_0 at $I_{b,dros} \approx 108$ μA, as is shown in Fig. 5.17b. However, the white flux noise was much larger than at $I_{b,dros} \approx 29$ μA. The experimental flux noise spectrum of a Smart DROS operated in FLL using room temperature electronics is shown in Fig. 5.18. The bias current of the DROS was $I_{b,dros} \approx 29$ μA. The Josephson counter did not supply any feedback flux to the DROS. The experimental white flux noise level, 7.6 $\mu\Phi_0/\sqrt{\text{Hz}}$, was somewhat larger than the design value, 5.7 $\mu\Phi_0/\sqrt{\text{Hz}}$.

The behavior of the fully operating Smart DROSs was investigated by measuring the flux-to-voltage characteristics with the Josephson counter on and off. Ideally, if the bias current of the Josephson counter is zero, no feedback flux will be supplied by the counter. This means that a normal flux-to-voltage characteristic is to be expected when applying a signal flux. On the other hand, if the Josephson counter is biased with an appropriate bias current, it will generate a feedback flux that exactly cancels the applied signal flux. The Josephson counter automatically locks the system into the dynamic equilibrium where both the signal SQUID and the reference SQUID have a switching probability of 50 %, i.e. the time-averaged voltage across the reference SQUID stays constant and is independent on the applied signal flux. This was also discussed in section 5.1.2.

The experimental results of a complete Smart DROS are shown in Fig. 5.19. In this case, the flux was indirectly applied via the storage loop of the Josephson counter. No readout SQUID was connected to the storage loop. In the ideal case where noise is neglected, the Josephson counter will never count flux pulses if

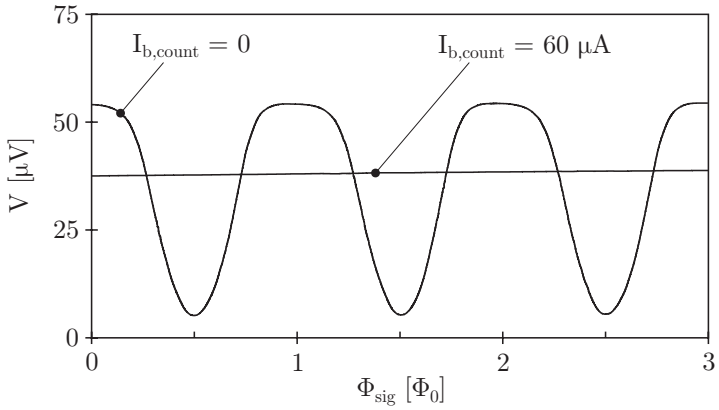

Fig. 5.19 Experimental flux-to-voltage characteristics of a complete Smart DROS operated in open loop and in flux locked loop, i.e. the bias current of the Josephson counter was respectively $I_{b,count} = 0$ and $I_{b,count} = 60$ μA. The flux was applied indirectly via the counter.

$I_{b,count} = 0$. In practical situations however, due to noise and fluctuations a small (bias) current may run and when the flux pulses are large enough, the Josephson counter can operate although no (external) bias current is supplied. Therefore, in the measurements shown in Fig. 5.19, the bias current of the DROS $I_{b,dros}$ and the reference flux Φ_{ref} were tuned such that the amplitude of the flux pulses that were coupled to the write gates was too small to cause variations in the feedback flux for $I_{b,count} \approx 0$. These settings were not the optimum settings for the DROS, such that the flux-to-voltage transfer was smaller than that of the measurements shown in Fig. 5.17. A normal flux-to-voltage characteristic was measured for $I_{b,count} = 0$ and for appropriate bias currents of the Josephson counter, the voltage across the reference SQUIDs stayed constant, as expected. This shows that, time-averaged, the Smart DROS was operating correctly. However, from the experiments described in this section, the actual bandwidth and the slew rate could not be determined. For these measurements, a high frequency readout scheme is required.

5.5.3 High frequency readout: Towards a digital readout scheme

The measurements described in the previous section, show that time-averaged the Smart DROS was operating as expected but they do not show whether all the voltage pulses that were generated by the DROS were counted correctly by the Josephson counter. For example, when a voltage pulse has for some reason a smaller amplitude than expected, there is a possibility that no flux quantum is written to the storage loop, which could cause a relative drift and low frequency excess noise [18,19]. To investigate the behavior of the Smart DROS in more detail, high frequency measurements were done using broadband preamplifiers, a spectrum analyzer and digital oscilloscopes with real-time sample rates up to 20 GSa/s. A scheme of the setup that was used for high frequency characterization of the separate test DROSs and the Smart DROSs is shown in Fig. 5.20.

Two chips were glued on an epoxy printed circuit board (PCB) and were connected to the transmission lines on the PCB. These transmission lines were

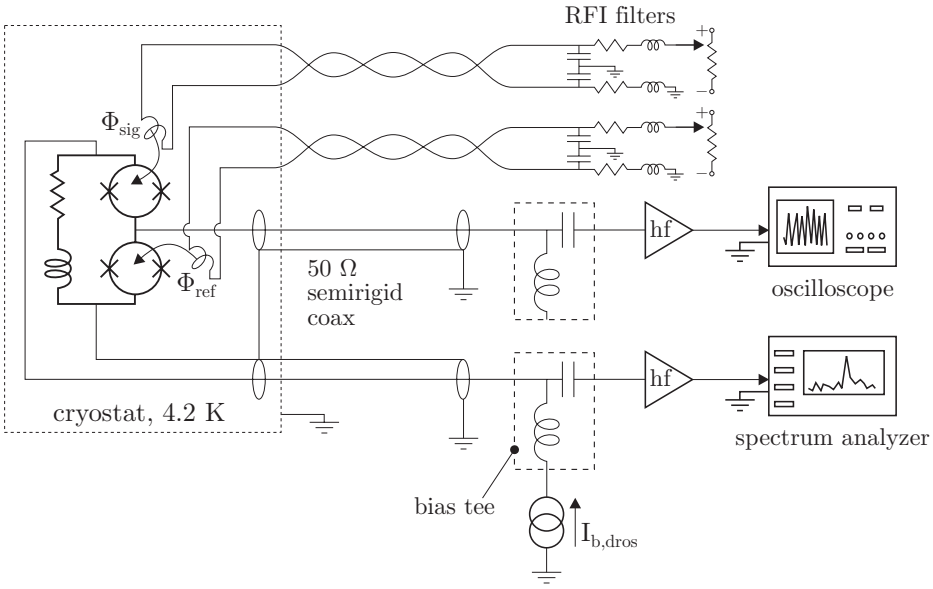

Fig. 5.20 Measurement setup for high frequency characterization of the separate test DROSs and the complete Smart DROSs. The power spectral density and the individual voltage pulses were measured either across the complete DROS or across the reference SQUID.

connected to 50 Ω semirigid coaxial cables by means of subminiature A (SMA) connectors. Two Mini-Circuits ZFBT-6G bias tees [47] were used to split the ac and the dc signals and to dc decouple the chips from the spectrum analyzer and the digital oscilloscope. In this way, the semirigid coaxial cables could be used both to supply the bias current to the DROS and to transfer the output signal of the DROS to the room temperature electronics. The wires between the coils of the DROS, i.e. the input coil and the coil on top of the reference SQUID, and the room temperature electronics were low pass filtered to prevent degradation due to RFI. Obviously, the semirigid coaxial cables were not filtered since these had to transfer the high frequency output signal of the Smart DROS.

In Fig. 5.21a, the power spectral density S of the fundamental and higher harmonics of a separate test DROS is shown. For these measurements, the high frequency output signal of the DROS was preamplified by an HP 83006A microwave system amplifier with a gain of ~20 dB and a frequency range of 10 MHz to 26.5 GHz. The amplified voltage pulses were coupled to an HP 8563E spectrum analyzer. The corresponding voltage pulses measured in time by a Tektronics TDS 7404 Digital Phosphor Oscilloscope (DPO) with a real-time sample rate of 20 GSa/s are shown in Fig. 5.21b. Taking the gain of the preamplifier into account, it can be concluded that the measured amplitude of the voltage pulses is somewhat larger than the simulated 0.4 mV. Since the amplitude of the voltage pulses is approximately $\frac{3}{2} I_0 R_{d,eff}$, the larger amplitude is caused by the fact that the experimental critical current density was larger than designed. Both measurements experimentally confirm the correct relaxation oscillation frequency and show that the transmission losses are negligible for these relaxation oscillation frequencies. The

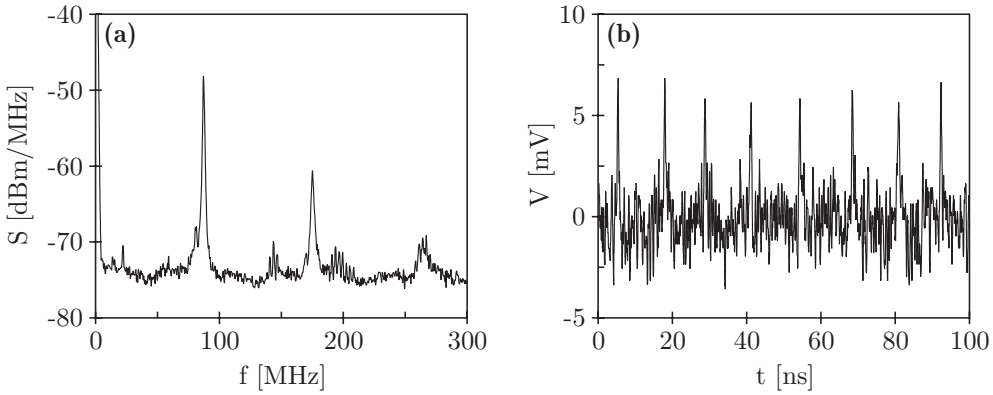

Fig. 5.21 (a) Spectrum of the output voltage across a separate test DROS. **(b)** Amplified voltage pulses measured in time. For both measurements, the bias current of the DROS and the reference flux were adjusted for maximum output of the DROS. The vertical axes have not been corrected for the gain of the preamplifier, ~20 dB.

experimental relaxation oscillation frequency of the DROS was ~90 MHz when the bias current and the reference flux were adjusted to give maximum output. Together with the measured inductance of the storage loop of the Josephson counter, $L_{st} = 43$ nH, and the measured mutual inductance between the feedback coil and the signal SQUID of the DROS, $M_{fb} = 2.1$ nH, the maximum flux slew rate of the Smart DROS can be calculated as $\partial\Phi_{sig}/\partial t = (M_{fb}/L_{st})\Phi_0 f_{RO} \approx 5{\cdot}10^6\ \Phi_0$/s, which corresponds to the designed flux slew rate.

The broadening of the peaks in the spectrum of the output voltage is caused by spectral impurity of the relaxation oscillation frequency. Consequently, the peak height also decreases and in some cases, the output signal almost drowned in the system noise. As is shown in Fig. 5.22, this was especially the case for the complete Smart DROSs, which were measured in the same way as the separate DROSs.

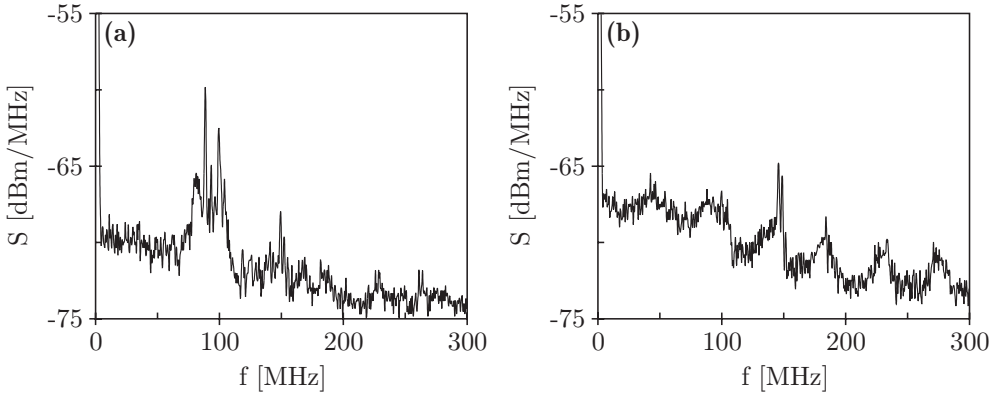

Fig. 5.22 Spectra of the output voltage across the reference SQUID of a complete Smart DROS operated in open loop and flux locked loop, i.e. the bias current of the Josephson counter was respectively **(a)** $I_{b,count} = 0$ and **(b)** $I_{b,count} = 60$ μA. The signal flux was applied indirectly via the counter.

These measurements show the power spectral density of the output voltage measured across the reference SQUID of the DROS and were performed using the same chip and the same settings as used for the low frequency characterization of the Smart DROS, shown in Fig. 5.19. For Fig. 5.22a, the bias current of the Josephson counter was $I_{b,count} = 0$ and thus no feedback flux was supplied by the counter. The signal flux Φ_{sig} was in this case adjusted such that $I_{c,sig}(\Phi_{sig}) > I_{c,ref}$, i.e. only the reference SQUID was participating in the relaxation oscillations at a frequency $f_{RO} \approx 90$ MHz. For Fig. 5.22b, the bias current of the Josephson counter was $I_{b,count} = 60$ μA and the Josephson counter locked the system in the dynamic equilibrium where $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$ and where both the signal SQUID and the reference SQUID have a switching probability of 50 %. As a result, the voltage pulses across the reference SQUID appeared at half the relaxation oscillation frequency, about 45 MHz, as expected.

An explanation for the additional broadening of the peaks and the additional small peaks in the measurements shown in Fig. 5.22, is that possibly the Josephson counter was not counting each individual voltage pulse generated by the DROS, i.e. the signal SQUID and reference SQUID were not oscillating exactly in turn. However, the broadening can also be caused by noise, e.g. degradation due to RFI since no filtering was used in the semirigid coaxial cables or due to transmission line resonances. Moreover, as was discussed above, the bias current of the DROS $I_{b,dros}$ and the reference flux Φ_{ref} were tuned such that the amplitude of the voltage pulses that were coupled to the write gates was too small to cause variations in the feedback flux for $I_{b,count} \approx 0$. These settings were not the optimum settings for the characteristics of the DROS, e.g. for the amplitude of the voltage pulses and the noise characteristics, and also resulted in broadening of the peaks in the spectra.

To study the behavior of the Smart DROS in more detail, e.g. slew rate, bandwidth and noise properties, a digital readout scheme can be used [7,48]. The

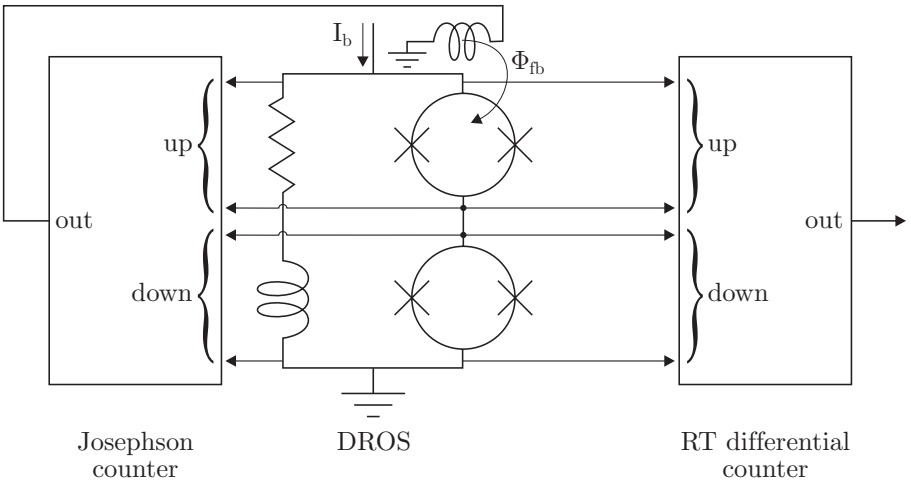

Fig. 5.23 Schematic overview of the Smart DROS with digital readout. The Josephson counter supplies the feedback flux at 4.2 K and the differential counter at room temperature counts the effective number of pulses, $N_{sig} - N_{ref}$.

schematic overview of this readout scheme is shown in Fig. 5.23. The differential counter at room temperature counts the effective number of pulses, $N_{sig} - N_{ref}$, and is used to reconstruct the applied signal. Here, N_{sig} represents the number of pulses generated by the signal SQUID and N_{ref} is the number of pulses across the reference SQUID, see also section 5.1.2. However, based on the measurements described above, it can be concluded that the amplitude of the output voltage pulses generated by the optimized Smart DROS would be too small if a digital readout scheme would be used similar to the measurement setup presented in Fig. 5.20.

One of the possibilities to improve the ability to use a simple digital readout scheme for the Smart DROS, e.g. using a commercially available differential counter [49] and low-cost preamplifiers [50] at room temperature, is to increase the amplitude of the voltage pulses that are generated by the Smart DROS. As was discussed in section 5.3.1, the amplitude of the voltage pulses is about $\frac{3}{2} I_0 R_{d,eff}$. Therefore, the effective damping resistor should be as large as possible within the requirement given by Eq. (5.6), i.e. the damping parameter should be $D = 1$. From Eq. (5.6), it can be concluded that the shunt inductance L_{sh} and the SQUID

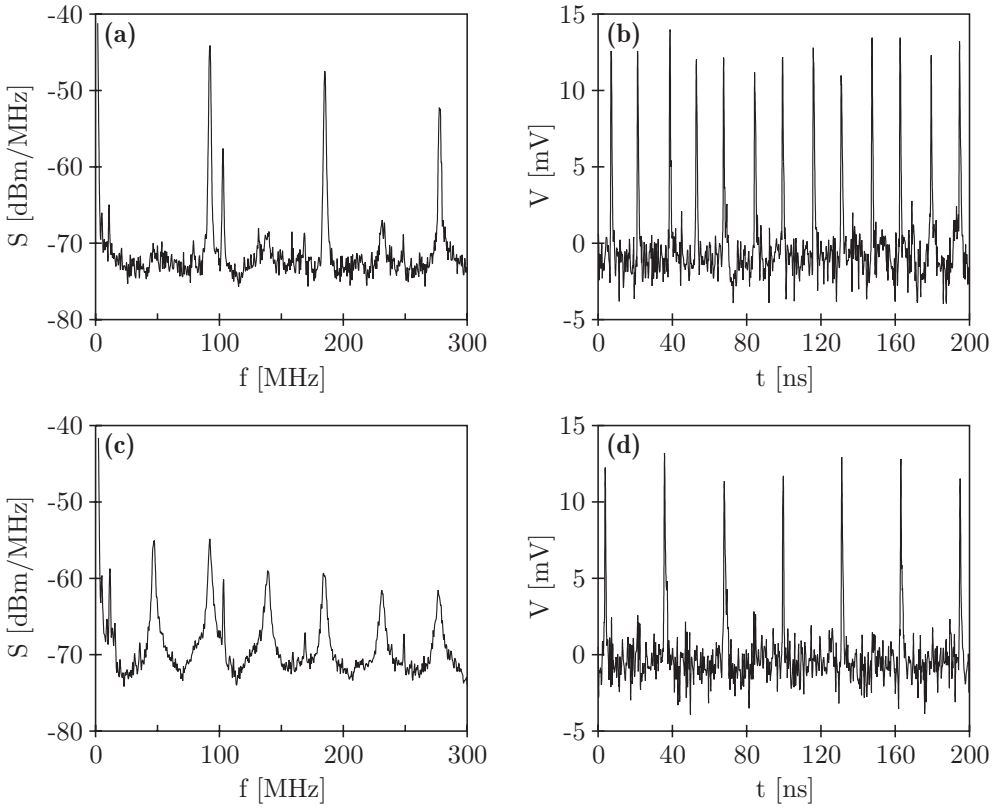

Fig. 5.24 Spectra of the output voltage across the reference SQUID of a separate DROS and the voltage pulses measured in time. The signal flux was adjusted such that $I_{c,sig}(\Phi_{sig}) > I_{c,ref}$ for **(a)** and **(b)** and $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$ for **(c)** and **(d)**. The small peaks in the spectra slightly above 100 MHz were caused by environmental noise.

capacitance C_{sq} are the parameters that determine the maximum damping resistance. These parameters are more or less fixed by the chosen relaxation oscillation frequency and the fabrication process, e.g. the fabrication process determines the minimum junction area and thus the minimum value for C_{sq}. Hence, one possibility to increase the amplitude of the voltage pulses is to decrease the junction area. This will be discussed in the next chapter.

Another possibility to increase the amplitude of the voltage pulses is to increase the critical current I_0 of the junctions of the DROS. However, I_0 is fixed by the design rule $\beta_{L,sig} = 2I_0L_{sq,sig}/\Phi_0 \approx 1$, thus it can only be increased by decreasing the SQUID inductance of the DROS. In order to show the possibility to improve the amplitude of the voltage pulses of the DROS by decreasing the SQUID inductance, a separate DROS was measured with an inductance of $L_{sq,sig} = 75$ pH. The critical current of the 4 x 4 μm^2 Josephson junctions was $I_0 = 30$ μA. The relaxation oscillation frequency was 100 MHz [6,7].

The measured spectra of the output voltage across the reference SQUID and the voltage pulses generated by the reference SQUID are shown in Fig. 5.24. For these measurements, the same setup as above was used, except for the digital oscilloscope. For measuring the voltage pulses in time, an HP 54845A Infiniium digital oscilloscope with a real-time sample rate of 8 GSa/s was used. As the measurements show, only the reference SQUID was participating in the relaxation oscillations for $I_{c,sig}(\Phi_{sig}) > I_{c,ref}$. When the signal flux was adjusted manually to make the critical currents of both SQUIDs equal, $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$, the signal SQUID and reference SQUID oscillated in turn on average, as expected. However, due to noise both SQUIDs did not oscillate exactly in turn, which caused the additional broadening and the reduced height of the peaks [51]. This is also shown in Fig. 5.25, which shows a pulse train of 1.2 μs measured across the reference SQUID at $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$. The amplitude of these voltage pulses was about twice as large

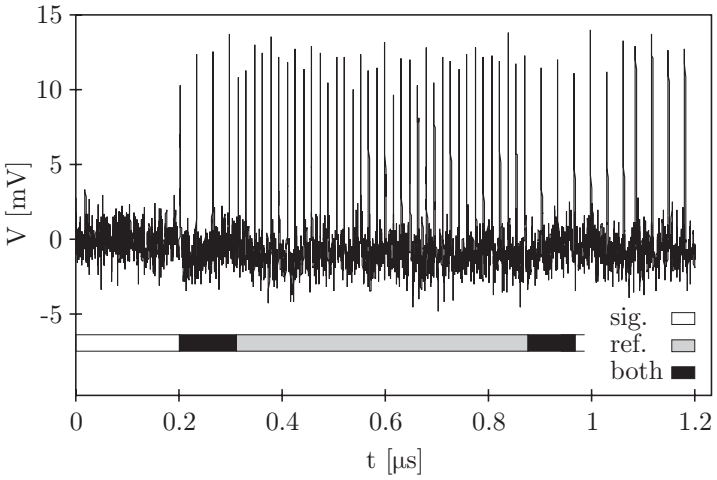

Fig. 5.25 Voltage pulse train measured across the reference SQUID of a 100 MHz separate test DROS with an inductance of $L_{sq,sig} = 75$ pH. The signal flux was adjusted such that $I_{c,sig}(\Phi_{sig}) = I_{c,ref}$. The vertical axis has not been corrected for the gain of the preamplifier.

as the amplitude of the voltage pulses of the optimized Smart DROS, which is caused by the smaller SQUID inductance and the higher critical current. Taking the gain of the preamplifier into account, the amplitude of the voltage pulses can be calculated to be ~1 mV. The voltage pulses resemble a periodic train of Dirac delta functions, such that the higher harmonics in the spectrum have a large amplitude. Since the voltage pulses are not ideal Dirac delta functions, i.e. the pulse duration is finite, the amplitude of the higher harmonics in the spectrum decreases as a function of the frequency, as is shown in Fig. 5.24a and Fig. 5.24c.

If a differential counter at room temperature with an input trigger level of 6 mV would be used, the voltage pulses could be counted. However, the input trigger level of commercial counters is typically 20 mV, which requires additional amplification of the voltage pulses. Nevertheless, these measurements show that in principle for a DROS with output voltage pulses with an amplitude of ~1 mV, with sufficient amplification and with a high-speed differential counter, the proposed digital scheme could be used for the readout of a Smart DROS.

5.6 Conclusion and discussion

The Smart DROS is a digital SQUID based on a DROS and a Josephson counter to supply the feedback flux. Because of the integration of a DROS and the complete flux locked loop circuitry on one single chip, this concept has the potential to be both very fast and very sensitive. Moreover, the relaxation oscillations of the DROS are used as an on-chip clock signal, such that no external clock is required. The prototype system that was developed by Van Duuren *et al.* proved the operation principle. However, it was not optimized with respect to the output range of the Josephson counter, the quantization unit of the feedback flux and the coupling scheme. By optimizing the Smart DROS with respect to these parameters, design rules were extracted in section 5.2.

Based on these design rules and numerical analysis, an optimized Smart DROS with a relaxation oscillation frequency of 100 MHz was designed and fabricated. The measured SQUID inductance of the DROS was $L_{sq,sig} = 280$ pH and the quantization unit of the feedback flux was ~50 mΦ_0, calculated from the experimental values for the inductance of the storage loop of the Josephson counter, $L_{st} = 43$ nH, and the mutual inductance between the feedback coil and the signal SQUID of the DROS, $M_{fb} = 2.1$ nH. The maximum flux slew rate based on these parameters was thus calculated to be $\partial\Phi_{sig}/\partial t = (M_{fb}/L_{st})\Phi_0 f_{RO} \approx 5{\cdot}10^6\ \Phi_0$/s. This is more than two orders of magnitude higher than the maximum flux slew rate of the prototype, which was $2{\cdot}10^4\ \Phi_0$/s [7]. Moreover, this is the highest slew rate that has been achieved for digital SQUIDs at the moment.

The measurements that were described in section 5.5 show that the Josephson counters that were fabricated, operated as designed and that all inductances in the Smart DROS corresponded very well to the numerically extracted values. It can be concluded that FastHenry is a useful tool for the numerical extraction of inductances from a layout. Also the working formulas given by Ketchen proved to give a good estimation of the inductances when the SQUID washer is completely

covered by the input coil. The complete Smart DROSs were characterized using both low frequency and high frequency measurement techniques. The measurements showed that, time-averaged, the Smart DROSs were operating properly.

In order to profit from the full potential of the Smart DROS and to become a device of real practical value, a Smart DROS with a digital readout is required. Although the first steps towards a digital readout scheme were made by using room temperature broadband amplifiers and a digital oscilloscope with a high real-time sample rate, this has not been accomplished yet. Amplification of the voltage pulses generated by the DROS without introducing additional noise is one of the most important topics in the development of a digital readout mode. Amplification at cryogenic temperatures has the advantage that the Smart DROS and the coaxial transmission lines can be decoupled, which prevents degradation of the Smart DROS characteristics due to transmission line resonances. A cryogenic high electron mobility transistor (HEMT) high frequency amplifier is a promising candidate [52,53]: HEMTs operating at 4.2 K have been reported with white noise levels below 0.5 nV/$\sqrt{\text{Hz}}$ and with a power supply of only 9.5 μW [54]. Another option is to use series arrays of Josephson junctions as a voltage driver to amplify the output voltage pulses of the Smart DROS [19,53]. The advantage of using a junction array is that it can be integrated on the same chip as the Smart DROS.

Instead of using a room temperature differential counter for the readout of the Smart DROS, the digital data processing can also be performed either partly or completely at cryogenic temperatures. For example, dedicated CMOS chips operating at cryogenic temperatures can be designed which convert the pulses generated by the Smart DROS to bits, e.g. a voltage pulse across the signal SQUID is '1' and a voltage pulse across the reference SQUID is '0'. The bits can be combined to bytes and can be transferred in parallel from the chip to room temperature, where further data processing can be performed to reconstruct the signal that is applied to the Smart DROS. Performing the complete readout at cryogenic temperatures on one chip can be the next step. The main advantage of a completely cryogenic digital readout scheme is that for most applications no coaxial transmission lines are required but simple wires can be used. Either the readout function can be performed by a separate chip or by one single chip can be used to supply the feedback flux and to read out the Smart DROS. This readout chip can either be implemented in superconducting electronics, e.g. based on rapid single flux quantum (RSFQ) logic, or in semiconductor electronics [55]. However, the interfacing problems between room temperature electronics and RSFQ logic, the complexity of the FLL circuitry when using RSFQ [56] and the advances made in semiconductor electronics [57] might favor semiconductor electronics. On the other hand, compared to RSFQ, the power consumption of semiconductor electronics is much larger [58].

Bit errors in an optimized Smart DROS with a digital readout scheme might cause additional low frequency noise [19]. Bit errors occur, for example, when the write gates fail to write a flux quantum to the storage loop of the Josephson counter or when the room temperature differential counter fails to count a voltage pulse. Moreover, the spectral impurity of the relaxation oscillation frequency might cause errors in the reconstruction of the signal when assuming that the voltage

pulse period is constant. The effects of the spectral impurity and the bit errors have to be studied during the further development of a digital readout scheme.

In order to make the development of a digital readout scheme easier, the relaxation oscillation frequency of the optimized Smart DROS was limited to 100 MHz, as was described in this chapter. However, to outperform analogue SQUID systems, Smart DROSs based on relaxation oscillation frequencies in the GHz range have to be developed, since the achieved flux slew rate of $5{\cdot}10^6$ Φ_0/s is only marginally larger than, e.g., the best dc SQUID systems based on ac flux modulated FLL electronics [59,60]. As is discussed in the next chapter, reducing the junction area allows flux slew rates for the Smart DROS up to 10^8 Φ_0/s. Together with the possibility to use multiplexing for the readout of multiple digital SQUIDs at cryogenic temperatures without breaking the feedback loop [4,5], this opens new possibilities for, e.g., the readout of fast cryogenic particle detectors and measurements in unshielded environments. Moreover, reducing the junction area allows an increase in the amplitude of the voltage pulses, as was discussed in section 5.5.3. Together with the development of a digital readout scheme following the recommendations given above, this can result in a digital SQUID system that surpasses every analogue dc SQUID system both in sensitivity and in slew rate.

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[50] For example: Mini-Circuits ZJL-6G low-cost broadband amplifiers with a specified bandwidth of 2-6000 MHz and a typical gain of 13 dB.
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Chapter 6

Low-T_c ramp-type junctions for SQUIDs

In the previous chapters, the operation principle, the design and the fabrication of two-stage SQUID systems and Smart DROSs were discussed. The experiments on these SQUIDs showed proper operation and one of the recommendations to further improve the characteristics, e.g. noise properties and maximum flux slew rates, was to decrease the area of the Josephson junctions.

In this chapter, the need for sub-μm^2 Josephson junctions [1] to further improve the performance of SQUIDs is discussed in more detail, concentrating on the two-stage SQUID system and the Smart DROS. In section 6.1.1, the possibility to reduce the white flux noise of a two-stage SQUID system using small-area Josephson junctions is discussed and in section 6.1.2 it is shown that using sub-μm^2 junctions for the Smart DROS in principle flux slew rates up to 10^8 Φ_0/s can be achieved. In order to reduce the effective area of low-T_c Josephson junctions, several techniques based on, e.g., chemical mechanical polishing [2,3] or spin-on glass planarization [4], anodization techniques [5,6], electron beam direct writing [7,8], focused ion beam implantation [9,10] or focused ion beam milling [11,12] have been studied intensively. Another useful technique for the fabrication of small-area Josephson junctions utilizes an edge geometry. This so-called ramp-type configuration is widely used for high-T_c Josephson junctions [13]. An important advantage of this technology is that very small junction areas can be achieved without requiring high-resolution photolithography, which makes the ramp-type configuration very attractive for the fabrication of sub-μm^2 low-T_c Josephson junctions. In section 6.2, the fabrication process and the experiments on Nb/Al,AlO_x/Al/Nb ramp-type junctions are presented. As is discussed, the process that was used resulted in non-hysteretic Josephson junctions and although the first steps towards SQUIDs based on sub-μm^2 junctions were made, further research is required to improve the junction characteristics.

6.1 Small-area Josephson junctions for SQUIDs

Superconductor-insulator-superconductor (SIS) Josephson tunnel junctions with an area smaller than 1 μm^2 are increasingly used for many applications because of their low capacitances and short switching times. These applications include, e.g., rapid single flux quantum (RSFQ) logic [14], single electron circuits [15] and quantum computing [16]. However, also analogue and digital SQUIDs benefit from scaling down the size of Josephson junctions [17,18,19,20], as is discussed in this section.

6.1.1 Two-stage SQUID systems with very low noise

In chapter 4, the two-stage SQUID system based on a DROS was discussed as a SQUID with an on-chip cryogenic low-noise preamplifier. An important conclusion that was drawn, was that the overall sensitivity of these two-stage SQUID systems was determined by the sensor SQUID and not by the DROS or the readout electronics. This means that the overall system noise level can be further improved by reducing the noise level of the sensor SQUID. Since a conventional resistively shunted dc SQUID was used as a sensor SQUID, the remainder of this section concentrates on the dc SQUID.

As was discussed in section 2.2.2, the white flux noise of a dc SQUID at 4.2 K is mainly caused by thermal noise in the shunt resistors and is given by

$$S_\Phi \approx \gamma \frac{2k_B T L_{sq}^2}{R}, \tag{6.1}$$

where the screening parameter was assumed to be $\beta_L = 1$. In this equation, $\gamma \approx 8$, T is the temperature, L_{sq} is the SQUID inductance and R is the shunt resistance. We can conclude that the noise of a dc SQUID can be reduced by increasing the shunt resistance. However, in most practical applications the junction hysteresis has to be removed, which means that the McCumber parameter should be smaller than unity. Consequently, the shunt resistance can be increased as long as the condition $\beta_C = 2\pi I_0 R^2 C_j / \Phi_0 < 1$ is fulfilled.

By eliminating the shunt resistance R from Eq. (6.1), the energy resolution of a dc SQUID, $\varepsilon = S_\Phi / 2L_{sq}$, can be written as

$$\varepsilon \approx \gamma k_B T \sqrt{\frac{\pi L_{sq} C_j}{\beta_C}}. \tag{6.2}$$

This equation clearly shows that for a fixed value of β_C, decreasing the junction capacitance C_j, and thus the junction area, allows the energy resolution to be improved. In other words, by reducing the junction capacitance, the value of the shunt resistance can be further increased. The minimum junction capacitance that can be achieved however, is limited by the junction fabrication technology. Reducing the SQUID inductance L_{sq} also improves the energy resolution. However, as the effective flux capture area reduces when the SQUID inductance is decreased, in most practical applications the SQUID inductance cannot be made too small [21]. Since the operation temperature is generally fixed, e.g. $T = 4.2$ K, this means that reducing the junction capacitance is in practice the most convenient way to improve the energy resolution of a dc SQUID.

Figure 6.1 shows a contour plot of the energy resolution of a conventional resistively shunted dc SQUID at 4.2 K as a function of the junction capacitance C_j and the SQUID inductance L_{sq}. The energy resolution was calculated using Eq. (6.2) and the screening parameter was fixed at $\beta_L = 1$. The McCumber parameter was $\beta_C = 0.3$. This plot clearly shows the advantageous effect of reducing the junction capacitance as was also discussed above.

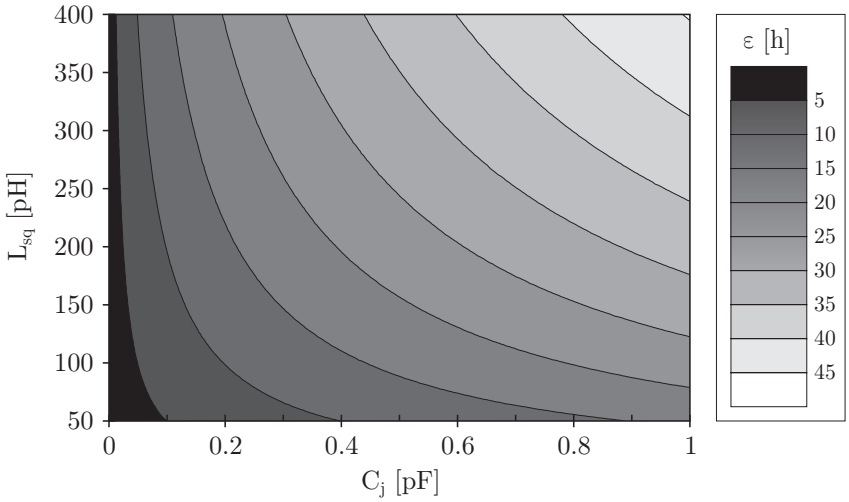

Fig. 6.1 Contour plot of the energy resolution of a dc SQUID at $T = 4.2$ K as a function of the junction capacitance C_j and the SQUID inductance L_{sq}. The screening parameter is $\beta_L = 1$ and the McCumber parameter is $\beta_C = 0.3$.

6.1.2 Smart DROSs with very high slew rates

As was discussed in section 5.1.1, a DROS consists of two hysteretic dc SQUIDs in series shunted with an *R-L* circuit. This means that when shunting the junctions with a resistance R, its value should be chosen such that the hysteresis in the *I-V* characteristics is not removed. As was discussed in section 2.1.2, the amount of hysteresis is described by the McCumber parameter β_C that follows from the widely used RCSJ (resistively and capacitively shunted junction) model [22,23]. The McCumber parameter is the ratio of the internal RC_j time to the period of the Josephson oscillation corresponding to the voltage $<V> = I_0R$. The amount of hysteresis is reduced when the RC_j time, and thus the junction area, is decreased.

In order to analyze the behavior of unshunted small-area Josephson junctions, the RCSJ model can be used, in which an ideal Josephson junction is shunted with a linear normal state resistance R_N and a capacitance C_j. According to the BCS theory, the critical current I_0 of a Josephson junction is related to the normal state resistance R_N and the gap voltage V_g. For junctions based on Nb/Al,AlO_x/Al/Nb technology operating at $T < 0.5\ T_c$, this relation is given by [24,25]

$$I_0 \approx 0.7 \frac{\pi V_g}{4R_N}. \tag{6.3}$$

For typical values, $I_0 = 20$ μA and $V_g = 2.8$ mV, this means that $R_N \approx 77\ \Omega$. Thus for a junction with an area of $A = 4$ x 4 μm^2 and a capacitance of $C_j = 0.5$ pF[i], the McCumber parameter is $\beta_C \approx 2{\cdot}10^2$. However, if the junction area could be reduced

[i] The specific capacitance was assumed to be $C/A = 0.03$ pF/μm^2.

to 0.2 x 0.2 μm^2 and the capacitance would scale down with the same factor, i.e. $C_j = 1.2$ fF, and the critical current of the junction is kept constant, the junction hysteresis is removed by the normal state resistance R_N, i.e. $\beta_C \approx 0.4$. Therefore, in designing a (Smart) DROS one should take into account that reducing the junction capacitance might lead to self-shunted non-hysteretic junctions [26].

Some practical remarks have to be made to the discussion above. First of all, the specific capacitance, i.e. the capacitance per junction area C/A, depends linearly on the thickness of the AlO_x barrier layer. This means that increasing the critical current density J_c, which is required for small-area junctions, leads to an increased specific capacitance. However, this effect is rather small [27] since the critical current density decreases exponentially with the barrier thickness. Moreover, the maximum critical current density of Josephson junctions based on Nb/Al,AlO_x/Al/Nb technology is limited by the fabrication process, e.g. high-quality junctions with a critical current density up to 4.5 kA/cm^2 are fabricated at the HYPRES foundry [28] and the RSFQ design rules of the process at the Jena foundry are currently based on critical current densities limited to 1.0 kA/cm^2 [29]. Consequently, the minimum area and thus the capacitance of a junction with a certain critical current are not only limited by, e.g., photolithography, but also by the maximum usable critical current density. Furthermore, for small-area junctions the contributions of parasitic capacitances become more important and may be even larger than the intrinsic junction capacitance between the two electrodes.

As was discussed in section 5.5.3, the amplitude of the voltage pulses generated by the Smart DROS can be increased by decreasing the junction capacitance. This is advantageous for the development of a Smart DROS with a digital readout scheme. Another important advantage of reducing the capacitance of the hysteretic junctions of a Smart DROS is that the relaxation oscillation frequency f_{RO} can be increased. To understand this mechanism, the theory of operation of the DROS presented in section 5.1.1 has to be extended.

The flux noise of a DROS is estimated by Eq. (5.5). One could conclude that the relaxation oscillation frequency could be increased infinitely to enhance the sensitivity. However, this equation is only valid when the relaxation oscillation frequency is smaller than ~1 % of the plasma frequency of the Josephson junctions,

$$f_p = \sqrt{\frac{I_0}{2\pi\Phi_0 C_j}} \,. \tag{6.4}$$

When the relaxation oscillation frequency exceeds ~1 % of the plasma frequency, the interference between the plasma oscillations and the relaxation oscillations causes unpredictable transitions between the voltage state and the superconducting state and starts to limit the sensitivity of the DROS [30,31,32,33]. From Eq. (6.4), it can be concluded that to increase the plasma frequency, and thus the maximum relaxation oscillation frequency, the junction capacitance should be decreased and thus the critical current density should be increased.

Figure 6.2 shows the energy resolution of a DROS as a function of the relaxation oscillation frequency. The full line was calculated for a DROS with a signal SQUID inductance of $L_{sq,sig} = 250$ pH and a screening parameter of $\beta_{L,sig} = 1$.

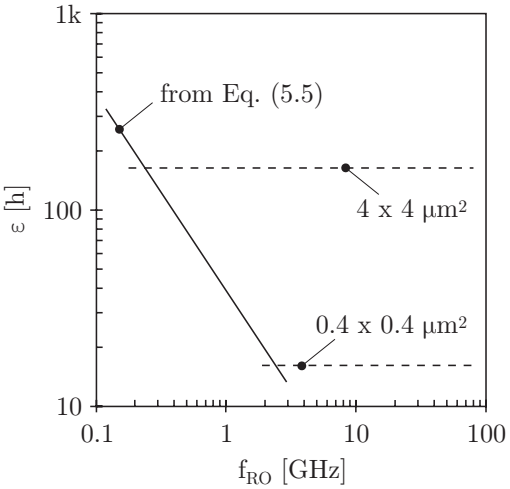

Fig. 6.2 Energy resolution of a DROS as a function of the relaxation oscillation frequency. The dotted lines, representing the minimum energy resolution, cross the full line at f_{RO} equal to 1 % of the plasma frequency. The signal SQUID parameters are: $L_{sq,sig}$ = 250 pH and $\beta_{L,sig} = 1$. The specific capacitance was assumed to be 0.03 pF/μm^2 and T = 4.2 K.

The dotted lines represent the minimum energy resolution that can be achieved by using 4 x 4 μm^2 junctions, f_p = 25 GHz, and 0.4 x 0.4 μm^2 junctions, f_p = 250 GHz. From this figure, the importance of decreasing the junction area becomes clear if we want to increase the relaxation oscillation frequency of the Smart DROS.

As was discussed in section 5.2.2, the quantization unit of the feedback flux of a Smart DROS should ideally be equal to the broadband flux noise of the DROS. As can be concluded from Eqs. (5.5) and (5.21), this means that the optimum value of the quantization unit is independent on the relaxation oscillation frequency [19],

$$\delta\Phi_{fb} = \frac{1}{2g}\frac{(1+\beta_{L,sig})}{I_0^{2/3}}\Phi_0\,, \tag{6.5}$$

with $g \approx 7{\cdot}10^4$ A$^{-2/3}$. For the optimized Smart DROS that was discussed in chapter 5, the optimum quantization unit of the feedback flux was ~50 mΦ_0. Together with a relaxation oscillation frequency of 100 MHz, this resulted in a maximum flux slew rate of $\partial\Phi_{sig}/\partial t = \delta\Phi_{fb} f_{RO} \approx 5{\cdot}10^6$ Φ_0/s. Thus if we could increase the relaxation oscillation frequency of the Smart DROS to 2 GHz, without changing the signal SQUID inductance $L_{sq,sig}$ and the critical current of the junctions I_0, the maximum flux slew rate could in principle be increased to 10^8 Φ_0/s.

In order to show the feasibility of the Smart DROS concept using small-area junctions, a Smart DROS based on a relaxation oscillation frequency of 5 GHz was designed and implemented in JSIM [34]. This design is similar to the design of the 100 MHz optimized Smart DROS described in the previous chapter. Since the parameter extraction and the simulation model of a Smart DROS were discussed thoroughly in section 5.3, the results of the 5 GHz Smart DROS are presented only briefly in this section.

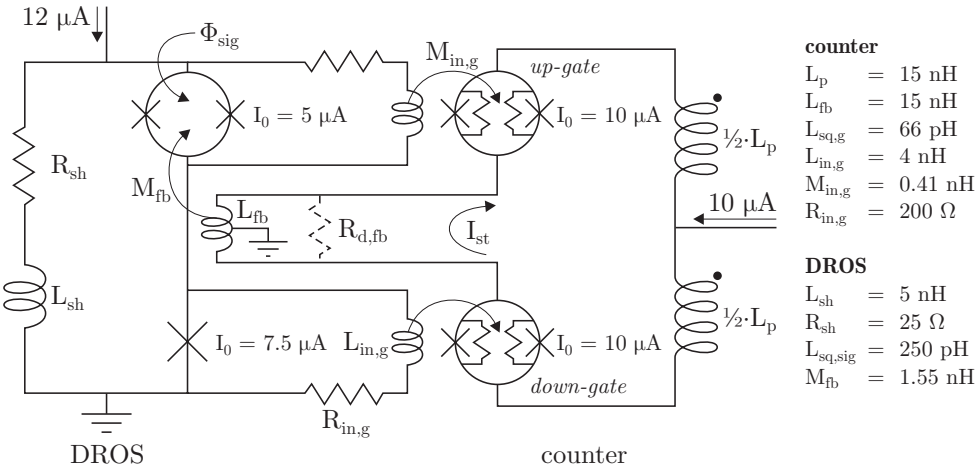

Fig. 6.3 Simulation scheme used to investigate the dynamic behavior of an optimized Smart DROS with a relaxation oscillation frequency of $f_{RO} = 5$ GHz and a quantization unit of the feedback flux of $\delta\Phi_{fb} = 52\ m\Phi_0$. The resulting maximum flux slew rate is $2.6{\cdot}10^8\ \Phi_0/s$.

The simulation scheme is shown in Fig. 6.3. The most important difference between the 100 MHz Smart DROS and the 5 GHz Smart DROS is that the latter is based on a signal SQUID with 0.4 x 0.4 μm^2 junctions whereas 4 x 4 μm^2 junctions were used in the 100 MHz Smart DROS. Assuming that the specific capacitance is $C/A = 0.03\ pF/\mu m^2$, the junction capacitance is $C_j = 5$ fF. The critical current of one junction is $I_0 = 5\ \mu A$ and the corresponding plasma frequency is $f_p = 280$ GHz. The R-L shunt of the DROS consists of a resistor $R_{sh} = 25\ \Omega$ and an inductor $L_{sh} = 5$ nH. The time constant $L_{sh}/R_{sh} = 0.2$ ns implies a relaxation oscillation frequency of about 5 GHz. The Josephson counter was designed such that the quantization unit of the feedback flux was $\delta\Phi_{fb} = 52\ m\Phi_0$, equal to the quantization unit of the feedback flux of the 100 MHz Smart DROS. The maximum flux slew rate of the 5 GHz Smart DROS is thus $\partial\Phi_{sig}/\partial t \approx 2.6{\cdot}10^8\ \Phi_0/s$.

Figure 6.4a shows the result of a numerical simulation of the Smart DROS in operation. The signal flux, represented by the dotted line, is applied to the signal SQUID of the DROS and is varied in time. At $t = 0$, the system is in its dynamic equilibrium and the signal SQUID and the reference junction oscillate in turn. When the signal flux is changed with a slew rate close to the maximum slew rate of the Smart DROS, the system is forced out of its equilibrium and either the signal SQUID or the reference junction generates voltage pulses until the equilibrium is restored. This simulation clearly shows the proper operation of the Smart DROS.

Figure 6.4b shows the effect of a two times larger junction capacitance: In this case, the specific capacitance was increased to $C/A = 0.06\ pF/\mu m^2$. All other parameters were the same as above. One of the consequences of the larger capacitance is that the parasitic resonances between the shunt inductance and the SQUID capacitance are less effectively damped, i.e. the damping parameter D becomes twice as small [from Eq. (5.6)]. As can be concluded from the simulation, the maximum flux slew rate reduces somewhat and the 5 GHz Smart DROS cannot track the applied signal flux properly.

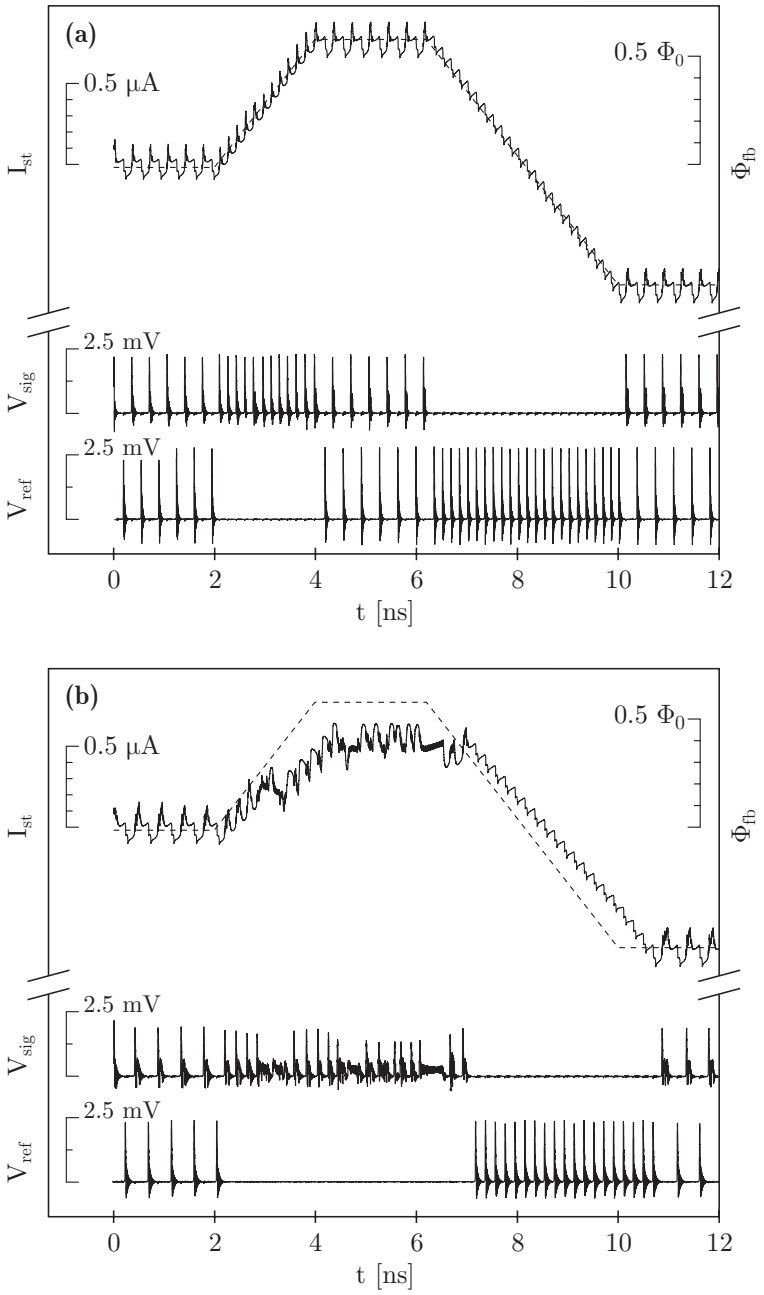

Fig. 6.4 (a) Numerical simulation of the response of the optimized 5 GHz Smart DROS to variations in input flux. The flux is directly applied to the signal SQUID of the DROS and is represented by the dotted line. V_{sig} is the voltage across the signal SQUID of the DROS and V_{ref} is the voltage across the reference junction. **(b)** As **(a)** except for the fact that in this case the capacitances of the junctions of the DROS were twice as large.

6.2 Ramp-type Josephson junctions based on Nb/Al technology

In the previous section, it was discussed that the flux noise of both the two-stage SQUID system and the Smart DROS can be improved by using small-area Josephson junctions. Moreover, it was shown that for a Smart DROS in principle flux slew rates up to 10^8 Φ_0/s can be achieved using junction areas of the order of 0.2 μm^2. In order to reduce the junction area, ramp-type junctions based on standard Nb/Al,AlO_x/Al/Nb technology were studied. The results are presented in this section.

6.2.1 Fabrication of the ramp-type Nb/Al,AlO_x/Al/Nb junctions

Around the year 1980, several groups started the research on low-T_c ramp-type junctions based on, e.g., Pb/Sn [35], PbIn/Pb [36], Nb/Pb [37] using native-oxide barriers and later also all-refractory, e.g., NbN/MgO/NbN [38] ramp-type junctions were studied. Now, for more than two decades ramp-type junctions have been made using a wide variety of materials. The standard low-T_c fabrication process at the Low Temperature Division at the University of Twente, see section 5.4.3, is based on planar Nb/Al,AlO_x/Al/Nb Josephson junctions, which limits the minimum achievable junction area. However, using a ramp-type configuration, see Fig. 6.5, small-area Josephson junctions can be fabricated without requiring high-resolution photolithography.

In planar junctions, the Nb/Al,AlO_x/Al/Nb layer is produced in-situ, whereas ramp-type junctions require multiple vacuum depositions. Consequently, the ramp that has to be etched in the Nb bottom layer is exposed to air and the superconducting characteristics are often deteriorated [39]. Moreover, the Nb ramp has a rougher surface than the Nb bottom electrode of planar junctions. However, the possibility to achieve sub-μm^2 junction areas using micrometer resolution photolithography is an important advantage of the ramp-type configuration. For example, assume that the minimum feature size that can be achieved is 2 μm. The ramp-type junction area is determined by the thickness of the bottom Nb layer and the width of the counter electrode at the ramp. For a bottom layer with a thickness of 150 nm and a width of the counter electrode at a 45° ramp of 2 μm, the resulting junction area is $\sqrt{2}$ x 0.15 μm x 2 μm = 0.4 μm^2. For planar junctions, the minimum junction area would be 4 μm^2, which is one order of magnitude larger.

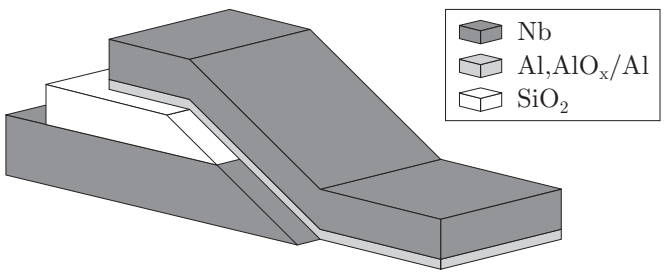

Fig. 6.5 Schematic overview of a low-T_c ramp-type Josephson junction based on standard Nb/Al,AlO_x/Al/Nb technology. The finger of the counter electrode overlaps the SiO_2 layer.

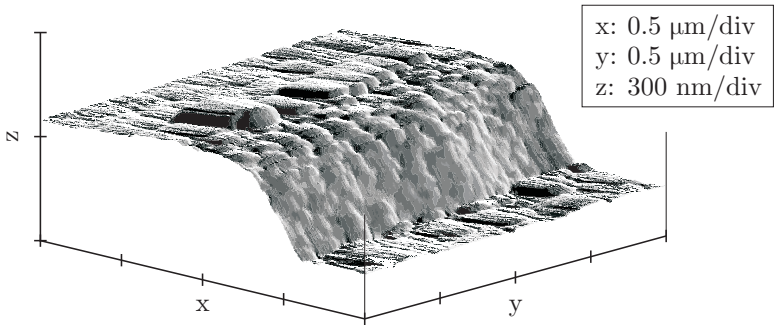

Fig. 6.6 Typical AFM micrograph of a ramp defined in a bilayer of 150 nm Nb and 100 nm SiO_2. The slope of the Nb bottom layer is about 45°.

In the fabrication process of Nb/Al,AlO_x/Al/Nb ramp-type junctions, first a bilayer of 150 nm Nb and 100 or 200 nm SiO_2 is sputtered, see also section 5.4.3. In the next step, a ramp is defined in this bilayer. The ramp can be defined in several ways, e.g. using resist reflowing and reactive ion etching (RIE) [40,41], wet etching of the top SiO_2 layer together with RIE [42,43] or argon ion beam milling [39]. We have used standard photolithography and argon ion beam milling to define the ramps. The argon ion beam voltage is 500 V and the milling is performed in a pulsed mode, i.e. 8 s on and 12 s off. For these settings, the etch rate of the bilayer is about 8 nm/min. The photoresist mask is also etched, such that for a 150 nm Nb and 100 nm SiO_2 bilayer an etch angle of 60° resulted in a slope of the ramp of about 45° [44]. After argon ion beam milling, the photoresist mask is removed. Figure 6.6 shows a typical atomic force microscope (AFM) micrograph of a ramp in an Nb/SiO_2 bilayer. The typical columnar structure of Nb is clearly visible. The 'hill' on top of the bilayer in the center of the AFM micrograph is caused by redeposition of etched material in the 'shadow' of the photoresist mask.

After defining the ramp in the Nb/SiO_2 bilayer, a second photoresist mask is used for patterning the SiO_2 layer. In this step, contact holes to the Nb bottom electrode are etched in the SiO_2 layer using a buffered oxide etcher (BOE) of 87.5 % HF and 12.5 % NHF_3. An etching time of 3½ minutes is required. The ramp is then cleaned in an Ar plasma. The Ar pressure is $P_g = 1.3 \cdot 10^{-2}$ mbar, the cleaning power is $P = 60$ W and the target voltage is $V = 300$ V. This cleaning step is required to remove the NbO_x layer formed on the Nb ramp that is exposed to air.

In the next step, the barrier layer and the counter electrode are deposited. The barrier layer and the counter electrode are fabricated by subsequently dc magnetron sputtering of a 10 nm Al layer, which is oxidized at room temperature for one hour at an O_2 pressure of 0.12 mbar to form the actual barrier layer, a second 10 nm Al layer and a 350 nm thick Nb counter electrode. Finally, a 5 nm protective Al layer is deposited on top of the counter electrode. The critical current density is designed to be 1 kA/cm^2. The first 10 nm Al layer reduces the roughness of the bottom electrode and the second 10 nm Al layer is used to prevent the reaction of the Nb counter electrode with the AlO_x barrier layer. The Al,AlO_x/Al layer and the Nb counter electrode are patterned, a 'finger' pattern, by photolithography together with either the lift-off technique or RIE and wet etching.

Based on the process described above, three series of ramp-type junctions were fabricated. For all three series, the slope of the ramp was about 45° and the width w of the finger of the counter electrode at the ramp was varied. The width of the finger was 1, 2, 4, 8, 16 and 32 μm. The designed smallest junction area is therefore $\sqrt{2}$ x 0.15 μm x 1 μm = 0.2 μm^2. Also the overlap of the finger at the Nb/SiO_2 bilayer was varied: 1, 2, 3 and 4 μm.

For series A and B of the Nb/Al,AlO_x/Al/Nb ramp-type junctions, the barrier layer and the counter electrode were patterned using the lift-off technique. This means that after fabrication of a ramped 150 nm Nb and 100 nm SiO_2 bilayer and the SiO_2 etching, a photoresist mask was applied and then the ramp was cleaned and the Al and the Nb layers were deposited. Finally, the remaining photoresist together with the material on top of it was removed in acetone. For series A, the ramp was cleaned for 10 minutes and for series B it was cleaned for 30 minutes. During the cleaning process of the ramp in an Ar plasma, Nb at the ramp and SiO_2 is partly removed. Consequently, the barrier layer is buried in the bottom electrode.

For series C, the counter electrode was patterned using RIE to prevent that the barrier layer is buried in the bottom electrode. First a ramped bilayer of 150 nm Nb and 200 nm SiO_2 was fabricated and the contact holes in the SiO_2 layer were etched. Then the ramp was cleaned for 30 minutes and the Al and the Nb layers were deposited. After deposition, a photoresist mask was applied and the Nb counter electrode was selectively etched in an SF_6 plasma. The underlying Al layer was used as a stopping layer. Finally, the remaining Al,AlO_x/Al was patterned by wet etching in diluted developer.

6.2.2 Experimental characteristics of ramp-type Nb/Al,AlO_x/Al/Nb junctions

In this section, the experimental results of the three series of ramp-type junctions are described one after the other. The junctions were characterized using standard homemade battery powered *I-V* electronics. The chips were electromagnetically shielded by a Nb can and all wires between the chips and the room temperature electronics were low pass filtered. The cryostat was surrounded by a cylindrical μ-metal shield at room temperature.

The *I-V* characteristics of the ramp-type junctions of series A did not show any hysteresis at 4.2 K. A typical *I-V* characteristic of a 32 μm wide ramp-type junction at 4.2 K measured by a Tektronix TDS 410A digital oscilloscope is shown in Fig. 6.7a. The non-hysteretic behavior is caused by the low value of the normal state resistance $R_N = 4\ \Omega$, i.e. much smaller than expected from Eq. (6.3). Because of the small critical current at 4.2 K, $I_0 \approx 3.5$ μA, the magnetic field dependence of the junction [45] could not be measured accurately. When reducing the temperature from 4.2 K to about 1.5 K, the critical current increased by a factor ~10.

For all junctions of series A, the normal state resistance R_N was almost temperature independent. Since the normal state resistance was almost independent on the overlap, its low value cannot be attributed to the overlap. As expected, the normal state conductance $1/R_N$ was linearly dependent on the junction width w and thus the junction area, as is shown in Fig. 6.7b. Based on these measurements however, the origin of the low normal state resistance and the large temperature

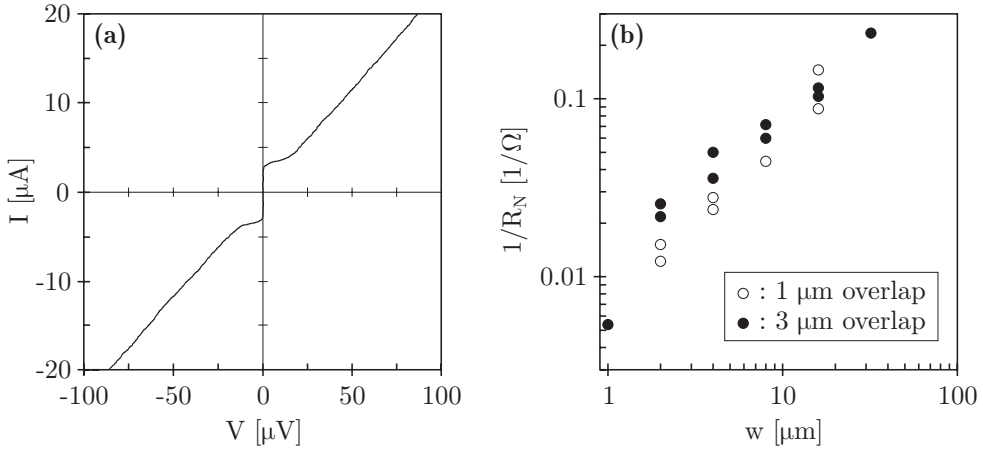

Fig. 6.7 (a) Typical I-V characteristic of a ramp-type junction of series A at 4.2 K. The width of the finger at the ramp was $w = 32$ μm and the overlap was 3 μm. The ramp was cleaned for 10 minutes and lift-off was used for patterning the counter electrode. **(b)** $1/R_N$ as a function of the junction width for an overlap of 1 and 3 μm.

dependence of the critical current cannot be retrieved. Since the I-V characteristics of these ramp-type junctions show similarity to the I-V characteristics of double-barrier junctions [46,47], the results might be attributed to reduced superconducting characteristics of the Nb ramp. This means that due to a too short cleaning time of the ramp, a second barrier of NbO_x might be formed at the ramp. Together with the AlO_x barrier layer, a Nb,NbO_x/Al,AlO_x/Al/Nb double-barrier junction might be formed. However, the low value of the normal state resistance can also be caused by an external parasitic shunt resistance, e.g. resulting from the fact that the counter electrode is buried in the Nb ramp or the Al layer lying under the AlO_x barrier layer [48], see Fig. 6.8. This underlying Al layer can also be the cause of the strong temperature dependence of the critical current as is discussed below.

To investigate the origin of the non-hysteretic behavior of the ramp-type junctions, the cleaning time of the Nb ramp for series B was increased from 10 to 30 minutes in order to remove the possible NbO_x layer at the ramp. These junctions did show hysteresis, but the normal state conductance $1/R_N$ and the critical current

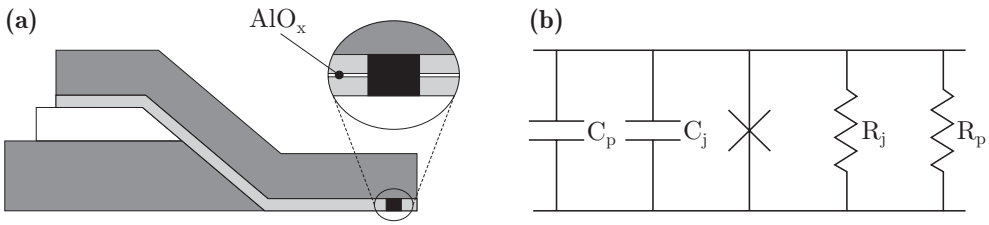

Fig. 6.8 (a) Schematic overview of a ramp-type Nb/Al,AlO_x/Al/Nb junction with a short through the AlO_x barrier layer, represented by the black rectangle. This short causes a low-ohmic parasitic shunt resistance R_p formed by the underlying Al layer. **(b)** Simplified equivalent circuit of the ramp-type junction. C_p represents the parasitic capacitance related to, e.g., the overlap.

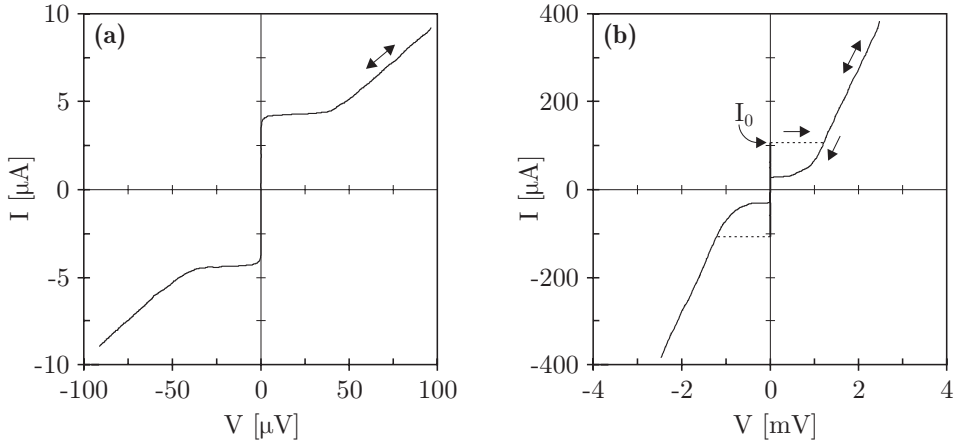

Fig. 6.9 (a) Experimental *I-V* characteristic of a ramp-type junction of series C at 4.2 K. The width of the finger at the ramp was $w = 16$ μm and the overlap was 3 μm. The Nb ramp was cleaned for 30 minutes and the counter electrode was patterned by RIE. **(b)** Hysteretic *I-V* characteristic of the same ramp-type junction measured at 1.5 K.

I_0 scaled linearly with the overlap of the counter electrode. This suggests that the samples were cleaned too long, such that the 100 nm SiO_2 layer was removed and the bottom Nb electrode was not sufficiently insulated from the Al,AlO_x/Al layer at the overlap.

For series C, the thickness of the SiO_2 layer was increased from 100 to 200 nm and the counter electrode was patterned using RIE to prevent that the barrier layer would be buried in the bottom electrode. The ramps were cleaned for 30 minutes. However, the measured *I-V* characteristics of the ramp-type junctions of this series were similar to those measured for series A. Also for this series, the junctions did not show hysteresis at 4.2 K, the normal state resistance was smaller than expected and $1/R_N$ was linearly dependent on the junction width. A typical *I-V* characteristic of a 16 μm wide ramp-type junction measured at 4.2 K is shown in Fig. 6.9a. The critical current of this junction is 4 μA and the normal state resistance, measured in the mV-range, is $R_N = 5\ \Omega$. Cooling the samples down from 4.2 K to about 1.5 K resulted in an increase of the critical current by a factor ~25, see Fig. 6.9b. The normal state resistance was almost temperature independent. At 1.5 K however, the *I-V* characteristics of the ramp-type junctions did show hysteresis because of the larger critical current. All junctions of series C showed a current deficit, i.e. extrapolating the linear *I-V* characteristics at high voltages back to zero voltage, gives a negative current offset. A current deficit is, for example, a typical effect of double-barrier junctions [47] and ultrasmall junctions [49], but in this case the origin of the current deficit remains unclear.

The typical dependence of the reduced critical current $I_0/I_0(0)$ on the applied magnetic field B in the direction perpendicular to the current direction and parallel to the counter electrode is shown in Fig. 6.10. The width of the junction was 32 μm and the overlap was 1 μm. Figure 6.10 closely approximates the Fraunhofer diffraction pattern of a rectangular junction, characterized by first-order side lobes

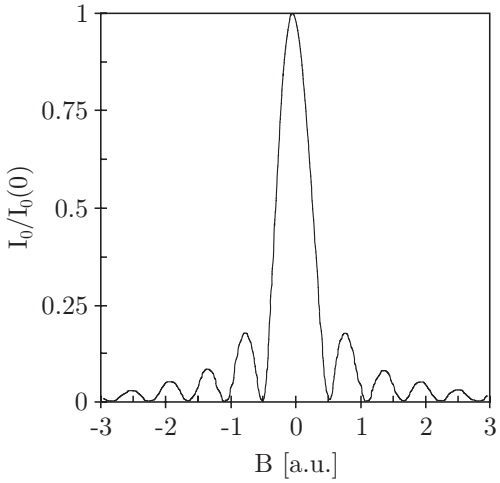

Fig. 6.10 Dependence of the reduced critical current $I_0/I_0(0)$ on the applied magnetic field B of a ramp-type junction at 4.2 K. The width of the finger at the ramp was 32 μm and the overlap was 1 μm.

with an amplitude of 22 % of the central maximum [45]. The measured ratio of 20 % indicates that the local critical current density along the length of the ramp-type junction is fairly uniform.

As was discussed above for the junctions of series A, the low normal state resistance can have several origins. A NbO_x layer on top of the Nb ramp leads to reduced superconducting characteristics and might cause double-barrier-like non-hysteretic *I-V* characteristics. In order to investigate the superconducting characteristics of the Nb ramp, reference samples were made using the same fabrication process as described in section 6.2.1, except for the deposition of the Al,AlO_x/Al layer. For these reference samples, the ramps were cleaned for 5 minutes in an Ar plasma. At 4.2 K, critical currents up to 40 mA were obtained for 2 μm wide contacts, corresponding to a critical current density of 10^7 A/cm^2. This means that the Nb ramp surface has good superconducting characteristics and that a double-barrier structure is not likely to be the origin of the low normal state resistance.

Since the ramp-type junctions of both series A and C showed non-hysteretic behavior at 4.2 K, the fact that the counter electrode is buried in the Nb ramp for series A cannot be the only origin of the low normal state resistance. Most likely, the low value is caused by a parasitic shunt resistance formed by the Al layer lying under the AlO_x barrier layer. When the AlO_x layer is completely closed, i.e. there are no shorts through this layer, the underlying normal conducting Al layer cannot cause a parasitic shunt resistance. However, shorts through the AlO_x layer[ii], e.g. under the lead part of the counter electrode, imply a parasitic resistance R_p in parallel with the actual junction, as is shown in Fig. 6.8. For the 16 μm wide ramp-

[ii] Since the AlO_x layer is very thin and the area of the Al,AlO_x/Al layer under the counter electrode is very large, the probability of shorts through the insulating AlO_x layer is high.

type junction shown in Fig. 6.9, the normal state resistance is $R_N = 5\ \Omega$. For 25 nm thick Al films, the specific resistance at 4.2 K was measured to be $\rho \approx 3{\cdot}10^{-8}\ \Omega$m. The finger of the counter electrode has a length of $l = 15\ \mu$m on the substrate and the width is $w = 16\ \mu$m. Thus, for a 10 nm thick Al film, the resistance of the finger would be ~3 Ω, which is close to the measured normal state resistance. This suggests that shorts in the AlO_x layer under the lead part of the counter electrode close to the finger can be the origin of the low normal state resistance. This model agrees with the fact that $1/R_N$ scaled linearly with the width of the finger.

The underlying Al layer is most probably also the origin of the strong temperature dependence of the critical current. Because of the proximity effect, the underlying Al layer is made weakly superconducting at the area where it is in close contact with the Nb bottom layer. As a result, the effective junction area at 4.2 K is enlarged by a factor of ~2 for our design of the ramp-type junction [50]. The proximity effect is temperature dependent. Consequently, the effective area of the ramp-type junction increases for decreasing temperatures until the critical temperature of Al, $T_c \approx 1.2$ K, is reached and the underlying Al layer becomes completely superconducting.

6.2.3 Experimental characteristics of ramp-type Nb/Al,AlO$_x$/Al/Nb dc SQUIDs

On the same wafer as the ramp-type junctions of series C, dc SQUIDs based on these ramp-type junctions were fabricated. The SQUID inductance was designed to be $L_{sq} = 150$ pH and a ½-turn coil was deposited at the outside of the washer to apply flux. No shunt resistors or damping resistors are used in the design of the SQUIDs. Figure 6.11 shows two micrographs of a dc SQUID based on ramp-type junctions with a width of 3 μm and an overlap of 4 μm.

Figure 6.12a shows the experimental *I-V* characteristics of a dc SQUID based on 0.2 x 2 μm^2 ramp-type junctions and Fig. 6.12b shows the *I-V* characteristics of a SQUID based on 0.2 x 12 μm^2 junctions. In both cases, the flux was swept via the ½-turn coils. The corresponding V-Φ_{sig} characteristics of the dc SQUID based on 0.2 x 12 μm^2 junctions for different values of the bias current are shown in Fig.

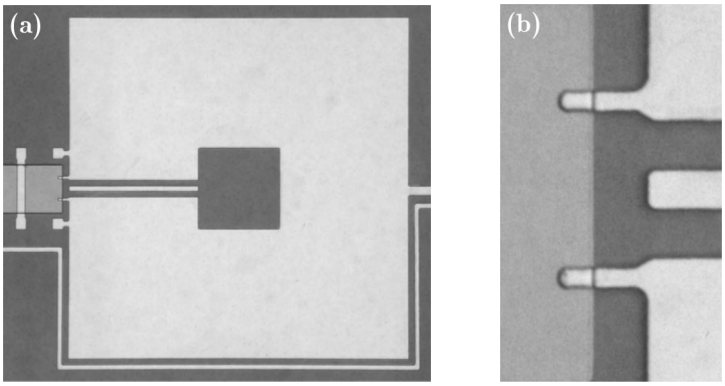

Fig. 6.11 (a) Micrograph of a dc SQUID based on ramp-type Nb/Al,AlO_x/Al/Nb junctions. **(b)** Micrograph zoomed in on the ramp-type junctions of the same SQUID. The junction width is 3 μm and the length of the overlap of the counter electrode is 4 μm.

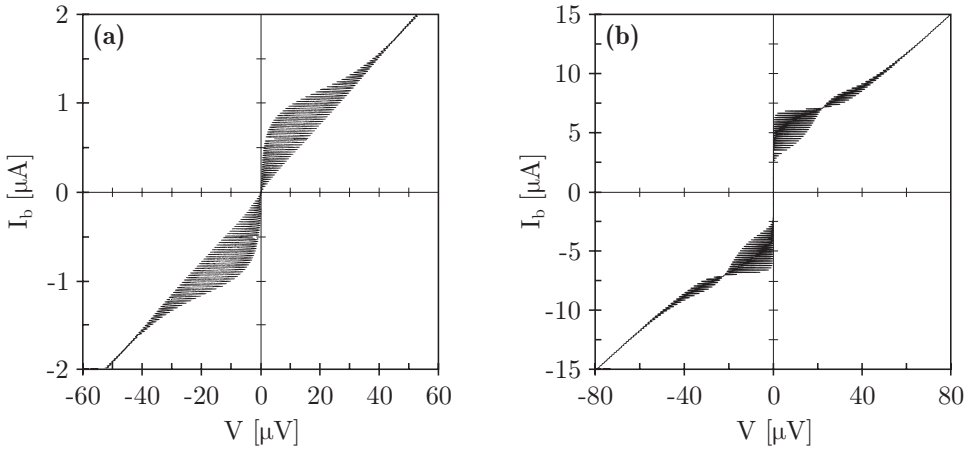

Fig. 6.12 (a) Experimental *I-V* characteristics of a dc SQUID based on ramp-type junctions with a width of 2 μm and an overlap of 3 μm. **(b)** *I-V* characteristics of a dc SQUID based on ramp-type junctions with a width of 12 μm and an overlap of 2 μm. The measurements were performed at 4.2 K. In both cases, the flux was swept via the ½-turn coil.

6.13a. The positions of the minimum and maximum voltages are interchanged from trace (a) to trace (b) and (c), which is caused by resonances between the SQUID inductance and the capacitances of the Josephson junctions. In the *I-V* characteristics of symmetric dc SQUIDs, a resonant step appears at the voltage [51]

$$V_r = \frac{\Phi_0}{2\pi} \frac{1}{\sqrt{L_{sq}\, C_j/2}}\,. \tag{6.6}$$

This resonant step can be so large that the $n\Phi_0$ and the $(n + ½)\Phi_0$ branches of the *I-V* characteristics cross, as is shown in Fig. 6.12b. Assuming that the resonant voltage V_r coincides with the voltage at which both branches of the *I-V*

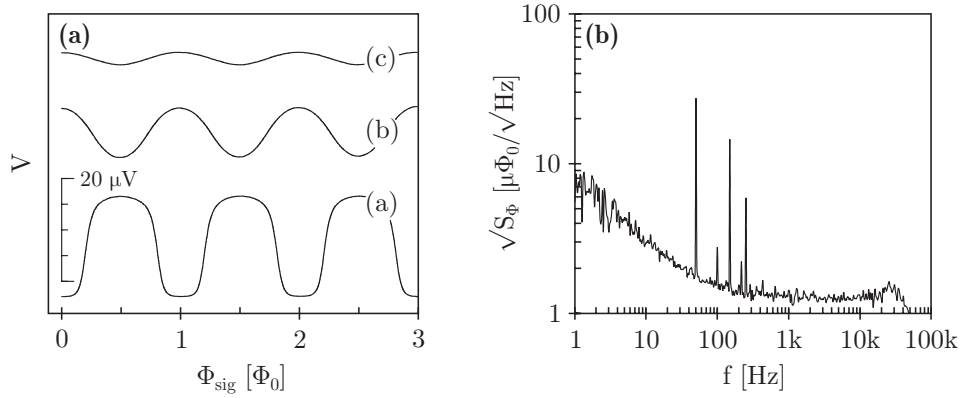

Fig. 6.13 (a) Experimental voltage vs. flux (V-Φ_{sig}) characteristics of a dc SQUID based on ramp-type junctions with a width of $w = 12$ μm at different bias currents. For trace (a), the bias current was $I_b = 6$ μA, for trace (b) 8 μA and for trace (c) 10 μA. The vertical offsets are arbitrary. **(b)** Flux noise spectrum of the same dc SQUID measured at 4.2 K.

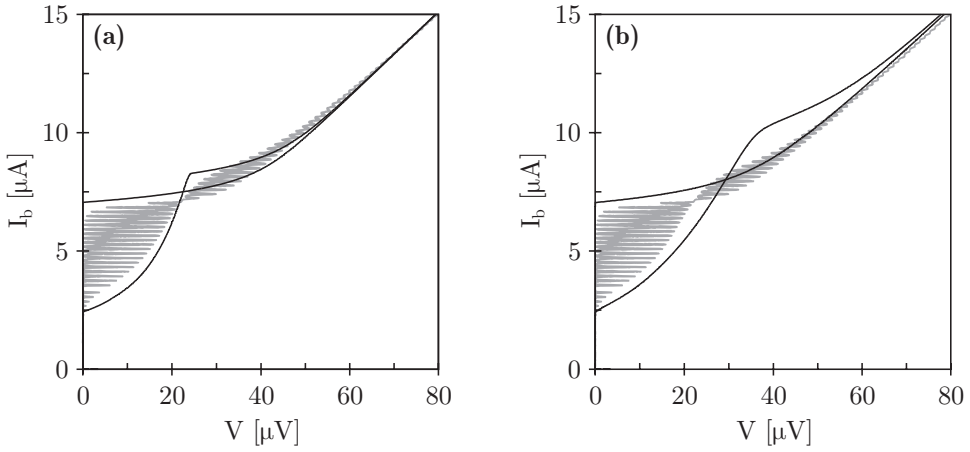

Fig. 6.14 Experimental *I-V* characteristics of a dc SQUID based on ramp-type junctions with a width of $w = 12$ μm, gray lines, see also Fig. 6.12b. The black lines are the simulated $n\Phi_0$ and $(n + ½)\Phi_0$ branches of the *I-V* characteristics. The parameters of the simulated SQUID were: $L_{sq} = 150$ pH, $2I_0 = 7$ μA and $R = 11$ Ω. The junction capacitance was **(a)** $C_j = 2.3$ pF and **(b)** $C_j = 1.0$ pF.

characteristics cross, i.e. $V_r \approx 22$ μV, the capacitance of the junction including parasitic capacitance, e.g. related to the overlap, can be calculated as $C_j = 2.9$ pF. Thus for a junction area of 0.2 μm x 12 μm = 2.4 μm^2, the specific capacitance can be estimated as $C/A \approx 1.2$ pF/μm^2. This is much larger than the value reported in, e.g., ref. [27] for critical current densities of $J_c \approx 1$ kA/cm^2: $C/A = 0.05$ pF/μm^2. As was discussed, the effective junction area is enlarged by the proximity effect. However, this effect is expected to increase the area by only a factor of ~2, which suggests that the parasitic capacitance is much larger than the capacitance between the two electrodes. The relative dielectric constant of SiO_2 is $\varepsilon_r = 3.7$. Thus, assuming that the remaining SiO_2 insulating layer has a thickness of $h = 130$ nm[iii], the overlapping area of $A = 2$ μm x 12 μm = 24 μm^2 causes a parasitic capacitance of only $C_p = \varepsilon_0\varepsilon_r A/h = 6.0$ fF. Therefore, the large junction capacitance cannot be attributed to the overlap. This suggests that the large parasitic capacitance is most probably caused by the capacitance between the Nb counter electrode and the underlying Al layer, as is discussed in detail in the appendix.

Generally the peak voltage of the resonant step does not agree with the resonant voltage V_r [51]. For this reason, the *L-C* resonances of the SQUID based on the 0.2 x 12 μm^2 ramp-type junctions were simulated using JSIM [34] and using the simple model shown in Fig. 6.8. The simulated $n\Phi_0$ and the $(n + ½)\Phi_0$ branches of the *I-V* characteristics are shown in Fig. 6.14. In the simulation, the SQUID inductance was $L_{sq} = 150$ pH and the Josephson junctions had a critical current of $I_0 = 3.5$ μA each. Each junction was shunted with a resistor of $R = 11$ Ω. For a junction capacitance of $C_j = 2.3$ pF, the $n\Phi_0$ and the $(n + ½)\Phi_0$ branches of both

[iii] First a bilayer of 150 nm Nb and 200 nm SiO_2 was fabricated. During cleaning of the Nb ramp, about 70 nm of SiO_2 is removed, such that about 130 nm SiO_2 remains.

the measured and the simulated I-V characteristics cross at a voltage of $V \approx 22$ μV, as is shown in Fig. 6.14a. This value of the junction capacitance is somewhat smaller than the value that was calculated from Eq. (6.6). The effect of a smaller junction capacitance is clearly visible in Fig. 6.14b. In this case, the junction capacitance was decreased to $C_j = 1.0$ pF. All other SQUID parameters were the same as above. As expected, the voltage at which a resonant step appears, is increased.

The flux noise spectrum of the dc SQUID based on 0.2 x 12 μm^2 junctions is shown in Fig. 6.13b. This measurement was performed in a two-stage setup, using a DROS as a low-noise cryogenic preamplifier for the ramp-type dc SQUID, as was discussed in chapter 4. In this way, the intrinsic flux noise of the SQUID could be measured. Moreover, by biasing the SQUID at a constant voltage instead of biasing it with a constant current, the adverse effect of resonances around V_r on the SQUID characteristics could be prevented. At a bias voltage of $V_{bias} \approx 10$ μV, the measured white noise level was $\sqrt{S_\Phi} = 1.2$ μ$\Phi_0/\sqrt{\text{Hz}}$, which agrees with the theoretically calculated value of 1.0 μ$\Phi_0/\sqrt{\text{Hz}}$ [from Eq. (2.18)]. The 1/f corner frequency is about 50 Hz and at 1 Hz the flux noise is $\sqrt{S_\Phi} \approx 8$ μ$\Phi_0/\sqrt{\text{Hz}}$.

6.3 Conclusion and discussion

In the first section of this chapter, it was discussed that reducing the capacitance and thus the area of the Josephson junctions of the two-stage SQUID system and the Smart DROS leads to improved performance of these SQUID systems. It was shown that the white noise level of two-stage SQUID systems can be reduced by using small-area junctions. For a Smart DROS, the maximum relaxation oscillation frequency is limited to about 1 % of the plasma frequency of the Josephson junctions. By decreasing the junction area, the plasma frequency is increased. Consequently, the maximum relaxation oscillation frequency and thus the maximum flux slew rate can be increased. Moreover, the white noise level of the Smart DROS is reduced. Numerical simulations showed that using junction areas of the order of 0.2 μm^2, flux slew rates up to 10^8 Φ_0/s are possible for the Smart DROS.

In order to reduce the junction area, ramp-type junctions based on standard Nb/Al,AlO_x/Al/Nb technology were studied. An important advantage of the ramp-type configuration is that sub-μm^2 junction areas can be achieved using micrometer resolution photolithography. The ramp-type junctions were fabricated by first depositing a Nb/SiO_2 bilayer, then a ramp is defined in this bilayer by argon ion beam milling and finally the barrier layer and the counter electrode are deposited. Martinis *et al.* [49] and Mizutani *et al.* [18,48] reported on similar fabrication processes of Nb/Al,AlO_x/Al/Nb ramp-type junctions. They omitted the SiO_2 insulating layer by using misalignment schemes, such that only some of the fingers of the counter electrode just contact the Nb bottom electrode at the ramp. In this way, only occasionally true ramp-type junctions are formed. However, this technique showed that in principle ramp-type junctions with very small capacitances can be fabricated. Martinis *et al.* reported junction capacitances as small as $C_j = 0.18$ fF.

An important disadvantage of the ramp-type configuration is that the Al layer lying under the AlO_x barrier layer can cause a low-ohmic shunt resistance in parallel with the junction [48]. As a result of this low-ohmic shunt resistance, the ramp-type junctions that were fabricated did not show hysteresis at 4.2 K. Furthermore, the critical currents of the junctions showed large temperature dependence. The origin of this large temperature dependence can also be found in the underlying Al layer. At the ramp, this Al layer is in close contact with the Nb bottom layer and is therefore made weakly superconducting by the proximity effect. This effect is temperature dependent such that the effective junction area and thus the critical current are also temperature dependent. Moreover, the proximity effect limits the minimum junction area that can be achieved for ramp-type junctions.

First dc SQUIDs based on Nb/Al,AlO_x/Al/Nb ramp-type junctions have been fabricated and experimentally characterized. In these SQUIDs, the non-hysteretic behavior of the ramp-type junctions was exploited and neither shunt resistors nor damping resistors were used in the design. As a result, the *L-C* resonances between the SQUID inductance and the junction capacitances were not effectively damped and the *I-V* characteristics showed large resonant steps. From these resonances, the capacitance per junction area was calculated to be $C \approx 1$ pF/μm^2, which is much larger than expected. This suggests that parasitic capacitances play an important role in the overall junction capacitance. The large parasitic capacitance might be attributed to the capacitance between the Nb counter electrode and the underlying Al layer, as is discussed in the appendix. Although the fabricated SQUIDs were not optimized, the low white noise level of $\sqrt{S_\Phi} = 1.2\ \mu\Phi_0/\sqrt{\text{Hz}}$ for a dc SQUID based on 0.2 x 12 μm^2 ramp-type junctions is promising.

In order to fabricate Nb/Al,AlO_x/Al/Nb ramp-type junctions of real practical value, further research is necessary. In this chapter, only the first steps towards high-quality sub-μm^2 junctions were described. The adverse effects of the underlying Al layer have to be solved. The large temperature dependence of the critical current, the non-hysteretic behavior and the large (parasitic) junction capacitance can be explained as effects of this layer. Reducing the thickness of the Al layers will reduce these effects. In the ramp-type junction process described in this chapter, the thickness of these layers was 10 nm, whereas in the standard fabrication process of planar Nb/Al,AlO_x/Al/Nb Josephson junctions, the thickness of these layers is 5 nm. However, the underlying Al layer must be sufficiently thick to cover the rough Nb surface. On the other hand, thicker layers will not smooth the ramp surface [39]. Another possibility to get rid of the adverse effects of the underlying Al layer would be to disconnect this layer close to the ramp, e.g. by using a patterned SiO_2 layer, a 'hill' or 'valley' pattern, under the Al,AlO_x/Al layer and the Nb counter electrode.

A second point that requires further research is the (parasitic) capacitance of the ramp-type junction. As was discussed in this chapter, the proximity effect, the overlap and the underlying Al layer increase the (intrinsic) junction capacitance. In section 6.2.3, it was shown that *L-C* resonances in SQUIDs could be a useful tool to investigate the junction capacitance. SQUID designs of varying SQUID inductances and ramp-type junctions could be used to systematically study the (parasitic) capacitances of Nb/Al,AlO_x/Al/Nb ramp-type junctions in the future.

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Appendix

Extended model for ramp-type junctions

In section 6.2.2, a simple model of a ramp-type Josephson junction was described. The ramp-type junction was modeled by an ideal Josephson element shunted with a linear (quasiparticle) resistance R_j, an intrinsic junction capacitance C_j, a parasitic resistance R_p and a parasitic capacitance $C_{p,}$ see Fig 6.8. However, this model oversimplifies reality. In this appendix, the model of the Nb/Al,AlO_x/Al/Nb ramp-type junctions described in chapter 6 is extended and the experimental results on the SQUIDs based on ramp-type junctions are compared to numerical simulations that were carried out using JSIM.

The extended model of the Nb/Al,AlO_x/Al/Nb ramp-type junctions is shown in Fig. A.1. The actual junction is represented by an ideal Josephson element in parallel with a quasiparticle resistance R_j. The intrinsic junction capacitance C_j between the electrodes is increased by the proximity effect as was discussed in chapter 6. This effect depends on the temperature and on the thickness of the underlying Al layer. For the fabricated ramp-type junctions that were discussed in chapter 6, the proximity effect increases the effective junction area at 4.2 K by a factor ~2. The two main differences between the simple and the extended model are the way in which the effect of a defect, a pinhole, in the AlO_x layer is modeled and

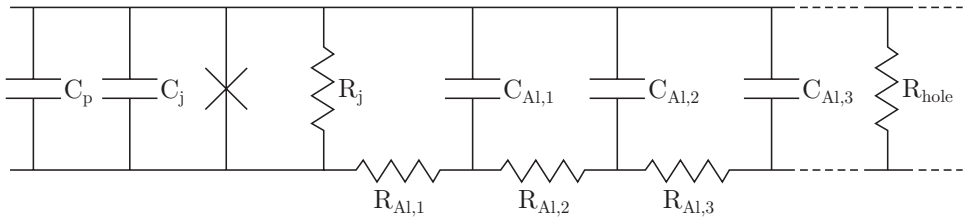

Fig. A.1 Extended model of the Nb/Al,AlO_x/Al/Nb ramp-type junction. C_p represents the parasitic capacitance related to the overlap of the finger of the counter electrode at the Nb/SiO_2 bilayer, C_j is the intrinsic junction capacitance between the electrodes, R_j is the quasiparticle resistance of the junction and $C_{Al,i}$ is the capacitance between the underlying Al layer and the Nb counter electrode. $R_{Al,i}$ corresponds to the resistance of the underlying Al layer and R_{hole} represents the resistance of a defect, e.g. a pinhole, in the AlO_x barrier layer.

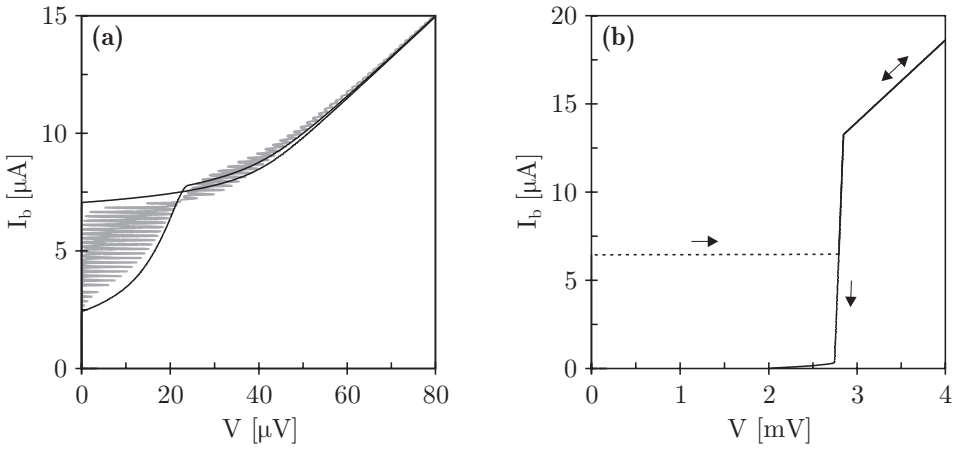

Fig. A.2 (a) Experimental *I-V* characteristics of a dc SQUID based on Nb/Al,AlO_x/Al/Nb ramp-type junctions with a width of 12 μm and an overlap of 2 μm at 4.2 K, gray lines. The black lines are the simulated $n\Phi_0$ and $(n + ½)\Phi_0$ branches of the *I-V* characteristics using the extended model. In the simulation, the presence of two pinholes in the AlO_x layer with a resistance of $R_{hole} = 10$ μΩ and at a distance of 10 μm from each ramp-type junction was assumed. **(b)** Simulated $n\Phi_0$ branch of the *I-V* characteristics of a dc SQUID with the same parameters as in **(a)**, but now without pinholes in the AlO_x layer.

the way in which the capacitance between the underlying Al layer and the Nb counter electrode, i.e. the capacitance between both Al layers of the Al,AlO_x/Al trilayer, is taken into account. In the extended model, the underlying Al layer is modeled by an array of distributed resistances, $R_{Al,i}$, and capacitances, $C_{Al,i}$. The resistance R_{hole} represents a defect in the AlO_x layer, see Fig. A.1.

In section 6.2.3, it was shown that the experimental *I-V* characteristics of a dc SQUID based on Nb/Al,AlO_x/Al/Nb ramp-type junctions could be simulated by using the simple model of the ramp-type junctions. The resonances were explained by assuming a large parasitic capacitance in parallel with the junction, caused by the capacitance between the underlying Al layer and the Nb counter electrode. The origin of the large parasitic capacitance can be explained by the extended model.

Figure A.2a shows the experimental and the simulated *I-V* characteristics of a dc SQUID based on ramp-type junctions with a width of $w = 12$ μm and an overlap of the finger of the counter electrode at the Nb/SiO_2 bilayer of 2 μm. In the simulation, the SQUID inductance was $L_{sq} = 150$ pH and the Josephson junctions had a critical current of $I_0 = 3.5$ μA. The specific capacitance of the junction, and thus of the Al,AlO_x/Al layer, was assumed to be[i] $C/A = 0.037$ pF/μm^2. Taking the proximity effect into account, the intrinsic junction capacitance between the electrodes was $C_j = 2$ x 0.2 μm x 12 μm x 0.037 pF/μm^2 = 0.18 pF. The parasitic capacitance related to the overlap was assumed to be $C_p = 6.0$ fF, see also section

[i] Taking the proximity effect into account, the effective junction area of the ramp-type junction was $A \approx 4.8$ μm^2. The critical current of the junction was $I_0 = 3.5$ μA, which means that the critical current density was only $J_c \approx 73$ A/cm^2. For this value of the critical current density, a specific capacitance of 0.037 pF/μm^2 is realistic.

6.2.3. The finger and thus the resistance of the underlying Al layer and the capacitance of the Al,AlO_x/Al layer were divided into sections with a length of 0.5 μm each. Furthermore, it was assumed that the thickness of the AlO_x layer and the thickness of the underlying Al layer were homogeneous over the whole length of the finger, i.e. the values of $R_{Al,i}$ and $C_{Al,i}$ were constant for all sections. For a section length of 0.5 μm, this means that $C_{Al,i} = 0.22$ pF. The resistance of the Al layer per section was assumed to be $R_{Al,i} = 0.56$ Ω, i.e. $\rho = 1.3 \cdot 10^{-7}$ Ωm. In order to fit the simulated results with the experimental results, two pinholes in the AlO_x layer at a distance of 10 μm from each ramp-type junction were modeled. The resistance of each pinhole was $R_{hole} = 10$ μΩ. This value is not important for the simulated *I-V* characteristics, as long as $R_{hole} \ll R_{Al,i}$.

Comparing the experimental *I-V* characteristics of the dc SQUID based on ramp-type junctions at 4.2 K and the simulated $n\Phi_0$ and $(n + ½)\Phi_0$ branches of the *I-V* characteristics using the extended model, it can be concluded that the experiments can be explained using realistic values for all parameters in the model. The $n\Phi_0$ and $(n + ½)\Phi_0$ branches of both the measured and the simulated *I-V* characteristics cross at a voltage of $V \approx 22$ μV, as is shown in Fig. A.2a. As a result of pinholes in the AlO_x layer, the junction is low-ohmically shunted, which removes the hysteresis in the *I-V* characteristics of the ramp-type junctions. However, if the AlO_x layer does not have any defects, the hysteresis of the junctions will not be removed, as can be concluded from Fig. A.2b. This figure shows the simulated $n\Phi_0$ branch of the *I-V* characteristics of a dc SQUID based on the extended model of the ramp-type junctions. All parameters were the same as above, except for the fact that in this simulation no pinholes were assumed to be present. In the simulation, the bias current was swept from zero to 20 μA and back to zero in 20 μs. Although the junction is hysteretic, the *R-C* shunt formed by the resistance of the underlying Al layer and the capacitance between this layer and the Nb counter electrode might limit the maximum operation frequency of devices based on these junctions. However, as was discussed in chapter 6, the effect of the underlying Al layer can be reduced in several ways, such that the maximum operation frequency can be increased.

Summary

The direct current superconducting quantum interference device (dc SQUID) is one of the most successful applications of superconductivity. It is well known to be the most sensitive sensor for magnetic flux currently available with a sensitivity that can approach the quantum limit and with a frequency response extending from dc to a few GHz. Because of their excellent characteristics, SQUID systems have a wide range of applications, e.g. the readout of cryogenic particle detectors or gravitational wave antennae and the detection of small magnetic fields produced by the human brain or heart. The subject of this thesis is the development and further improvement of both new and existing low-T_c SQUID systems.

A dc SQUID consists of a superconducting ring, interrupted by two weak links, the Josephson junctions. Generally, the dc SQUID is biased with a constant (dc) current, hence the name dc SQUID. In this current bias mode, the voltage across the SQUID is modulated by the magnetic flux which is applied to the SQUID loop. Thus a current-biased dc SQUID acts as a flux-to-voltage converter. Since any internal magnetic flux in superconductors exists only in discrete amounts, i.e. the flux is quantized, the voltage versus flux characteristic of a SQUID is periodic with a period equal to the flux quantum $\Phi_0 = 2.07 \cdot 10^{-15}$ Wb. In order to linearize its output, the SQUID is often operated as a null-detector in a feedback loop, the so-called flux locked loop (FLL). Conventionally, the FLL circuitry is implemented in room temperature electronics. However, the flux-to-voltage transfer of a standard dc SQUID is so small, typically of the order of 100 $\mu V/\Phi_0$, that a direct voltage readout mode would lead to preamplifier limitation of the overall system sensitivity, i.e. the output voltage noise of a SQUID is about one order of magnitude smaller than the input voltage noise of a low-noise room temperature dc preamplifier.

In order to solve the matching problem between the dc SQUID and the readout electronics, ac flux modulation together with a step-up transformer can be used. The modulation frequency is generally in the range of 100 to 500 kHz, which limits the usable measurement bandwidth. A few wideband ac flux modulated SQUID systems have been reported, but the complexity of these systems is much higher than that of direct voltage readout schemes. Another possibility to solve the matching problem is to increase the flux-to-voltage transfer of the SQUID. Various

second generation dc SQUIDs with a large flux-to-voltage transfer, e.g. two-stage SQUID systems, series SQUID arrays and double relaxation oscillation SQUIDs (DROSs), have been developed. Since no ac flux modulation is required for the readout of these devices, it is relatively easy to achieve a large system bandwidth. Even larger bandwidths can be achieved by using digital SQUIDs. A digital SQUID incorporates a SQUID and the complete FLL circuitry on one chip. Because of its high slew rate and large bandwidth, the digital SQUID is a promising candidate for high frequency applications, such as the readout of cryogenic particle detectors.

For the readout of cryogenic particle detectors, low-noise SQUID systems with a slew rate high enough to trace the full output signal of the detector are required. Currently, large arrays of cryogenic particle detectors are being developed, which require dedicated SQUID systems capable of reading out these arrays. The most straightforward approach would be to use one SQUID including readout electronics for each pixel. However, the large number of wires from the particle detectors to the SQUIDs and the room temperature electronics would form a major limitation on the maximum size of the array, because of, e.g., the large thermal load and the complexity of the readout electronics. A useful technique to reduce the number of wires is multiplexing.

First generation SQUID multiplexers for small particle detector arrays have been developed. NIST has developed a SQUID readout system based on time-division multiplexing and at the University of California a SQUID readout system based on frequency-division multiplexing has been developed. Using the correct filtering techniques, in principle the noise contributions from the different detectors do not add, but the bandwidth that can be achieved at each pixel is rather limited.

If the degradation of the signal-to-noise ratio (SNR) due to mixing of noise from different pixels is acceptable, code-division multiplexing can be used, which allows higher bandwidths. In that way, the bandwidth at each pixel is not reduced. The coded SQUID array that has been developed at the University of Twente is based on code-division multiplexing. In this system, each pixel has its own unique binary code representing its position in the array. Each pixel is connected to one or several SQUIDs, which is determined by this code. Using two of these coded SQUID arrays based on M and N SQUIDs respectively, $(2^M - 1)$ x $(2^N - 1)$ cryogenic particle detectors can be read out. Thus the coded SQUID array allows detector arrays to be read out by a significantly reduced number of SQUIDs.

Prototype coded SQUID arrays based on three conventional resistively shunted dc SQUIDs have been developed. Two of these systems can be used for the readout of 49 cryogenic detectors. Both calculations and experiments on these prototype systems showed that the amount of crosstalk between the different channels can be made negligible. Measurements on coded SQUID arrays connected to cryogenic particle detectors have not been performed yet.

For the readout of the sensor SQUIDs of the coded SQUID arrays, a two-stage configuration can be used in which a second stage SQUID is used as a low-noise cryogenic preamplifier. The large flux-to-voltage transfer of a two-stage SQUID system enables a direct voltage readout mode without degradation of the overall system sensitivity. The first stage of a two-stage SQUID system consists of a voltage-biased conventional resistively shunted dc SQUID, the sensor SQUID, that

acts as a flux-to-current converter. The current through this SQUID is converted to a magnetic flux that is coupled to the second stage SQUID, thereby introducing a flux gain. The flux gain should be sufficiently large, such that the amplified flux noise of the sensor SQUID is much larger than the noise contributions of the second stage and the readout electronics at room temperature.

Although it is beneficial to use a SQUID with a large flux-to-voltage transfer, in principle any type of SQUID can be used for the second stage. For example, two-stage SQUID systems based on a single dc SQUID or a series SQUID array as the second stage have been reported in literature. Because of the large flux-to-voltage transfer, the relatively large voltage modulation depth and the low noise level, the DROS is an excellent choice for the second stage SQUID. Experiments on a non-integrated design using two separate chips, i.e. one for the sensor SQUID and one for the DROS, showed that comparing to commercial ac flux modulated electronics, a two-stage SQUID system based on a DROS resulted in considerable performance improvement. The white flux noise of a conventional resistively shunted dc SQUID with an inductance of 100 pH measured using a commercial ac flux modulated SQUID controller was 4.3 $\mu\Phi_0/\sqrt{\text{Hz}}$. The design value for the white flux noise however, was 1.2 $\mu\Phi_0/\sqrt{\text{Hz}}$. In a two-stage setup using a DROS as a cryogenic preamplifier, the overall system noise was 1.3 $\mu\Phi_0/\sqrt{\text{Hz}}$ ($\varepsilon = 55\ h$).

The main advantage of a non-integrated two-stage SQUID system is that this configuration allows high design flexibility. However, the reliability and the intrinsic bandwidth of the systems can be improved by integrating the first and the second stage on one chip. The integrated two-stage SQUID systems based on a DROS that are discussed in this thesis had a flux-to-voltage transfer up to 3.6 mV/Φ_0. This large value allowed a direct voltage readout mode. The overall white flux noise level measured in FLL was 1.3 $\mu\Phi_0/\sqrt{\text{Hz}}$ ($\varepsilon = 27\ h$). This noise level corresponds to the theoretically expected value for the white flux noise of the sensor SQUID, which means that the noise contributions of the DROS and the readout electronics were negligibly small. At 1 Hz, the flux noise was ~9 $\mu\Phi_0/\sqrt{\text{Hz}}$. Using wideband FLL electronics based on direct voltage readout, a maximum closed loop bandwidth of 2.5 MHz, limited by the readout electronics, was measured and the slew rate was measured to be $1.3{\cdot}10^5\ \Phi_0/\text{s}$.

A DROS is not only a suitable choice for a second stage in a two-stage SQUID system, it is also one of the two key elements of the Smart DROS, a digital SQUID based on a DROS. A DROS consists of two hysteretic dc SQUIDs in series, the signal SQUID and the reference SQUID, shunted with an external *L*-*R* circuit. If an appropriate bias current is applied to the DROS, relaxation oscillations are generated. Only the SQUID with the smallest critical current participates in the relaxation oscillations and generates voltage pulses, while the other SQUID remains in the superconducting state. Thus the DROS acts as a critical current comparator. The time-averaged voltage versus flux characteristic of a DROS has a large maximum flux-to-voltage transfer, typically of the order of ~1 mV/Φ_0, at the points where the critical currents of the signal SQUID and the reference SQUID are equal.

Similarly to a two-stage SQUID system, the large flux-to-voltage transfer of a DROS enables direct voltage readout without ac flux modulation. The readout of a DROS is generally performed at room temperature using FLL electronics with a

bandwidth much smaller than the relaxation oscillation frequency, such that only the time-averaged dc component of the voltage pulses is measured. In the Smart DROS however, the pulsed output of the DROS is used for digital readout. Besides the DROS, the second key element of the Smart DROS is a superconducting up-down counter, the Josephson counter. The voltage pulses of the DROS serve as the input for the Josephson counter and the output of the counter is fed back to the signal SQUID and supplies the feedback flux. The relaxation oscillations of the DROS serve as an on-chip clock signal, such that no external clock is required, which is an important advantage compared to other digital SQUID concepts.

Using an on-chip FLL circuitry, the dead-time in the feedback loop of the Smart DROS can be reduced significantly, which enables very large bandwidths and very high slew rates. To fully benefit from the Smart DROS concept, the design was optimized with respect to the output range of the Josephson counter, the coupling between the DROS and the counter and the quantization unit of the feedback flux. The quantization unit of the feedback flux should be equal to the broadband flux noise of the DROS. A larger value leads to quantization errors, whereas a smaller quantization unit means that the Smart DROS unnecessarily compensates for its own noise, such that the bandwidth and the slew rate will be compromised.

For an optimized Smart DROS, the quantization unit of the feedback flux is typically of the order of 50 $m\Phi_0$. The optimum value for the quantization unit is independent on the relaxation oscillation frequency. An optimized Smart DROS with a relaxation oscillation of 100 MHz was designed, fabricated and characterized. The relaxation oscillation frequency was limited to 100 MHz to make a possible digital readout scheme, using a second counter at room temperature to reconstruct the applied signal, easier. The maximum slew rate was $5 \cdot 10^6$ Φ_0/s. The experimental results confirmed the proper operation of the DROS, but a digital readout scheme has to be further developed to profit from the full potential of the Smart DROS.

In order to increase the amplitude of the voltage pulses generated by the Smart DROS, and to increase the relaxation oscillation frequency such that both the bandwidth and the maximum slew rate can be increased, the capacitance of the Josephson junctions has to be decreased. Simulations showed that slew rates as high as $3 \cdot 10^8$ Φ_0/s are possible by increasing the relaxation oscillation frequency to 5 GHz. Also the white noise levels of the Smart DROS and of the two-stage SQUID system can be improved by reducing the junction capacitance and thus the junction area. Therefore, small-area Josephson junctions based on a ramp-type configuration have been developed. The experimental current versus voltage characteristics of the first junctions showed non-hysteretic behavior, caused by a parasitic resistance in parallel with the junction. Numerical analysis of the ramp-type junctions showed that the non-hysteretic behavior could be explained by assuming pinholes in the AlO_x layer that lies under the counter electrode. However, promising results on the first ramp-type dc SQUIDs encourage further development of the ramp-type junctions, which could result in very low-noise two-stage SQUID systems and very fast Smart DROSs.

Samenvatting (Summary in Dutch)

Het SQUID, een acroniem voor *Superconducting QUantum Interference Device*, is één van de succesvolste toepassingen van supergeleiding. Momenteel is het SQUID de gevoeligste sensor voor magnetische flux. De grensgevoeligheid van deze sensor kan de kwantumlimiet benaderen en het frequentiebereik is dc tot een paar GHz. Vanwege deze eigenschappen worden SQUIDs voor vele toepassingen gebruikt, waaronder de uitlezing van deeltjes- en gravitatiegolfdetectoren en de detectie van zeer kleine magneetvelden die door de hersenen en het hart worden opgewekt. In dit proefschrift wordt de ontwikkeling van nieuwe lage-T_c SQUIDs en de optimalisatie van bestaande lage-T_c SQUIDs beschreven.

Een dc SQUID bestaat uit een supergeleidende ring die onderbroken wordt door twee zwakke koppelingen, de Josephson juncties. In het algemeen wordt het SQUID gevoed met een constante (dc) elektrische stroom, vandaar de naam dc SQUID. De elektrische spanning over het SQUID is in dat geval afhankelijk van de magnetische flux die in het SQUID wordt gekoppeld. Een stroom-gebiast SQUID is dus een flux-naar-spanning omzetter. Omdat de magnetische flux in een supergeleidende ring gekwantiseerd is, is de uitgangsspanning periodiek afhankelijk van de aangeboden flux met het fluxkwantum $\Phi_0 = 2.07 \cdot 10^{-15}$ Wb als periode. Meestal wordt het uitgangssignaal van het SQUID door middel van een terugkoppeling, de *flux locked loop* (FLL), gelineariseerd. Normaliter wordt de FLL gerealiseerd door gebruik te maken van elektronica op kamertemperatuur. De flux-naar-spanning coëfficiënt van een standaard dc SQUID is echter zo klein, typisch 100 $\mu V/\Phi_0$, dat in het geval van directe spanningsuitlezing de grensgevoeligheid van het systeem beperkt wordt door de voorversterker. Uitgedrukt in ruisspanningen is de uitgangsruisspanning van een SQUID namelijk een grootteorde lager dan de ingangsruisspanning van een ruisarme dc voorversterker op kamertemperatuur.

Om te voorkomen dat de elektronica op kamertemperatuur de gevoeligheid van het SQUID-systeem beperkt, kunnen fluxmodulatietechnieken en transformatoren worden gebruikt. Veelal ligt de modulatiefrequentie tussen 100 kHz en 500 kHz, waardoor de bruikbare bandbreedte vrij klein is. Hogere modulatiefrequenties zijn mogelijk, maar hebben tot gevolg dat de elektronica complexer wordt. Het is echter ook mogelijk de flux-naar-spanning coëfficiënt van het SQUID te vergroten, zodat

directe spanningsuitlezing mogelijk is zonder dat de voorversterker de gevoeligheid beperkt. Voorbeelden van tweede generatie dc SQUIDs met een grote flux-naar-spanning coëfficiënt zijn tweetraps SQUIDs, in serie geschakelde SQUID-arrays en dubbele relaxatie oscillatie SQUIDs (DROSen). Omdat modulatietechnieken niet vereist zijn, is een breedbandig systeem gebaseerd op tweede generatie dc SQUIDs relatief eenvoudig te realiseren. De bandbreedte van een digitaal SQUID, een chip met daarop het SQUID en de gehele FLL-elektronica, kan echter nog groter zijn. Vanwege de grote bandbreedte en hoge volgsnelheid is het digitale SQUID zeer geschikt voor hoogfrequente toepassingen, zoals de uitlezing van deeltjesdetectoren.

Om het uitgangssignaal van cryogene deeltjesdetectoren te kunnen meten, zijn ruisarme SQUID-systemen met een grote volgsnelheid vereist. Op dit moment is er veel belangstelling voor de ontwikkeling van grote arrays van deeltjesdetectoren. Om deze arrays te kunnen uitlezen, zijn echter speciale SQUID-systemen nodig. Indien men voor elke afzonderlijke pixel één SQUID met de benodigde elektronica zou gebruiken, zou het grote aantal draden tussen de deeltjesdetectoren, de SQUIDs en de elektronica op kamertemperatuur een grote beperking vormen voor het maximum aantal pixels. Een groot aantal draden betekent immers een zeer complex uitlezingsschema en een groot warmtelek. Door multiplexing toe te passen kan het aantal draden echter aanzienlijk worden verminderd.

De eerste generatie SQUID-multiplexers voor de uitlezing van kleine arrays zijn reeds ontwikkeld. NIST heeft een SQUID-multiplexer ontwikkeld die gebaseerd is op *time-division* multiplexing en op de Universiteit van Californië is een systeem ontwikkeld dat gebaseerd is op *frequency-division* multiplexing. Door gebruik te maken van filters kan worden voorkomen dat de ruissignalen van de verschillende detectoren bij elkaar worden opgeteld en dat de signaal-ruisverhouding afneemt. In beide systemen is de bandbreedte per pixel echter vrij beperkt.

Indien de afname van de signaal-ruisverhouding acceptabel is, kan *code-division* multiplexing worden toegepast, waarmee grotere bandbreedtes mogelijk zijn. De gecodeerde SQUID-array die ontwikkeld is op de Universiteit Twente maakt hier gebruik van. Met behulp van een binaire code wordt elke pixel in dit systeem gecodeerd. Elke pixel is aangesloten op één of meerdere SQUIDs, wat bepaald wordt door deze code. Met twee gecodeerde SQUID-arrays, gebaseerd op respectievelijk M en N SQUIDs, kunnen $(2^M - 1)$ x $(2^N - 1)$ cryogene deeltjesdetectoren worden uitgelezen. Het aantal SQUIDs dat nodig is voor de uitlezing van een array van cryogene deeltjesdetectoren kan dus aanzienlijk worden verminderd.

In dit proefschrift worden prototype gecodeerde SQUID-arrays beschreven die gebaseerd zijn op drie standaard dc SQUIDs. Twee van deze systemen kunnen worden gebruikt voor de uitlezing van 49 cryogene detectoren. Zowel berekeningen als experimenten toonden aan dat de hoeveelheid overspraak tussen aangrenzende kanalen verwaarloosbaar kan worden gemaakt. Metingen aan gecodeerde SQUID-arrays gekoppeld aan cryogene deeltjesdetectoren zijn nog niet uitgevoerd.

Voor de uitlezing van de SQUIDs van de gecodeerde SQUID-arrays kan een tweetraps configuratie worden gebruikt. Het tweede SQUID in een dergelijk systeem functioneert als een ruisarme, cryogene voorversterker. De grote flux-naar-spanning coëfficiënt van een tweetraps SQUID maakt het mogelijk directe spanningsuitlezing te gebruiken zonder dat de gevoeligheid van het SQUID-systeem

afneemt. De eerste trap van een tweetraps SQUID bestaat uit een spanning-gebiast standaard dc SQUID, het sensor-SQUID, en werkt als een flux-naar-stroom omzetter. De stroom door dit SQUID wordt omgezet in een magnetische flux die in het tweede SQUID wordt gekoppeld. Het tweetraps SQUID is zodanig ontworpen dat er sprake is van fluxversterking. De fluxversterking moet zo groot zijn dat de versterkte fluxruis van het sensor-SQUID vele malen groter is dan de ruisbijdragen van de tweede trap en de elektronica op kamertemperatuur.

In principe kan elk type SQUID worden gebruikt voor de tweede trap. In de literatuur zijn bijvoorbeeld tweetraps SQUIDs gebaseerd op één SQUID of een in serie geschakelde SQUID-array als tweede trap vermeld. Vanwege de grote flux-naar-spanning coëfficiënt, de relatief grote spanningsmodulatie en het lage ruisniveau is een DROS zeer geschikt als tweede trap. Experimenten aan een niet-geïntegreerd ontwerp, bestaande uit één chip voor het sensor-SQUID en één voor het DROS, toonden aan dat vergeleken met commerciële gemoduleerde SQUID-elektronica een tweetraps SQUID gebaseerd op een DROS tot een aanzienlijke verbetering van de ruiseigenschappen leidt. Van een standaard 100 pH SQUID dat werd uitgelezen met commerciële SQUID-elektronica was de totale witte fluxruis 4.3 $\mu\Phi_0/\sqrt{\text{Hz}}$. De ontwerpwaarde van de witte fluxruis was echter 1.2 $\mu\Phi_0/\sqrt{\text{Hz}}$. De totale ruis van hetzelfde SQUID gemeten met een DROS als ruisarme, cryogene voorversterker was 1.3 $\mu\Phi_0/\sqrt{\text{Hz}}$ ($\varepsilon = 55\ h$).

Een belangrijk voordeel van een niet-geïntegreerd tweetraps SQUID is dat de configuratie zeer flexibel is. De betrouwbaarheid en de intrinsieke bandbreedte van een tweetraps SQUID kunnen echter verbeterd worden door zowel de eerste als de tweede trap te integreren op één chip. De geïntegreerde tweetraps SQUIDs die in dit proefschrift worden besproken, hebben een grote flux-naar-spanning coëfficiënt, tot 3.6 mV/Φ_0, zodat een directe spanningsuitlezing mogelijk is. De fluxruis gemeten in FLL was 1.3 $\mu\Phi_0/\sqrt{\text{Hz}}$ ($\varepsilon = 27\ h$). Deze waarde komt overeen met de theoretisch verwachte waarde van de witte ruis van het sensor-SQUID, wat betekent dat de ruisbijdragen van het DROS en de elektronica verwaarloosbaar zijn. Bij 1 Hz was de fluxruis ~9 $\mu\Phi_0/\sqrt{\text{Hz}}$. De maximum bandbreedte in FLL was 2.5 MHz en werd beperkt door de elektronica op kamertemperatuur. De maximum volgsnelheid was $1.3{\cdot}10^5\ \Phi_0/\text{s}$.

Een DROS is niet alleen zeer geschikt als tweede trap in een tweetraps SQUID, maar het is ook één van de belangrijkste elementen van het Smart DROS, een digitaal SQUID gebaseerd op een DROS. Een DROS bestaat uit twee in serie geschakelde, hysteretische dc SQUIDs, het signaal-SQUID en het referentie-SQUID, geshunt met een extern *L*-*R* circuit. Indien het DROS met een geschikte stroom wordt gevoed, ontstaan relaxatie oscillaties. Alleen het SQUID met de kleinste kritische stroom neemt deel aan het relaxatie oscillatie proces. Dit SQUID genereert spanningspulsen en het andere SQUID blijft in de supergeleidende toestand. De in de tijd gemiddelde spanning-versus-flux karakteristiek heeft een grote flux-naar-spanning coëfficiënt op de punten waar de kritische stromen van het signaal-SQUID en het referentie-SQUID gelijk zijn. Een typische waarde is 1 mV/Φ_0.

De grote flux-naar-spanning coëfficiënt van een DROS maakt een directe spanningsuitlezing zonder modulatietechnieken mogelijk. Normaal gesproken wordt het DROS uitgelezen met behulp van FLL-elektronica op kamertemperatuur. De

bandbreedte van de FLL-elektronica is veel kleiner dan de relaxatiefrequentie, zodat alleen de dc-component van de spanningspulsen wordt gemeten. Echter, in een Smart DROS wordt het gepulste uitgangssignaal van het DROS gebruikt voor een digitale verwerking. De spanningspulsen van het DROS dienen als ingangssignaal voor een supergeleidende, bidirectionele teller. Deze zogenaamde Josephson-teller zorgt voor een terugkoppeling op de chip zelf: het uitgangssignaal van deze teller levert de terugkoppelingsflux. Aangezien de relaxatie oscillaties een interne klok vormen, is er geen externe klok nodig. Dit is een belangrijk verschil met en een groot voordeel ten opzichte van andere digitale SQUIDs.

Doordat de terugkoppeling van een Smart DROS op de chip geschiedt, kan de dode tijd in de terugkoppeling aanzienlijk worden gereduceerd, zodat een zeer grote bandbreedte en een zeer hoge volgsnelheid mogelijk zijn. Om volledig van het Smart DROS-concept te kunnen profiteren, is het ontwerp geoptimaliseerd met betrekking tot het meetbereik van de Josephson-teller, de koppeling tussen het DROS en de teller en het discretisatieinterval van de terugkoppelingsflux. In een geoptimaliseerd Smart DROS is het discretisatieinterval van de terugkoppelingsflux gelijk aan de amplitude van de breedbandige fluxruis van het DROS. Een grotere waarde leidt tot kwantisatieruis en een kleinere waarde heeft tot gevolg dat het Smart DROS onnodig de eigen fluxruis compenseert, waardoor de bandbreedte en de volgsnelheid worden beperkt.

Een typische, geoptimaliseerde waarde voor het discretisatieinterval van de terugkoppelingsflux is 50 $m\Phi_0$. Het optimale discretisatieinterval is onafhankelijk van de gebruikte relaxatiefrequentie. Een geoptimaliseerd Smart DROS met een relaxatiefrequentie van 100 MHz is ontworpen, gefabriceerd en gekarakteriseerd. De relaxatiefrequentie was beperkt tot 100 MHz om de ontwikkeling van een digitaal uitlezingsschema, dat gebruik maakt van een tweede teller op kamertemperatuur voor de reconstructie van het aangeboden signaal, te vereenvoudigen. De maximum volgsnelheid was $5{\cdot}10^6$ Φ_0/s. Experimenten toonden de correcte werking van het Smart DROS aan, maar om de volledige potentie van het Smart DROS te kunnen benutten, moet het digitale uitlezingsschema verder worden ontwikkeld.

Om de amplitude van de spanningspulsen die door het Smart DROS worden gegenereerd en om de relaxatiefrequentie te vergroten, zodat zowel de bandbreedte als de volgsnelheid toenemen, moet de capaciteit van de Josephson juncties worden verminderd. Simulaties toonden aan dat volgsnelheden tot $3{\cdot}10^8$ Φ_0/s kunnen worden bereikt door de relaxatiefrequentie van het DROS te verhogen tot 5 GHz. Tevens verbeteren de ruisniveaus van zowel het Smart DROS als het tweetraps SQUID indien de capaciteit en dus de junctieoppervlakte verkleind worden. Daarom zijn hellingstype Josephson juncties met een kleine oppervlakte ontwikkeld. De experimentele stroom-versus-spanning karakteristieken van de eerste juncties waren niet-hysteretisch. Dit werd veroorzaakt door een parasitaire weerstand parallel aan de junctie. Numerieke analyse toonde aan dat het niet-hysteretisch gedrag zeer waarschijnlijk te wijten is aan defecten in de AlO_x-laag die onder de bovenste elektrode ligt. De veelbelovende resultaten die behaald zijn met de eerste hellingstype dc SQUIDs sporen aan tot verder onderzoek naar en ontwikkeling van hellingstype juncties, waardoor in de toekomst zeer ruisarme tweetraps SQUIDs en zeer snelle Smart DROSsen mogelijk zullen zijn.

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