Electrostatic Discharge Effects in Thin Film Transistors

Natasa Golo

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ELECTROSTATIC DISCHARGE EFFECTS IN THIN FILM TRANSISTORS

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Cover page: The cover photo is taken during Liquid Crystal Hot Spot measurements on a fingerprint sensor.

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PROEFSCHRIFT

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in het openbaar te verdedigen
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door

Nataša Golo, geboren Tošić
op 11 december 1969 te Niš, Servië, Joegoslavië

Dit proefschrift is goedgekeurd door
de promotor Prof. dr. ir. Fred G. Kuper en
de assistent-promotor Prof. dr. ir. A. J. Mouthaan.

To Goran and Sofija

Thank you!

It rained for four years, eleven months and two days. There were periods of drizzle during which everyone put on his full dress and a convalescent look to celebrate the clearing, but people soon grew accustomed to interpret the pauses as a sign of redoubled rain. This is how a chapter in "One hundred years of solitude", by G. G. Marquez, begins. A PhD student coming from Yugoslavia to the rainy Netherlands, could indeed easily condemn himself to solitude. Many people have generously helped me to overcome this feeling and I would like to thank them all.

At the first place, I want to thank my promoter Fred Kuper and my co-promoter Ton Mouthaan, for supervising my work and for guiding me in my research. I would like to mention how much I appreciate constantly supportive and constructive remarks of Fred. I will never forget how much Ton helped me in the testing room, when he was literally assisting me during one of my first soldering experiences. I also would like to thank Ton for many sincere both scientific and social discussions that we had, during which he was often a good and strong opposition.

My PhD research was closely related to Philips. I am very thankful to Jeremy Sandoe who helped in organisation of my short but efficient staying in PRL, England. While I was there I have heard some very competent advices from John Hughes and Steve Deane related to my research on thermal simulations. Thanks to Michael Pitt, with whom I had the most agreeable collaboration, and the samples he sent me from Philips MDS, Japan, I got opportunity to investigate how ESD protections work. Thanks to Gerard Harkin and Niel Bird I got some first ideas about fingerprint sensor. Benno Krabbenborg helped me introducing me with LUMEX and electro-thermal simulations. Some very fruitful discussions I had with Theo Smedes, though unfortunately just at the end of my PhD study.

Many other people contributed to my PhD thesis. I would like to acknowledge Bernd Stannowski from the Utrecht University for DOS and FTIR help. Prof. Jan F. Verweij for some good advises about testing strategies. Kees Revenberg who helped me to organise FIB and LCHS and

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During my PhD study I had opportunity to cooperate with master students through my educational tasks. I am indefinitely indebted to Siebrigje van der Wal for her contribution on density of states calculation and for being such a pleasant companion to work with. D1 project students, generation 2000, 2001 also gave their input on the fingerprint system.

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I want to mention my Dutch class, meaning my dear classmates and our teacher Inge, which was always so positively charged, and where I met Corina and Petrica, who became very close and dear friends. And also my old Serbian friends who are now in the Netherlands and were my friends and colleagues back in Serbia, Silvana and Slobodan, Milena and Dragan, Nenad. I liked very much our large Serbian barbecue community here in Enschede. I am especially thankful to Jelena and Boris, Vesna and Marko, and all the others who really cared about my problems and progress.

I have always had enormous support of my family. I will always be obliged to my late father who instilled in me love for science, my mama who is always ready to jump in and give even more that she should, my only brother Vlada who could always cheer me up, and my 14 years old dog Oskar who still waves when I come "home", even it is once per year.

Most of all, I want to thank to my husband Goran and my baby Sofija. They were just simply always there, encouraging me in every possible way to accomplish my PhD thesis. This comes from my ♡.

Nataša Golo

Contents

Chapter 1

Amorphous silicon thin film transistors

A short introduction into the world of amorphous silicon thin film transistors will be given in this chapter. An overview of the current developments of thin film transistors based on amorphous silicon will be shown. The most important facts about understanding the physics, the fabrication and modelling of thin film transistors will be presented. A short retrospect concerning the process of degradation due to electrical stress will be introduced and depicted with an example. Finally the content of this thesis will be introduced.

1.1 Introduction

Thin Film Transistors (TFT's) are indispensable in large area electronics. Hydrogenated amorphous silicon (α-Si:H) TFT's, or polysilicon TFT's are as important for large area electronics as crystalline MOS transistors for integrated circuits. TFT's have found their place in low temperature electonics ($\sim 100^oC$), or for deposition over a large area ($1m^2$), where crystalline silicon could not be used. In Active-Matrix Liquid Crystal Displays (AMLCD's), amorphous silicon TFT's are most often used as switching devices inside each pixel in the display (TFTLCD's). The use of a TFT in this way was introduced more then 20 years ago [19].

1.1.1 Working of α-Si:H TFT's

Thin film transistors have obtained their name as they are made of thin films usually deposited on an insulating substrate. A cross-section of a thin film transistor is shown in Fig. 1.1. The picture was taken by a Transmission Electron Microscope (TEM), on a sample prepared by Focus Ion Beam (FIB).

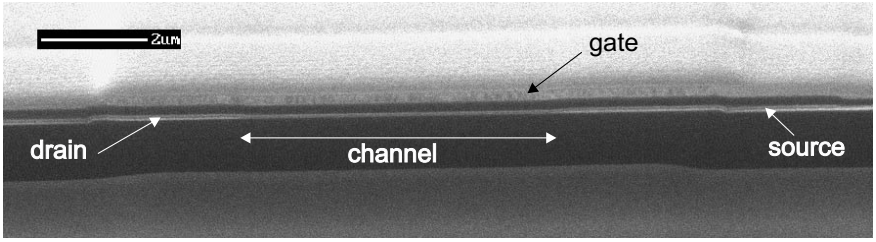

Figure 1.1: Cross-section of a thin film transistor.

Amorphous silicon

The α-Si:H TFT's are built on glass substrate. That is a necessity in display industry, otherwise the light could not pass through the display. As glass has a relatively low melting point ($\sim 600^oC$), it means that all technology processes of TFT deposition are temperature limited. The channel material of TFT's is amorphous silicon. Amorphous silicon thin films are commonly produced using a glow discharge technique, also known as Plasma Enhanced Chemical Vapour Deposition (PECVD). A silicon rich gas (usually silane SiH_4) is admitted to a vacuum reactor chamber. Then discharge is initiated and maintained by an electric field between two parallel plates [48]. The hydrogen was recognised as being essential for tightening up the unpaired valence electrons that would otherwise lead to electronic defect states. The main advantages of α-Si:H are that it can be deposited over a large area and at the low temperature [71]. A disadvantage is poor electron mobility (μ <1 cm^2/Vs). Therefore the conductivity, which is related to the electron mobility μ and the density of states in the band gap $N(E)$ by 1.1 is very poor as well.

$$\sigma = qn\mu = q\int N(E)\mu(E)f(E)dE = g\int N(E)\mu(E)exp(-\frac{E-Ef}{kT}) \quad (1.1)$$

The problem is up to some level lessened by introducing the proper amount of hydrogen into amorphous silicon. Hydrogen atoms are small and can move easy through the network of amorphous silicon. In that way some of the dangling silicon bonds are compensated [58], making the density of gap states lower and the electron mobility higher. The conductivity of α-Si:H is determined by transport in the extended states at the band edge. Fig. 1.2 shows the conductivity of α-Si:H as a function of the doping gas concentration [48] [59]. Fig. 1.2 was firstly published by Spear and Le Comber [57]. From Fig. 1.2 can be seen that α-Si:H is *n-type when undoped*. This comes from the defect states in the band gap. Therfore an n-type TFT operates in accumulation and not in inversion, like an n-type MOS transistor.

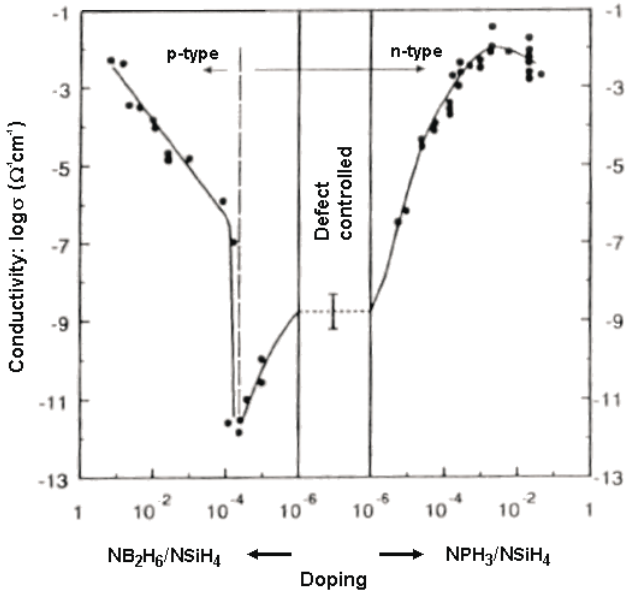

Figure 1.2: The variation of the room temperature dc conductivity of α-Si:H films doped by the introduction of phosphine and diborane into the deposition gas (Spear and LeComber).

Another important issue in α-Si:H is that it is very sensitive to light. It was discovered in 1977 that prolonged illumination of light causes creation of additional localised gap states [59]. To minimise creation of light induced defects, α-Si:H layer in a TFT switch in AMLCD's is normally shielded

from the back-light.

Thin film transistor structures

There are four possible TFT structures: staggered (top-gate), inverted staggered (bottom-gate), coplanar and inverted coplanar structure. A staggered structure has the source and drain contacts located on one side of the semiconductor and the gate electrode on the opposite side. Inverted means that the gate electrode is deposited first and therefore it is at the bottom of the TFT. A coplanar structure and inverted coplanar structure have all three contacts on the same side of the semiconductor film. Both top-gate and bottom-gate staggered structure are used in commercial production. Bottom gate devices show better interface properties than top-gate devices. Another advantage is that light shield for back light illumination is not needed as the amorphous silicon layer is protected by the gate layer itself. This structure is widely used in display industry and it can be found in two variations: so called back channel etch (BCE) and etch stop (ES) structure. On the other side, the top-gate TFT fabrication has an important advantage that it needs less photolithography masks. It is important to mention that fabrication process of TFT's is relatively simple and cheap, as only few photolithography masks are needed for the TFT processing. In this thesis both staggered and inverted staggered structures will be under investigation.

Analytical models of α-Si:H

α-Si:H TFT's are basically similar to MOS (Metal-Oxide-Semiconductor) devices. The only difference is that instead of oxide, mainly silicon nitride is used as the gate dielectric, as it produce better surface properties in amorphous silicon (less defects in the upper part of the band gap), and instead of crystalline, amorphous silicon is used as the channel material. Another important difference is that there is no bulk contact (as the substrate is from insulating material). The principle of operation is still the same as in crystalline MOS transistors. Therefore they can be well described by standard MOS equations. An analytic model for amorphous silicon TFT's based on MOS equations is previously published by Shur [52]. The application of a gate voltage V_G induces a free charge density in the channel region. Applying a drain voltage V_D provides flow of the current. For a drain voltage,

V_D, range of $0 \leq V_D \leq (V_G - V_T)$, the drain current is given by:

$$I_D = \mu_n C_i \frac{W}{L}((V_G - V_T)V_D - \frac{V_D^2}{2}) \tag{1.2}$$

Where $C_i = \frac{\epsilon_i}{d_i}$ is the gate capacitance per unit area, W is the channel width, L is the channel length and V_T is the threshold voltage. For low drain voltage ($V_D < 1$), the drain current belongs to the linear regime of operation and 1.2 is reduced to:

$$I_D = \mu_n C_i \frac{W}{L}((V_G - V_T)V_D) \tag{1.3}$$

For $V_D > V_G - V_T$ the drain current is saturated. Saturation of the current occurs due to the pinch-off of the conducting channel in the vicinity of the drain. The saturation current is given by:

$$I_{Dsat} = \frac{1}{2}\mu_n C_i \frac{W}{L}(V_G - V_T)^2 \tag{1.4}$$

Finally, to give an example of TFT's working, a typical set of measured $I_D(V_D)$ characteristics for a top-gate TFT with the channel dimensions $L = 6\mu m$ and $W = 100\mu m$, under different voltages applied on the gate $V_G = 20V \div 50V$, is shown in Fig. 1.3. It can be seen in Fig. 1.3 that there are

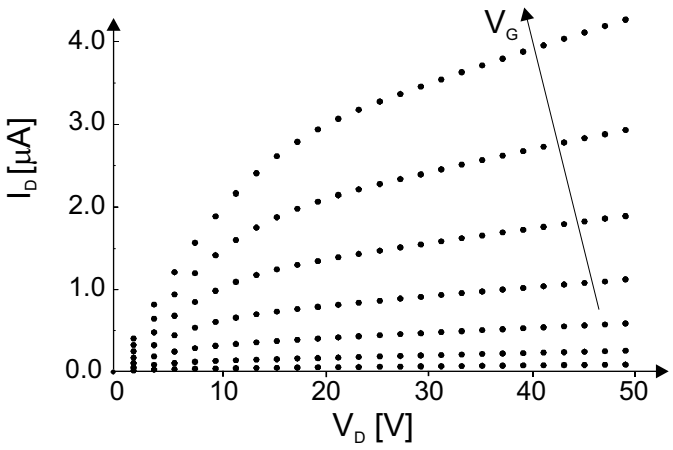

Figure 1.3: A typical set of measured $I_D(V_D)$ characteristics of an α-Si:H TFT.

two distinguished regions of working: linear and saturation. It also can be noticed that current in the saturation regime is not flat. That is particularly

expressed for short-channel TFT's (in this investigation all TFT's with $L < 9\mu m$ are considered as short-channel TFT's) and is not included in the described model. A significant concern for short channel α-Si TFT design is possible self-heating of the device due to high thermal resistance and large heat dissipation density [55]. This self-heating effect has been described in detail for silicon-on-insulator (SOI) MOS transistors [8]. In α-Si:H TFT's, the low thermal conductivity of the glass substrate prevents effective cooling of the TFT's. Self-heating effects have been observed in short channel TFT's as a lack of saturation at high drain biases [31]. Instead the slope of the output characteristics increases steadily with V_{DS}. The effect of self-heating is clearly visible at high drain and gate biases.

1.1.2 Instabilities in α-Si TFT's

A short review of the existing theory of instabilities in amorphous silicon will be given in this section. Beside that, some experiments with instabilities in α-Si TFT's will be reported here [64].

The instabilities in α-Si:H TFT's were subject of research of many researchers during last twenty years. Stability of TFT's upon prolonged positive and negative gate-bias application or light soaking has been already well described (see for example [22], [7], [29], [33], [44], [56]). It was shown that amorphous silicon TFT's suffer from very pronounced electrical instabilities, such as threshold voltage shift and also change in the transconductance $\frac{dI_D}{dV_G}$ when they are exposed to prolonged biasing on the gate. These electrical instabilities in TFT's are due to charge trapping (located in the gate dielectric or at the silicon-dielectric interface), and/or creation of gap states in the amorphous silicon itself.

An example of what is happening during electrical stress will be given [64]. A DC voltage was applied on the drain and the gate of a TFT. It was ramped up by steps of height 1 V and time duration 1 s, in the range of 0-100 V. The source was grounded. The stress voltage was ramped up to 40 V, when the experiment was stopped and the TFT was taken out for measuring transfer characteristics. Without cooling, the transfer characteristic $I_D(V_G)$ was measured in the linear region, with drain voltage V_D=1 V. Immediately after, the testing was continued by increasing voltage up to 60 V, when the second break point has been made. A control measurement was performed in the same way. After that the experiment was continued in the same manner. The next intermediate points were at 80 V and 100 V. During stressing electrical current was measured and it is shown in Fig. 1.4.

In Fig. 1.4 is important to notice that before failure point (which hap-

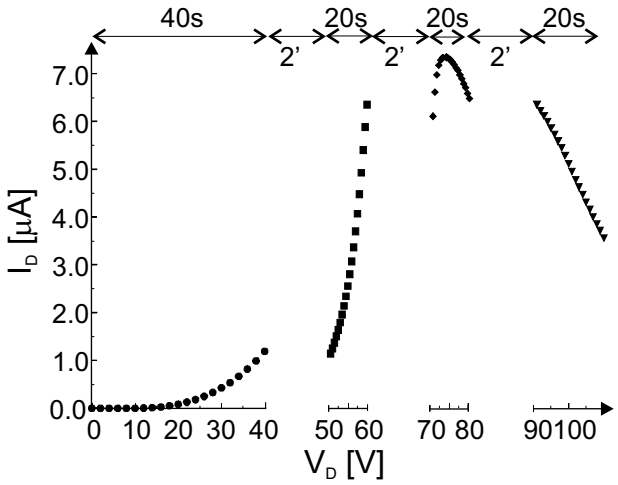

Figure 1.4: An experimental curve showing degradation process in an α-Si:H TFT.

pens close to 70 V) the current is increasing with increasing voltage ($\sim V^2$), and after failing current starts to decrease with increasing voltage (TFT damaged). Fig. 1.5 shows $I_D(V_G)$ characteristics measured in 2 minutes long break points. It can be observed that even before failing the transfer characteristic of TFT shifted for $\sim 10V$. The shift of the transfer characteristics represent actually an increase of threshold voltage. This large shift of transfer characteristics is either due to the charge trapping or due to creation of the states in the amorphous silicon layer.

1.2 Motivation

Although a lot of effort has been made to clarify the instabilities of electrical characteristics of thin film transistors, very little is known about their behaviour under severe stress conditions such as electrostatic discharge stress (ESD). And on the other side, ESD failure is a hot topic in the display industry, as a large part of the damaged TFT displays originates from ESD failure. The ESD problem is even more severe then in IC's as the TFT's are built on the insulating substrate and often over the large area. Further, it is not possible to design an effective ESD protection using MOS transistors switched as bipolar transistors, the conventional solution for ESD protection in IC's.

Therefore the motivation for this work was the need for explanation of

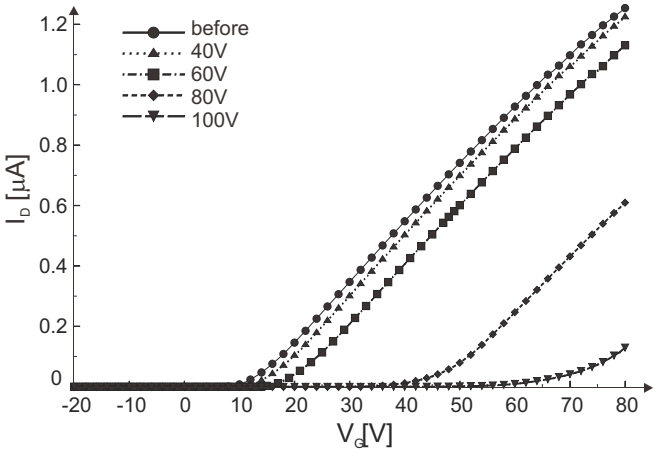

Figure 1.5: Shift of transfer characteristics due to the electrical stress.

ESD failure in α-Si:H TFT's. This knowledge is necessary required in the design of the transistors used in a ESD protection circuit. One of the first goals of this work was to identify failure under ESD stress and to model the failure. It was expected that α-Si:H TFT behave similarly to crystalline MOS transistors under ESD stress. It will be disproved in this thesis. It will be clarified how a α-Si:H TFT respond to an ESD zap. The further challenge is to apply this knowledge for the purpose of design of ESD protection for TFT circuits.

1.3 Outline of the thesis

This thesis is focused towards testing and protection of hydrogenated amorphous silicon thin film transistors for electrostatic discharge. The research starts with the experiments with ESD stress on single TFT's. The results are further analysed and the ESD event in a single TFT is clarified. Then an example of TFT circuit is manufactured and presented. Further ESD event is investigated in TFT displays, by means of experiments and circuit simulations. Finally the role of the ESD protection structures is discussed. The body of the thesis is organised as follows.

Chapter two gives the results of testing of grounded gate single TFT's on ESD stress. It describes the discharge event and how it can be modelled. Damage mechanisms and failures are dealt with. Dependence of the breakdown voltage on technology parameters (channel length and width) is

discussed. Also dependence of degradation and damage on stress duration. The results published in this chapter are based on the author's publications [65], [66], [70], [47], [21], [68].

In *chapter three* electro-thermal simulations with a circuit simulator are used to identify the distribution and dissipation of temperature in α-Si:H TFT under ESD stress conditions. It is presented how the thermo-electrical network is generated. A part of the results from this chapter are published, see [67].

In *chapter four* the influence of ESD stress on density of band gap states in amorphous silicon is estimated. Density of states is calculated before and after ESD stress and the impact of ESD stress is estimated. The results from this chapter are published in [69].

A practical example of an ESD problem in α-Si:H TFT circuit is presented in *chapter five*. The application example, fingerprint sensor, is built. and furthermore it will be tested on ESD. Process flow and the results of the electrical and material characterisation is presented. The weakest point of the sensor, ESD sensitivity, is analysed. The solution of the problem is discussed.

Finally *chapter six* gives an answer to the questions that we have often met about how to design a TFT-based ESD protection structure. It is analysed by means of electrical measurements and circuit simulations how a TFT display responds on ESD stress. Also the role of existing ESD protection is tested and simulated. From the analysis of this ESD protection structures a number of recommendations for the design of ESD protection in TFT circuits is drawn.

Chapter seven summarises the research and highlights the findings. Recommendations for further research in the field of ESD stress on α-Si:H TFT's are given.

Chapter 2

Electrostatic discharge stress on grounded gate α-Si:H TFT's

A short introduction about electrostatic discharge stress will be given in this chapter. The results of the ESD testing on amorphous silicon TFT's will be shown. The most important results of the testing with regard to the design parameters and the stress duration will be listed and analysed. The electrical model of degradation prior to electrical breakdown will be given. The results of failure analysis of the electrical breakdown will be shown.

2.1 Electrostatic discharge theory

Electrostatic discharge is a fast event of passing the triboelectric charge accumulated in an object (such as a human body or a transistor) to a grounded object. It happens in every day life all the time. People are every day electrically charged and discharged. The process of discharge can be a small event, as the stinging sensation that you sometimes feel when you touch the metal door handle, or it can be catastrophic event as it is the touch of a lightening. Something very similar happens with transistors. The only difference is that even a very low voltage, which a human body can take without any consequences, could damage or even destroy a transistor.

2.1.1 Electrostatic discharge models

When an electrostatic discharge failure is observed in an integrated circuit, an analysis process aimed at identifying and solving the problem must follow. The basic failure mechanisms and electrical behaviour of a device influenced by ESD can be reproduced in a simpler form by using a brief voltage pulse. Different experimental models are developed depending on the way in which such brief voltage pulse originates. These ESD models are actually equivalent circuits or waveforms representing charging events experienced by semiconductor devices. The most widely accepted model for the use in industry quality and reliability testing is the Human Body Model (HBM). It represents human interaction with semiconductor devices though a resistor R=1500 Ω and a capacitor C=100 pF. This model is defined by the ESD Association Standard 5.1 [16]. Very similar is the Machine Model (MM). It represents contact of tools with semiconductor devices by a capacitor C=200 pF. This model is defined by the ESD Association Standard 5.2 [17].It is primarily used in Japan and in the automotive industry [10]. The stress pulse in both model is modelled through the discharge of a charged capacitor. Furthermore, there is the Charged Device Model (CDM). In contrast with the previous two models, the stress pulse is obtained through discharge of the charged semiconductor device itself via a pin. This model is in the process of being defined. Currently there are two methods [10], one supporting the field-induced method [46] and the other supporting a socketed method ESD association standard D5.3 [18].

But unfortunately even the best models only approximate the reality. Apart of the approximate nature of the models, the ESD sensitivity of a device (defined in volts and determined by using any of the defined models) in reality is additionally disturbed by the effect of parasitic inductors and stray capacitors. Therefore the test results are only a rough approximation to the ESD event. ESD sensitivity testing of devices, whether performed using the CDM, MM or the HBM, is used to provide ESD sensitivity levels for the comparison of one device to another, as all these models provide good repeatability.

For a researcher working on a real ESD problem, only the data about ESD sensitivity does not help to solve the problem. The real ESD event may be dependent on the rise time of the ESD event, on its length, on device design, fabrication technology, device package etc. The researcher needs more information but only ESD sensitivity to establish the actual mechanism of breakdown, and in final to be able to prevent the ESD induced breakdown. A testing system that can provide some more information about the be-

haviour of a tested device under ESD stress is Transmission Line Model (TLM) system, where ESD stress is produced by a charged transmission line, and which will be used for ESD experiments reported in this thesis. It will be explained in detail in Section 2.1.2.

2.1.2 Transmission Line Model testing system

Transmission Line set-up was firstly introduced by Tim Maloney [36]. It was initially developed for ESD research, and it was proved to be a very important tool for the scientific approach to ESD problem, as it allows systematic stressing and also monitoring of device under stress during stressing. The TLM system, was widely used for the studying of the transient behaviour of electrostatic discharge protection devices for the IC circuits as it is well calibrated and easy to use. The parasitics can be kept small and repeatability is enhanced.

The TLM set-up is shown in Fig. 2.1. A 50 Ω coaxial cable (transmission line) is first charged by the high voltage generator up to a known voltage. The amount of charge on the transmission line depends on its length. When the line is discharged (the switch is closed) a short ESD pulse is created (10 nanoseconds per meter of cable). The line is terminated with a 50 Ω resistor to minimise reflections. The voltage and the current can be monitored on the oscilloscope, enabling accurate estimation of the power delivered in the device. A high-impedance transmission line model can be constructed by placing a resistor ($> 450\Omega$) in series with the device under test. This resistor is meant to provide that a voltage stress pulse is transformed into a current stress pulse (as the serial resistance is much higher then the resistance of the device under test). The TLM is a step wise testing procedure. The current stress pulse is stepped up and the voltage on the device under test is measured.

2.1.3 On chip ESD protection strategy

To fully protect electrical circuits from the ESD, protection circuits are added at every input, output and supply pin. The protection circuit has to provide a conductive path to discharge the ESD stress. It has to limit the current and the voltage in the circuit. It also has to stay invisible during the normal operation of the circuit.

This can be achieved using semiconductor devices such diodes and transistors. The elements of the protection circuit must be designed to withstand the high level currents and voltages. A very often used protection

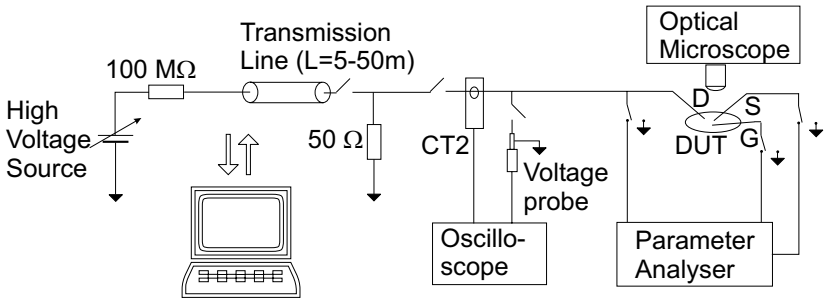

Figure 2.1: Transmission Line Model experimental set-up.

device in silicon technology is the grounded gate NMOS transistor. The gate, source and substrate are grounded and the ESD pulse is applied to the drain with respect to ground. A typical electrical characteristic of an NMOS transistor is shown in Fig. 2.2. At low voltage and current the transistor is off. Under the high voltage on the drain, avalanche multiplication starts at the drain/substrate junction. The generated electrons are flowing towards the positive biased drain and the created holes drift towards the substrate contact. Due to the increased substrate current, a voltage drop is created that makes the source/substrate junction forward biased and electrons are emitted into the substrate, giving rise to an increase in the drain current. The drain voltage needed for this current decreases and a negative resistance region (snapback) is observed due to further carrier multiplication, until a minimum voltage (holding voltage) is reached. At a certain current level, thermal breakdown, or so called second breakdown occurs. Hereafter, the device is catastrophically damaged. It has been proven that during an ESD zap, the NMOS transistor sinks the majority of the current delivered to the pin and holds the voltage at a constant value. During discharge, NMOS transistor operates in the snapback mode. The question arises whether TFT's operate in the snapback regime during an ESD zap and if so, whether it is possible to use the snapback regime for designing ESD protections in TFT circuits.

2.2 TLM Experiments on grounded gate α-Si:H TFT's

In order to study breakdown behaviour under electrical stress the following measurements have been carried out. Unfortunately the the TLM measure-

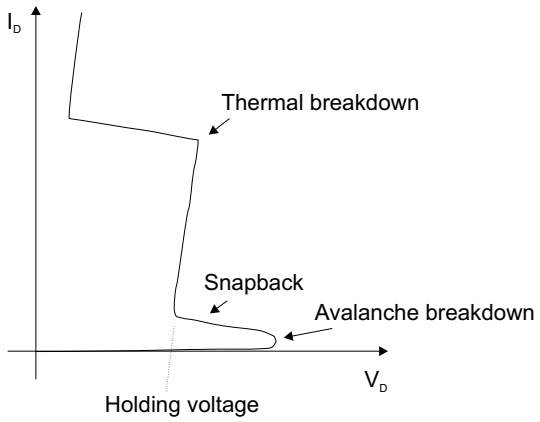

Figure 2.2: IV characteristic of a NMOS emphasising the behaviour of the transistor in the high current regime.

ments can not be performed in the way that is accepted in IC's (it means stressing by a current pulse). The on-resistance of α-Si:H TFT's is much higher then of crystaline MOS transistors. The value of the on-resistance varies, but it is in order of M Ω. As a consequence of this high on-resistance the stress current is very low. Even the current under high ESD stress of few hundreds of Volts is so low that it can not be measured by the current transformer of the oscilloscope (sensitivity of which is 5 mA). Only the peak of the drain current can be measured. Also, the drain current during the breakdown can be read out. That is shown in Fig. 2.3. It also should be noted that the gate and the source current during the breakdown are not known, so the path of the breakdown current can not be established by this measurement. The voltage data on the drain could be easily measured by the oscilloscope. Therefore the standard TLM measurement system had to be changed in order to compensate for the loss of data (current measurements) in the following way. Between each two TLM stress pulses, the transfer characteristic $I_D(V_G)$ of the TFT was monitored by the Parameter analyser (Fig. 2.1). From the transfer characteristics important electrical parameters like threshold voltage, subthreshold slope were extracted. From the behaviour of the transfer characteristic the degradation flow was estimated. Another important parameter that was measured by the Transmission Line model is the breakdown voltage. The measurement of the TLM voltage showed that TFT's give different response to the TLM stress then crystalline MOS devices. The TLM voltage was increased up to the catas-

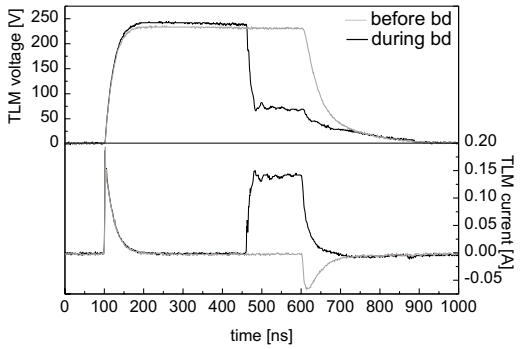

Figure 2.3: Shape of current and voltage TLM pulses monitored on the oscilloscope before and during breakdown.

trophic breakdown and it did not go into snapback. After the breakdown the TFT's were already thermally damaged (this point is equivalent to the second breakdown when reading a typical TLM curve for crystalline MOS devices).

In this chapter experiments with stressing the grounded gate α-Si:H TFT's on the drain are presented. This structure is chosen as it is known as one of the most popular ESD protection devices in IC technology. Our intention is to check if the same structure can be used in ESD protection of TFT circuits. In the experiments, the TLM voltage pulse generator was typically set up with a pulse width of 100 ns, 300 ns, 500 ns and 1000 ns. These are pulse durations that in comparison with the typical pulse length used in standard ESD investigations on IC's must look rather long. The reason for choosing such long pulses is that in the case of α-Si:H TFT's the RC time of the device is rather long (< 100 ns), as shown in Fig. 2.3, due to the large resistivity of amorphous silicon. Therefore short pulse measurements would not always give complete results. The reason for choosing to experiment with different pulse durations is to investigate whether power dissipation given by $P(t) = i(t)v(t)$ is a parameter in breakdown or it is only stress voltage level. A number of experiments repeated for different pulse widths are investigated in [21].

2.2.1 Breakdown voltage due to TLM

The breakdown voltage under TLM pulse (V_{BR}) is defined as the voltage at which the drain current increases sharply and accompanied with a decrease

in the drain voltage. In Fig. 2.4 some typical TLM curves are shown measured for TFT's with different dimensions.

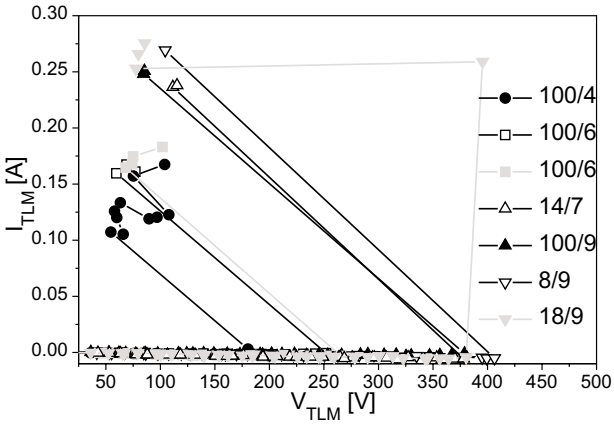

Figure 2.4: TLM curves shows different breakdown voltages for TFT's with different dimensions.

The results presented in this section are concerning two important subject related to TLM stress induced breakdown:

- breakdown voltage vs. channel width and channel length
- breakdown voltage vs. pulse length.

An overview of the TFT's with a variety of the channel length and width tested by the TLM measurement system is given in Table 2.1. From the data shown in Table 2.1 it can be quickly concluded that breakdown voltage depends on the channel length and does not depend on the channel width (from the fact that the TFT's with the constant channel length $L = 9\mu m$ and with different channel widths did not show noticeable variations of the breakdown voltage). The dependence of the breakdown voltage versus the channel length , which is extracted from the data shown in Table 2.1, is separately plotted in Fig. 2.5. Fig. 2.5 shows that breakdown voltage depends almost linearly on the channel length for the short channel TFT's ($L < 10\mu m$). For long channel TFT's ($L \geq 10\mu m$) the breakdown voltage stays constant with an approximate value of $Vbr = 425V$.

Beside the breakdown voltage measurements in the sample consisting of the TFT's with W and L variations, an other experiment is carried out in order to get a better insight in the breakdown physics. The breakdown voltage

Table 2.1: Breakdown voltages under TLM stress in a sample with variations of W and L.

W/L	sample A1	sample B1	sample C1	mean value
100/10	420	450	410	427
100/100	430	440	400	423
8/9	430	430	400	420
4/9	430	430	400	420
10/9	420	420	400	413
18/9	410	410	400	407
6/9	420	420	390	410
100/9	410	400	370	393
100/8	370	370	320	353
14/7	350	330	300	327
100/6	280	280	260	277
10/5	260	240	230	243
100/4	210	190	190	197

was measured for different duration of the TLM stress pulse. Differences in breakdown voltage due to difference in channel lengths/batches, mask possible difference in breakdown voltages due to difference pulse lengths. Therefore for the following experiments only TFT's were used with constant W/L ratio (18/9). In Table 2.2 the breakdown voltages of tested TFT's are listed. These TFT's were stressed with TLM pulses with pulse lengths of 100 ns, 300 ns, 500 ns and 1 μs. It should be noted that the large ($\sim 100ns$) rise/fall time of the TFT has to be taken into account.

The data from Table 2.2 are graphically presented in Fig. 2.6. The experimental data show that the breakdown voltage lowers when the TLM stress time increases. Unfortunately the number of data points in the Fig. 2.6 is not enough for a reliable extrapolation.

The conclusion that we can draw from the experiments is that the breakdown voltage apparently depends on the channel length and does not on the channel width. In the TFT's with the channel length $L < 10\mu m$, so called short-channel effects, similar as in the standard crystalline devices, occurs and the breakdown voltage is considerably lower. The current flow is dependant on the W/L ratio, but also on the channel length itself, due to

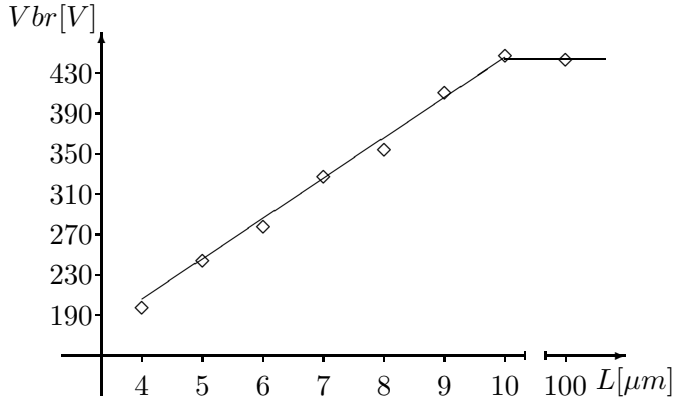

Figure 2.5: The mean value of the breakdown voltage versus the channel length.

punch through effect, which will be discussed later on. It is also shown that the breakdown voltage depends on the stress time. As the stress time is increased, the breakdown voltage is decreased. These results suggests that electrical breakdown is in the end a thermal process. The heat generation is due to the current flow and it depends on the thermal properties of the materials used, amorphous silicon, Si_xN_y and glass. The time dependence suggests also that a high power dissipation develops (Wunsch and Bell model [15]).

Table 2.2: Breakdown voltages of the TFT's with W/L=18/9 tested by the TLM with different pulse lengths.

	100ns	300ns	500ns	$1\mu s$
sample T1	430	420	400	380
sample T2	430	430	400	380
sample T3	470	x	380	360
sample T4	470	x	370	360
sample T5	x	x	380	360
mean value	450	425	386	368

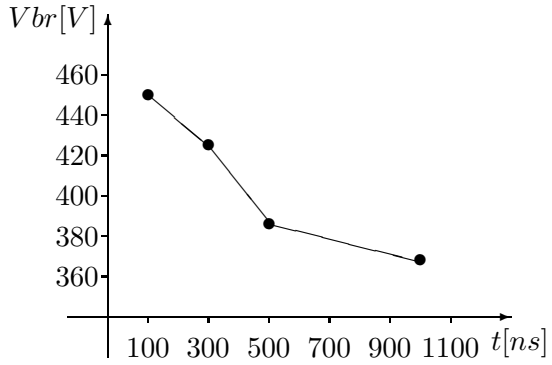

Figure 2.6: The mean value of the breakdown voltage versus the TLM stress time.

2.2.2 Pre-breakdown degradation due to TLM

If a TLM stress is higher than the "threshold of degradation" ($V_{THDEG} \sim$ 180 V), the transfer characteristic, monitored between two TLM stress pulses, starts to change. The transfer characteristic shifts to the negative side and the slope of the characteristic increases. A set of $I_D(V_G)$ curves monitored in this way is shown in Fig. 2.7. The drain current behaviour un-

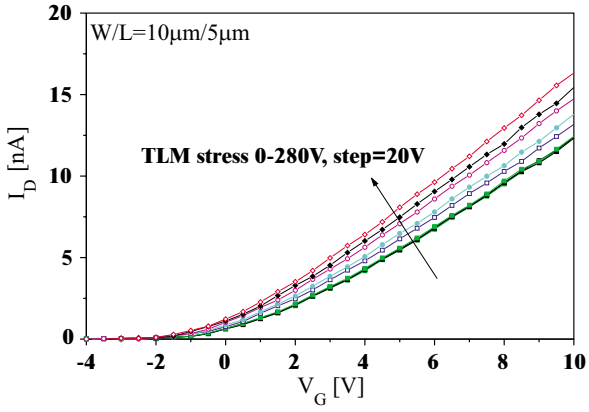

Figure 2.7: Transfer characteristics monitored during the TLM series.

der applied gate voltage is already explained in Chapter 1, by equations 1.2, 1.3 and 1.4. In literature, two mechanisms have been found to contribute to degradation effects in α-Si:H TFT's:trapping of charge in the gate dielectric

and change in the density of states (DOS) of the amorphous silicon itself. Which of this two set in during ESD stress will be investigated further in this section. It is clear that change in the drain current might be due to

- the change in the threshold voltage, which can be due to the charge accumulation in the dielectric or at the interface dielectric/amorphous silicon
- due to the change in the electron mobility. The electron mobility μ_n is thermally activated with an energy given by the width of the tail states, not by $E_C - E_F$ [43].

$$\mu_n = \mu_0 N_c \frac{kT}{n} e^{-\frac{E_a}{T}} \tag{2.1}$$

  where μ_0 is the extended state electron mobility, N_C is the density of states at the mobility edge, n is the total electron density and E_a is the activation energy which reflects the tail state distribution of the α-Si:H. Therefore the electron mobility might change if the temperature of the TFT is changed.

The presence of the interface states can be read from the subthreshold slope. The sub-threshold slope is defined by:

$$S = \frac{dV_G}{d(logI_D)} \tag{2.2}$$

The change in the subthreshold slope will help us to distinguish whether the charges that are able to change threshold voltage are located in the gate dielectric (which produce no change in the subthreshold slope) or at the gate dielectric/amorphous silicon interface which will produce change in the subthreshold slope).

The threshold voltage (V_T) is derived from the intersection of the slope of linear characteristic with x-axis. It is found that once the TLM voltage exceeds the threshold of degradation, V_T decreases linearly with applied voltage. The peak decrease in the threshold voltage is just before breakdown. The breakdown voltage and TLM stress that a TFT can stand depends on the channel dimensions, as explained in 2.2.1. On the other hand, if the same amount of TLM stress is applied to TFT's with different channel dimensions, the threshold voltage shift shows the same dependence with the channel dimensions like the breakdown voltage. An overview of the V_T shift for TLM stress of 500 ns and transistors with different channel dimensions is shown in Fig. 2.8 [70]. Appearance of the negative shift of V_T can be

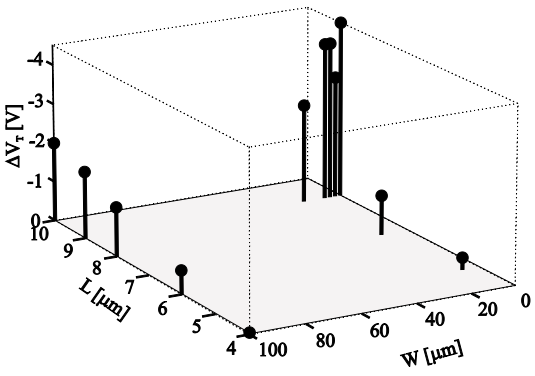

Figure 2.8: Threshold voltage shift after TLM series (from 20 V up to 250 V) as function of W, L.

connected with both mechanisms, the creation of states in the amorphous silicon layer, or near the interface and due to the charge trapping in the gate dielectric. For example, an amount of positive interface would cause an accumulation of electrons in the channel, which would result in a lowering of the threshold voltage.

Besides V_T, the transconductance is also derived from the slope of the linear transfer characteristics. An increase of electron mobility is assumed and will be further explained by the analysis that follows. In α-Si TFT's, the main carriers are electrons whose room-temperature mobility is typically $0.3 - 0.6 cm/Vs$. The dependence of the mobility with temperature is given by equation 2.1. We suppose that a shift of V_T and shift of μ are independent processes, although they can be correlated, as shift in μ will almost certainly shift V_T. We assume positive interface charges, which would help to move the current flow closer to interface α-Si/SiN and further from the bottom interface of α-Si/SiO_2, where it is more confined in higher mobility part of the band-gap. The fixed charge present in the gate dielectric causes bend bending at zero bias. Thus the DOS will be spatially inhomogeneous (in the direction of the channel depth) and determined by the surface charge layer induced in the α-Si:H by the fixed charge in the gate insulator. There is also another possible mechanism which can help to explain the change in the transfer characteristic's slope, assuming that interface charges are inhomogeneous in the direction of the channel length. The assumption is that an amount of positive interface charges is created close to the drain. These positive charges would attract an accumulation

layer (N^+) that extends the drain, resulting in a shortening of the effective length of the transistor [73]. In this case electrom mobility stays constant. To avoid this uncertainty, the slope change will be presented through a relative change of transconductance:

$$g_m = \frac{\delta I_D}{\delta V_G} = \frac{W}{L}\mu C V_{DS} \tag{2.3}$$

Stepped lowering of V_T implies stepped accumulation of positive charges. Irreversibility of this degradation is observed and confirmed by means of repeated TLM experiment under the same conditions. To investigate whether the SD induced degradation is permanent, repeated TLM stresses were applied in the following way. In the first TLM series, TLM stress (V_{TLM}) is stepped from 20 V up to 250 V, when the series is stopped. After 100 min of pause (with all electrodes grounded) the second TLM series is repeated (V_{TLM} =20-250 V). This time both V_T and g_m stay constant during TLM stress. After pause of 1000 min the third TLM series is applied (V_{TLM} was increased from 20 V up to dielectric breakdown). Same as in the previous case, no degradation is found for voltages up to 250 V. Finally, when V_{TLM} >250 V, then degradation of V_T and g_m continues with the same rate (1 V/100 V) as in the first TLM series (Fig. 2.9).

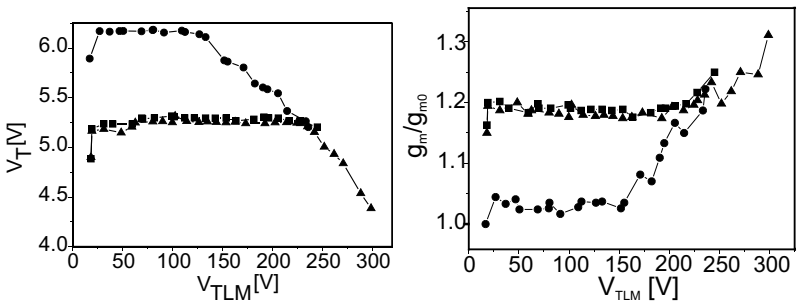

Figure 2.9: Threshold voltage and transconductance behaviour during the first and the repeated TLM series.

It should be noted that after the first TLM stress the "turnaround phenomenon" of the threshold voltage shift is noticed. This phenomena for the low negative gate bias is already known in the literature [62] and it appears when the negative threshold voltage shift caused by the hole trapping in the SiN gate dielectric are positively compensated by the states created near the conduction band in the α-Si film. This process of state creation should be distinguished from the creation of states under high electric field.

In order to distinguish whether these charges are located in the gate dielectric or at the gate dielectric/amorphous silicon interface, the sub-threshold slope of the transfer characteristics is analysed. It appears that sub-threshold slope increases during TLM stressing, which can be the result of interface state creation. Assuming that created defects in amorphous silicon are located at the gate dielectric/amorphous silicon interface, the effective defect density D_{it} can be related to the sub-threshold slope [9] as:

$$S = ln10\frac{kT}{q}\left(1 + \frac{q^2 D_{it}}{C_i}\right) \tag{2.4}$$

where q is the electron charge, k is the Boltzmann constant, C_i is gate capacitance per unit area and T is absolute temperature. The calculated values of the density of interface states vary between TFT's. For example, after a TLM series up to 250 V they are estimated to be in the order of $10^{12} cm^{-2} eV^{-1}$. The behaviour of the subthreshold slope under TLM stress is shown in Fig. 2.10.

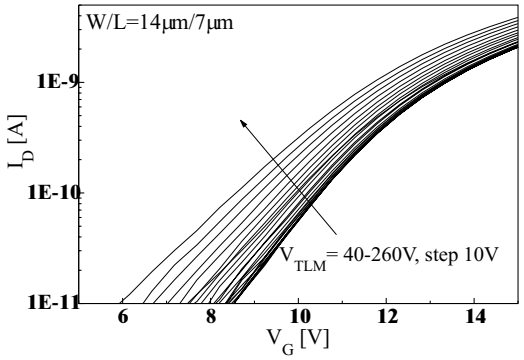

Figure 2.10: Subthreshold slope change during TLM.

2.2.3 Where are the defects?

The sub-threshold slope increase during TLM stressing implies defect state creation. In order to determine where these defect states are located within volume of a TFT a repeated symmetrical experiment is performed as follows. After the first TLM series (V_{TLM}=50-250 V, step=10 V) is applied on the source of the TFT, the second TLM series is applied on TFT's drain. In the second TLM series the V_T decrease and g_m increase continuously

from the same threshold of degradation voltage, when compared to the first series (Fig. 2.11). Apparently, repetitive TLM stresses on one side of the transistor up to the highest previous level do not create additional damage, whereas an additional TLM series with the same low voltage on the other terminal does create additional damage. It means that if TLM stress is applied on the drain, the defect states are non-equally distributed along the channel. They are located close to the drain of TFT.

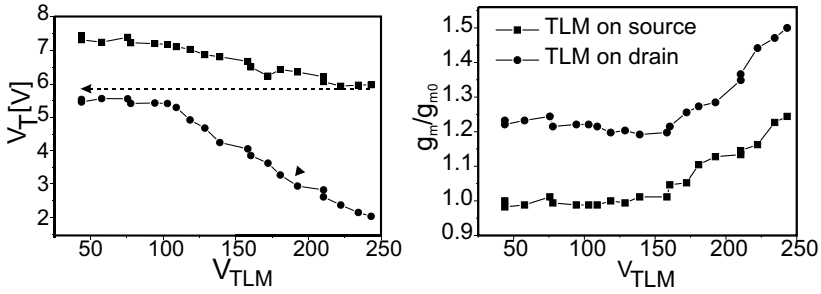

Figure 2.11: Threshold voltage and transconductance variation under two repeated symmetrical TLM series (first series on the source, second on the drain).

2.2.4 CV measurements showing interface states creation

An additional proof that TLM stress induces creation of fast interface states is obtained from high frequency C(V) measurements [23]. Parasitic capacitances of the drain and the source are measured before and after a TLM series up to $200V$ applied on drain. The position of the Fermi level in an undoped α-Si, as used in this investigation, is shifted closer to the bottom of the conduction band. Therefore, tested TFT's are undoped and n-type (Fig. 2.1cv). It should be noted that during the TLM testing the TFT's threshold voltage is decreased by 0.5 V, and the transconductance is slightly increased. As it is shown in Fig. 2.12, the high frequency $C(V)$ curves of the parasitic capacitance of the source before and after TLM stress are the same, meaning that TLM stress did not induce any damage at the source side. In contrast, the high frequency $C(V)$ curve of the parasitic capacitance at the drain side (Fig. 2.12) after TLM stress is stretched-out to the negative side and degraded as compared with the curve monitored before the TLM stress.

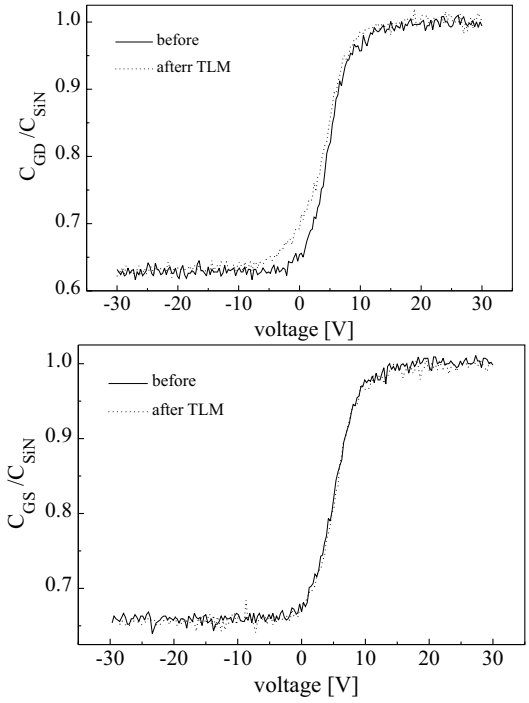

Figure 2.12: Normalised high frequency capacitance vs voltage curves measured for the gate/source overlapping and gate/drain overlapping capacitances before and after TLM stress applied on the drain.

2.2.5 Modelling of TLM stress induced degradation

Firstly, the gradually distributed electric field across the gate dielectric is simulated using Silvaco device simulator [14] for the TFT in gg mode. The simulation shows that if the threshold voltage of degradation is applied on the drain, the electric field close to drain has value $\sim 5 - 10$ MV/cm. This electric field peak is located close to the drain, but it expands from drain to source during each next TLM stress pulse, since the TLM stress is stepped.

The assumption that a TLM stress creates positive interface charges, giving rise to sub-threshold slope and lowering V_T, is interpreted by means of electrical simulations. The assumed model says that the new created interface charge, induced by the electric field, widens with every step along the interface from the drain to the source (Fig. 2.13). The transfer characteristic of the top gate amorphous silicon transistor is simulated by Silvaco

simulation tools [14], taking into account created interface charge. Initially, the transfer characteristic is simulated without any interface charge. At each simulation step a constant quantum of interface charge is added along the length from drain to source (Fig. 2.13). Charge parameters have been optimised, leading to: length of the cube $x = 0.2\mu m$ and fixed charge density quantum of $10^{12} cm^{-2}$. The result of the simulations is presented in Fig. 2.14. It can be seen that it describes the experimentally measured characteristics, shown in Fig. 2.7. This is the effect of the positive inter-

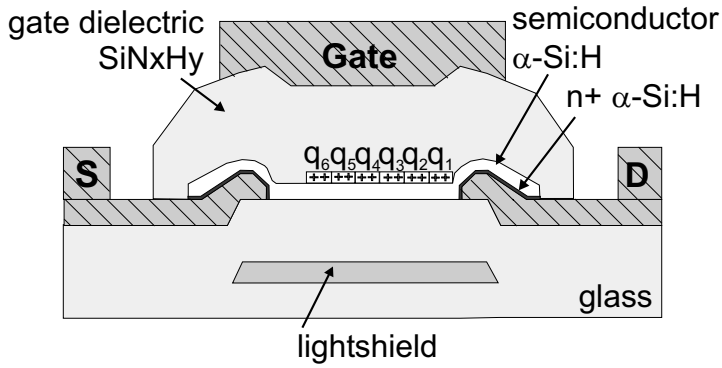

Figure 2.13: Model of stepped accumulation of the interface charges from q1 until q6.

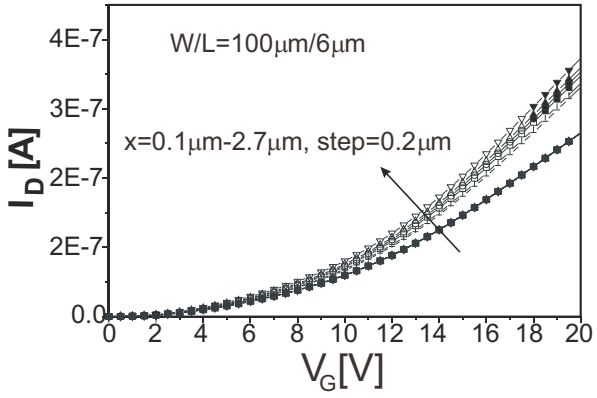

Figure 2.14: Simulated transfer characteristics with increasing interface charge as depicted in Fig. 2.13.

face charges, which help creating an inversion layer "extending" the drain. If we assume negative charges in the channel (α-Si:H), the effect will be the same. Negative states in the band gap of amorphous silicon are the states in the upper part of the band gap, donor-like states. Conduction band-tail states are neutral when empty and negative when filled [12].

2.2.6 Thermal annealing of degradation

In order to remove created interface traps, TFT's are thermally annealed. The procedure of annealing for both variations that will be presented is as follows: first thermal annealing, then the first TLM series (when threshold voltage and transconductance were monitored), a second thermal annealing (with repeated conditions of first annealing), the second TLM series (V_T and g_m monitored). Two variations of annealing are carried out: dry annealing in vacuum, and wet annealing in an N_2/H_2 ambient. Hydrogen was chosen as it has an important role in closing the dangling bonds in the amorphous silicon.

Dry annealing

After initial annealing and the first TLM series, the TFT is annealed at 200^oC for 1 hour in vacuum, with all electrodes open. Analysing the behaviour of V_T and g_m under second TLM series, it can be seen that they are not constant under TLM stress. It means that the annealing is sufficient to de-trap, at least partly, the created traps. During the second TLM series after thermal annealing, transconductance is completely recovered. It returns to the starting value, and behaves similarly (same threshold of degradation and rate) as during the first TLM series (Fig. 2.15). It proves that created interface states, responsible for increasing of the transconductance, are removed by thermal annealing at the $200\ ^oC$. The threshold voltage value did not recover to the starting value (Fig. 2.15). This leads to the conclusion that processes of change in transconductance and threshold voltage have different activation energies. The process of recovering of transconductance has a lower activation energy than the process of recovering of the threshold voltage. A possible explanation is that heat treatment removes only created fast states from the interface, but that the energy/time is not enough to remove deep states in the gate dielectric.

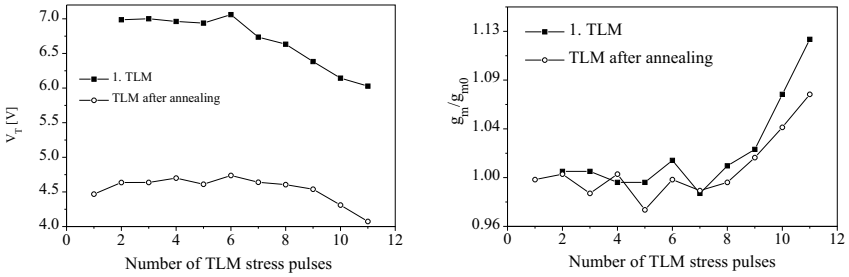

Figure 2.15: Effects of dry thermal annealing on threshold voltage and transconductance.

Wet annealing

A completely different result is obtained by wet open-circuit thermal annealing in the atmosphere of N_2 with the presence of H_2 at 250 ^oC for 30 min. The results are shown in Fig. 2.16. As shown in Fig. 2.16, the threshold voltage after thermal annealing is increased (in contrast to the dry annealing), while transconductance is almost completely recovered, although it does not return exactly to the starting value. Both V_T and g_m under the second TLM series are active (changing with increasing the TLM stress), they degrade in the same way as under the first TLM series, which implies that created states are removed from the α-Si:H/SiN interface. The difference in V_T shift during wet and dry annealing comes from the presence of hydrogen. Annealing without the presence of hydrogen gives negative, while annealing in the presence of hydrogen gives positive shift, as hydrogen plays important role in the process of de-trapping holes.

2.3 Long time experiments

A square voltage pulse in the range of seconds is applied to the drain of a TFT using a parameter analyser HP4142B and a voltage generator expander. The stress pulses are increased in voltage up to 200 V, the highest voltage that can be generated by the parameter analyser equipped with a voltage expander. During each stress pulse the drain current is measured and after each stress pulse the transfer characteristics are measured, both with the same parameter analyser.

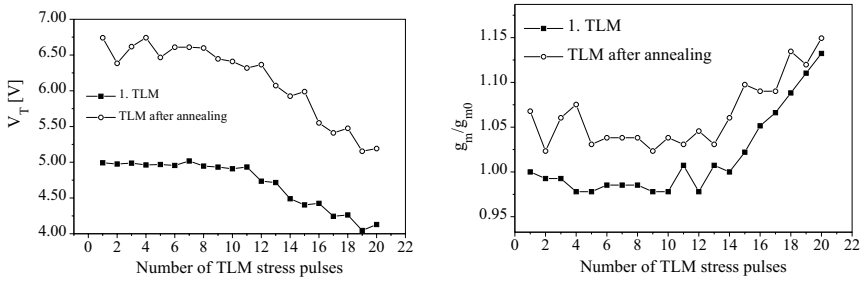

Figure 2.16: Effects of wet thermal annealing on threshold voltage and transconductance.

2.3.1 Current during stress

Both, the voltage and the current during stressing were measured. As the voltage during stress is given by the voltage generator, the voltage is constant. The information of the current during stress is important, bearing in mind that that information was lost during TLM measurements. The current during stress measured on both the drain and the source of the TFT with $W/L = 18/9$ is shown in Fig. 2.17 for stress voltage on the drain V_D=200 V, with the source and the gate grounded. It can be concluded from the plot that the current during stress is drain to source current, as two curves shown in Fig. 2.17 overlap, except for the first point. It should be noted that the drain current during stress is in the beginning (low drain voltages) only a subthreshold (leakage) current, as the gate is grounded. Expected level of the leakage current is in the order of several pico amps. After the drain stress voltage is increased, the real conduction current (order of μA) sets in. Due to the high voltage applied on the drain, the DIBL effect is initiated, as it will be explained further in section 2.5.

Another important remark about the drain current during stress is that although the drain current level measured with each stepped voltage stress increases, during a stress pulse the current shows an exponential decay (Fig. 2.17). This decay is due to the process of creation/removal states across the amorphous silicon layer. This process is confirmed from the measured transfer characteristic after stress, as it will be explained later in this section. The current during stressing reflects the creation/removal of states at the interface, but also in the bulk of α-Si (reaching final steady state situation in this process takes some time - if it is reached at all [47]?).

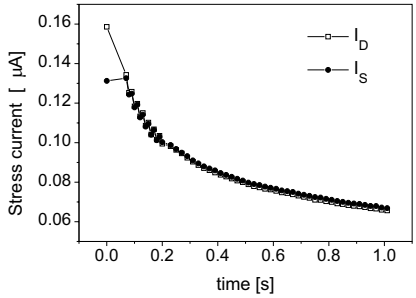

Figure 2.17: Current during Long pulse stress measured on the drain and the source (the source current is actually measured with the negative sign, plotted as positive for convenience.

2.3.2 Breakdown voltage due to Long pulse

Due to the limitations of the measurement set-up (stress voltage only up to 200 V), the breakdown voltage under long pulse stress could be measured only for the TFT's that have a breakdown voltage lower than 200 V. Therefore the breakdown voltage measurements were limited on the short channel TFT's. Two TFT's were measured: $W/L = 100/6$ and $W/L = 100/4$. For these TFT's the breakdown voltages of 150 V and 110 V are measured, respectively, under the stepped stress of 1 s. Also TFT with $W/L = 18/9$ was tested, but it did not breakdown up to 200 V stress of 1s. The current measured on the drain one step before and during the breakdown is shown in Fig. 2.18.

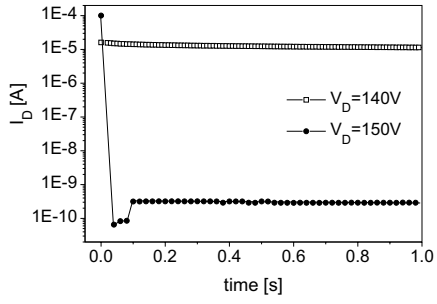

Figure 2.18: Pre-breakdown and breakdown current during Long pulse stress.

2.3.3 Pre-breakdown degradation due to Long pulse

Pre-breakdown degradation is monitored in the same way as it was under the TLM stress. From the measured transfer characteristics, values of threshold voltage, subthreshold slope and transconductance are extracted. All these parameters show the similar behaviour as under the TLM stress.

Threshold voltage , sub-threshold slope and transconductance shows similar behaviour as under TLM stress. Therefore the experimental results will not be discussed in details, but only in general. An overview of the pre-breakdown degradation measured on the TFT with $W/L = 18/9$ under Long pulse stress of different lengths is given in Table 2.3. There

Table 2.3: Pre-breakdown degradation of the TFT's with W/L=18/9 tested by the Long pulse with different pulse lengths.

Stress [V]	$0 \div 50$	$50 \div 125$	$125 \div 200$
V_T	↗/0	↘	↘↘
g_m	0	↗	↘↘
S	0/↘	0/↘	↗↗

are three distinguished regions in the behaviour of monitored parameters. While stress voltage is low (V_D <50 V) there is a slight increase in the V_T followed with also very small decrease of S. This is initial change that is known in the literature and it is called the turnaround phenomena and it was already mentioned in section 2.2.2. After the stress voltage is increased further (50< V_D <125 V), an other region could be recognised when threshold voltage decreases moderately ($\Delta V_T < 1$ V), the transconductance increases and the subthreshold slope stays same as in the previous region. In this region there is no significant creation/removal of interface states and the process of charge trapping in the gate dielectric dominates. After the stress voltage is higher then 125 V, V_T degrades severely ($\Delta V_T \sim 3V$), while g_m decreases severely and S increases sharply. In this region creation/removal of interface states in the amorphous silicon layer dominates in the process of degradation.

2.4 Time-voltage trade-off

In this section the time-voltage trade-off is presented in order to give an in-depth analysis of the ESD effects in α-Si:H TFT's. The data presented

in this section are actually drawn from the experimental results shown previously in section 2.2 and section 2.3.

2.4.1 Breakdown voltage over time

The question we want to have an answer to is whether the breakdown depends on the stress time or it is only related to the stress level. That is important information to determine the mechanism of breakdown. The dependence of the power of the square pulse and the time to failure is due to the energy consumed at TFT, as explained by the Wunsch and Bell model [74], [15]:

$$E = \int_0^t I(t)V(t)dt \tag{2.5}$$

It is an early model of thermal breakdown in Si devices. In this model the pulse power and time to failure are related by $P \sim t^{1/2}$. This model covers only the middle part (typically for Si that is in the region 10 ns$< t <$ $100\mu s$) of the $P(t)$ curve. For very short failure time ($t < 10ns$), the little heat is developed so that the process is adiabatic $P \sim t^{-1}$. For very large failure times, typically above $100\mu s$ and after thermal equilibrium has been established, the constant or steady state term dominates.

Unfortunately, there are not enough (accurate) breakdown voltages measured for different pulse lengths using TFT's with the same W/L. The data measured under TLM stress are shown in Fig. 2.6, and the same TFT ($W/L = 18/9$) could not be measured by Long pulse stress. Only the small number of data for TFT's $W/L = 100/6$ and $W/L = 100/4$ are available. In these two TFT's the breakdown voltage change from $240V$ under TLM stress to $150V$ under Long pulse stress and from $180V$ to $110V$, respectively. Still, from this limited data source it is possible to draw the conclusion that breakdown voltage depends on the pulse duration, e.g. it lowers if the pulse length of applied stepped voltage stress increases, but a unique function of this dependence is not known. Though the current in TFT under square voltage pulse proves not to be constant in time (it exponentially decreases with time), we could assume from equation 2.5 that V_{BR} lowers if the pulse length of applied stepped voltage stress increases. This conclusion implies that the breakdown due to ESD stress in TFT's is a thermal breakdown. The power-density-dependant failure of amorphous silicon TFT was previously investigated in [61] in the range 1-10 ms. From the power of the square stress, knowing the volume of the melted area, the melting point of the breakdown can be calculated. That will be mentioned later in section 2.6.

2.4.2 Pre-breakdown damage threshold over time

The pre-breakdown degradation dependency on time is explained through the damage threshold. The damage threshold, a stress voltage above which pre-breakdown degradation sets in, was extracted as a voltage for which threshold voltage V_T starts to decrease. Measurements of the damage threshold shown in Fig. 2.19 involve both TLM and Long pulse measurements. The data are collected from section 2.2.2 and section 2.3.3. The extrapolated function of the threshold of degradation over stress pulse length is shown in Fig. 2.19. The measured data are approximately described (as

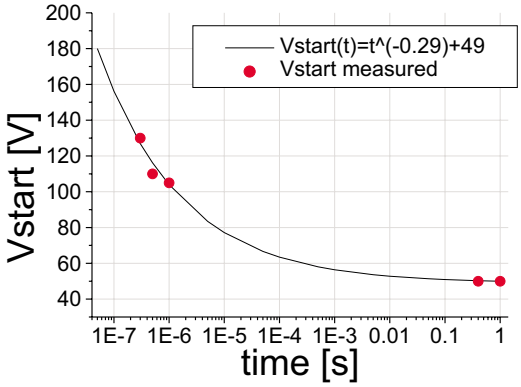

Figure 2.19: The time dependence of the degradation presented with points (measurements) and line (descriptive power law curve).

the number of data is low for a reliable fitting) by an analytical function, which is based on the formula that describes time dependence of the threshold voltage V_T shift at voltages where states creation dominates, described by a power law, $\Delta V_T = at^{\beta}$, with β about 0.3 to 0.5 [45]. It concurs very well with the measurements, which supports our earlier statement that the secondary degradation of the threshold voltage is due to state creation.

It is also important to note that there are two regions in the dependence between the damage threshold and time. In the first region the damage threshold decreases with time. In the later part of the curve ($t > 100\mu s$) the equilibrium process is established, the temperature in the system becomes constant and the further increase in stress time does not speed up degradation process anymore. It is related with the self-heating of the TFT,

as the states creation is a thermal process. Self-heating will be analysed in the Chapter 3.

2.5 Device simulations

2.5.1 Theoretical introduction

The breakdown of amorphous silicon devices was earlier investigated in diodes [5], or in an antifuse structure [1], where an evidence was found of impact ionisation in a-Si. In the thin film transistors itself a huge amount of work and research was focused on metastable effects in amorphous silicon, but very little was published on the subject on electrical breakdown. The items that have to be clarified about electrical breakdown in α-Si:H TFT's are:

- is there punch-through?
- is there impact ionisation and avalanche breakdown?
- is there snapback?

Before the results of simulations regarding these questions will be shown, a few basic definitions will be introduced. The punch-through effect occurs when the neutral substrate width is reduced to zero at a sufficient drain voltage and the source depletion region is in direct contact with the drain depletion region. At this point, the source is effectively short circuited to the drain, and a large current can flow. What actually happens is that under high drain bias the channel depletion width is no longer constant along the length of the device, but varies from the source to the drain. This effect is called Drain Induced Barrier Lowering (DIBL) Effect and it occurs when higher drain voltage is applied to the device. It is very well known in MOS devices [3]. The surface potential (band bending) along the channel between source and drain for long channel devices is normally constant. In short devices, or in long devices under very high drain biasing, it happens that the peak of the surface potential is reduced and is constant only over a small part of the channel, if at all. Since the peak surface potential is reduced, which means that the barrier is lowered, the current will increase.

Avalanche multiplication that may occur by means of impact ionisation is very well explained in standard crystalline Si devices [11]. Electrons/holes gain so much energy in a high electric field that they can generate extra electron-hole pairs by exciting electrons from the valence band into the conduction band. In this way an avalanche of free carriers may arise. Could we

expect an avalanche multiplication due to impact ionisation in amorphous silicon in our TFT's?

It has been already confirmed by the experimental results shown in this chapter that the snapback regime in TFT's is not detectable by ESD testing such as TLM. This stands in opposition with the expectations, as the snapback regime is known in all similar crystalline silicon devices, like NMOS transistors and even n-well resistors [37]. If impact ionisation at the drain/bulk junction due to the high electric field is proved to be present, then the holes concentration inside the n α-Si bulk starts to rise significantly. Then the source/bulk junction should become forward biased and the electrons from the source n^+ region would contribute to the drain current. This process is self-enhancing, as a lower external voltage is needed to maintain impact ionisation. This is seen as a snapback. An interesting issue is to verify the concentration of electrons and holes across the channel length of a TFT under ESD conditions.

2.5.2 Simulation results

The electrical simulations of TFT's are performed by Silvaco process and design simulation software [14]. The effect of DIBL is shown through the simulations of:

- surface potential of an a-Si:H TFT under high drain bias
- surface potential of a long- and a short-channel TFT under the same biasing conditions.

In Fig. 2.20 is shown how the surface potential is distributed along the channel for three different drain biases (V_D=10, 20, 50 V). In all cases the gate voltage was kept constant. It should be noted that the simulated TFT was scaled in lateral direction, which means that channel length and the drain biasing are divided with the factor 10. So the channel length of simulated device was $L = 0.6\mu m$, under drain bias (V_D=1, 2, 5 V). That is done for the simplicity. It slightly influences the accuracy of the simulation results, but does not influence the conclusion extracted from the results at all. This figure shows that by increasing the drain bias, we decrease the barrier. It proves that the DIBL effect is present in α-Si:H TFT devices. It also helps us to understand the results obtained from the experiments. In the experiments the drain was stressed. The gate was grounded, so that the device was not active in the conductive mode. Initially, under very low drain voltage a low leakage current was flowing through the channel.

As the drain voltage was increased, the DIBL effect was more and more pronounced. When the drain voltage is large enough, the real current flows through the device.

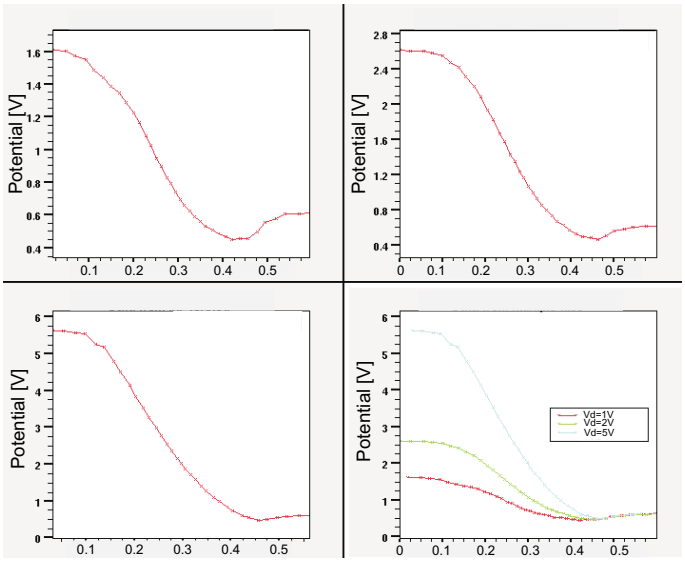

Figure 2.20: An example of DIBL effect in amorphous thin-film transistors simulated for various drain voltages (V_D=10, 20, 50 V).

In another example it is shown that the same effect of barrier lowering can happen if the channel length is varied. Therefore a TFT with two different channel lengths is simulated. The results of these simulations is presented in Fig. 2.21. The simulations show that with shortening of the channel, the barrier between source and drain is lowered. It also agrees with our experimental observations. Namely, it was noticed that both the threshold of degradation and the breakdown voltage depend on the channel length. The shorter TFT's degrade and fail earlier than the longer ones.

The previous simulation results prove the presence of the punch-through in α-Si:H TFT's. It shows that the punch-though occurs when drain voltage is high enough to suppress the barrier in surface potential between source and drain. It happens earlier in shorter devices from the reason that in the short channel devices the barrier is already initially lowered. What we want to know further is if the depletion width at drain extends far enough in real device to have punch-through.

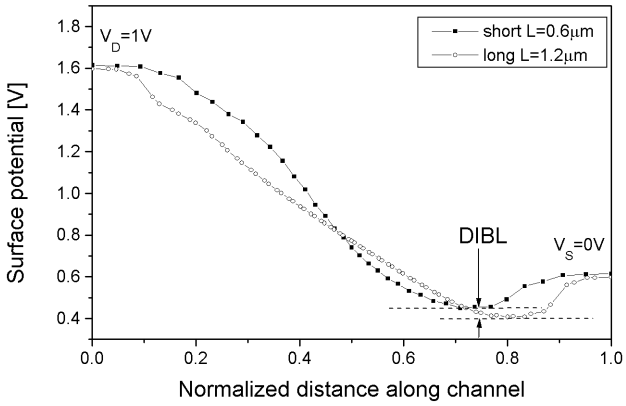

Figure 2.21: Surface potential distribution for TFT's along the channel obtained for examples with different channel lengths.

The question of the impact ionisation and the avalanche breakdown is analysed through the simulation of the recombination/generation rate under stepped drain bias. The results of the simulations performed for a constant gate voltage (V_G=25 V) and different drain biasing are shown in Fig. 2.22. Fig. 2.22 shows (please note that the drain voltage and the channel length are scaled with factor 10) that the peak generation rate is located at the drain, in case when stress is applied to the drain. The generation peak value in the TFT with the channel length $L = 0.6\mu m$ changes from $G = 9{\cdot}10^{10}\frac{1}{scm^3}$ for V_D=1 V to $G = 1{\cdot}10^{21}\frac{1}{scm^3}$ for V_D=10 V and $G = 3{\cdot}10^{25}\frac{1}{scm^3}$ for V_D=20 V. As the results are scaled by factor 10, it allows us to compare this result with the TFT with $L = 6\mu m$ and V_D=10, 100, 200 V, although we must be aware that linear scaling of both voltage and size is not the same as scaling the problem, as depletion layer width goes with $V^{1/2...1/3}$. The experiment shows that the breakdown in the TFT with $L = 6\mu m$ occurring at 280 V could really be initiated by avalanche breakdown at the drain side. In this case we can expect an generation rate $G > 3 \cdot 10^{25}\frac{1}{scm^3}$. This level of generation is enough to start an avalanche breakdown. Simulation results prove that an avalanche breakdown is possible in amorphous silicon TFT's under ESD stress conditions provided similar physical models for ionisation can be used for crystalline and amorphous silicon.

Finally the presence of snapback is examined. A short (L=0.6 μm) ggTFT is stressed by 40 V on the drain. This situation is similar to 400

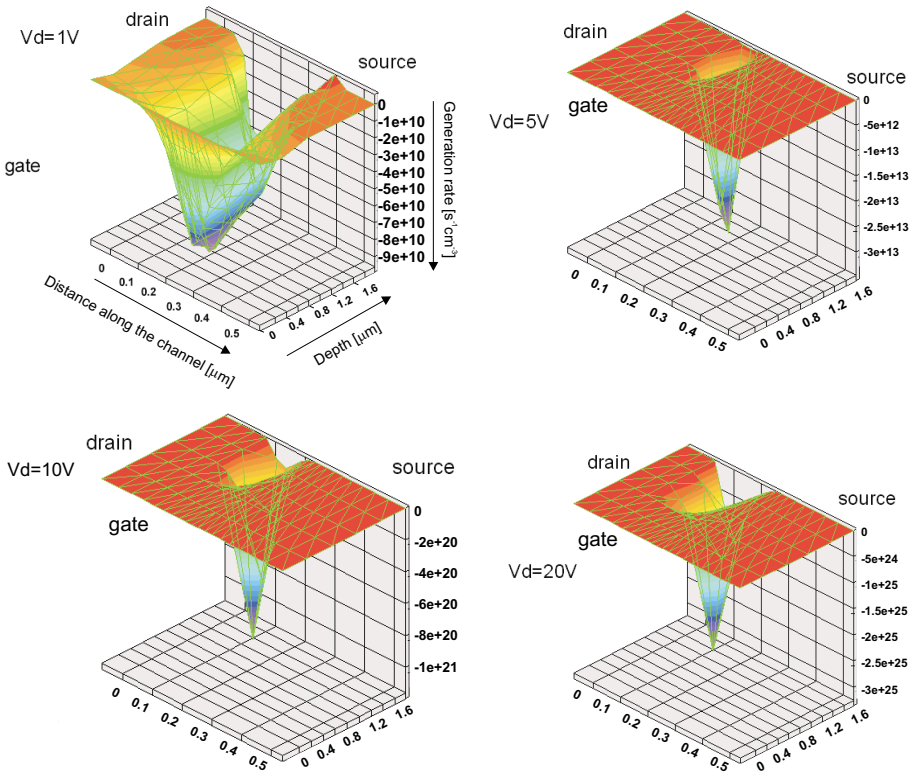

Figure 2.22: Generation rate simulated under constant gate V_G=25 V and varying drain biasing V_D=1, 5, 10, 20 V.

V stress on a TFT with L=6 μm. Simulated structure, recombination and concentration of holes and electrons are shown in Fig. 2.23. The peak of electric field is situated at the drain/bulk junction. This is where the impact ionisation sets in. The generation rate of $G = 9{\cdot}10^{28}\frac{1}{scm^3}$ is simulated at the same location. The holes and electrons flows away from this location towards the source and the drain contact, respectively. The amount of holes in the bulk/ back channel region is increased several orders of magnitude, still its effect is not strong enough to seriously contribute to the output current. It can therefore be concluded that the snapback effect in amorphous silicon is disturbed due to the properties of amorphous silicon.

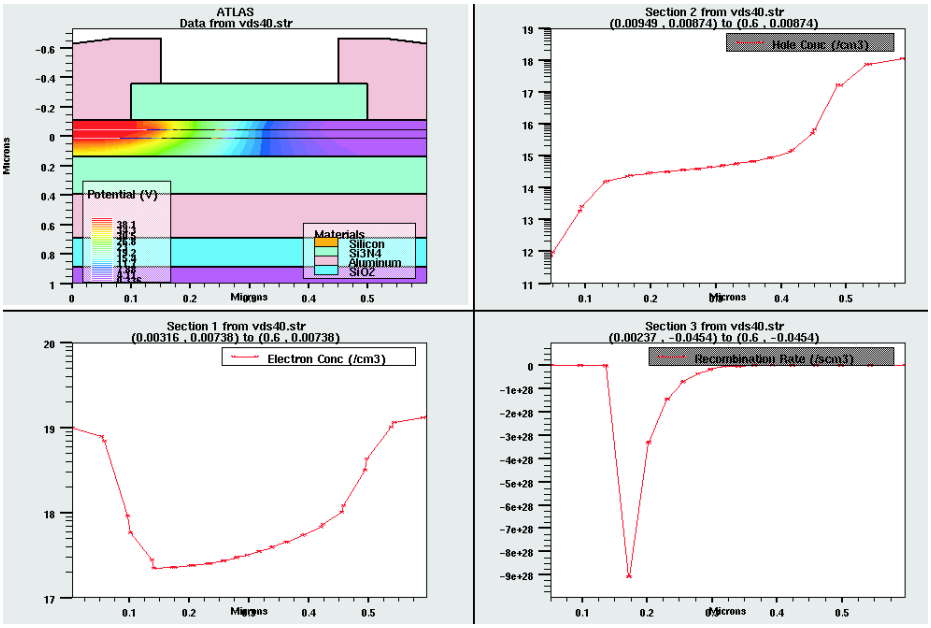

Figure 2.23: Simulated TFT with potential distribution within the α-Si layer, simulated concentration of holes and electrons through the bulk and the recombination through the bulk.

2.6 Post-breakdown observation

Finally, post-breakdown observations have been carried out using optical microscopy and scanning electron microscopy (SEM). The observation confirms the location of the breakdown spot close to the drain in case when the ESD stress is applied to the drain. This further support our conclusion that avalanche creates onset of breakdown in short devices. In long-channel devices, where breakdown voltage is higher then in the short-channel devices, electric field close to drain at the moment of breakdown is very high and very close to the value of the critical electric field for silicon nitride (the value 5-6 MV/cm is found in the literature for the stoichiometric Si_3N_4. The silicon nitride used in TFT's is not stoichiometric and the breakdown field value may vary. Electrical field propagation during a stepped TLM stress is simulated. TLM voltage was applied on the drain (ggTFT). Distribution of the electric field is shown in Fig. 2.24 for the drain voltage V_D=200 V. In this case the peak field (close to the drain) is 7.5 MV/cm. Simulated

TFT has a burried metal layer that shields the amorphous silicon from the backlight. Increasing the TLM stress up to 350 V the field peak is increased up to 10 MV/cm. This could indicate that not only avalanche is cause of breakdown, but under sufficiently high drain voltage that is also the field across the dielectric. Actually, the most often found failure mode is the

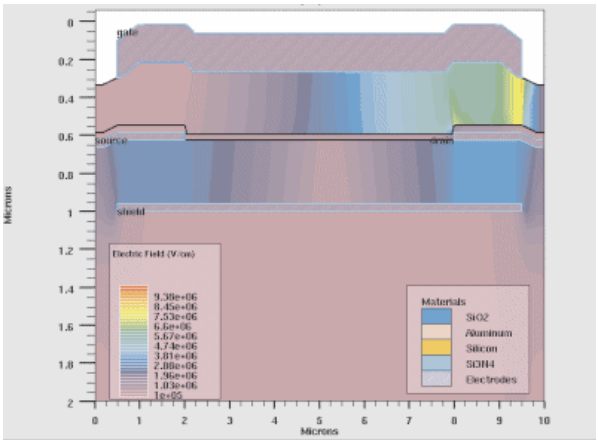

Figure 2.24: Electrical field in the ggTFT with the lightshield under TLM stress (200 V) on the drain.

gate dielectric breakdown . It appears as a rupture localised close to the drain, with a center at the edge between drain and channel. Exceptions are short channel devices, where the rupture completely covers the channel length. In this case, because of the punch-trough, the avalanche generation rate is no longer confined to the drain side. The size of the rupture indicates that the breakdown is a high temperature event. The temperature of the breakdown was calculated on basis of the rupture size, assuming a spherical volume of the whole rupture, and the temperature of over 1400^oC is estimated. The assumption of the spherical volume is made after the ruptures were examined under the microscope. The location of the rupture indicates the position of the highest temperature peak. After inspection of failed devices the assumption is made that the highest peak of the temperature is located at the edge between the drain and the channel, as it is shown in Fig. 2.25. Fig. 2.25 shows example of gate dielectric breakdown in a TFT with $L = 6\mu m$, after etching of the top gate electrode. The size of the breakdown spot is large so that it covers almost the whole channel length. The centre of the breakdown spot is located exactly on the drain/gate edge.

One other failure mode, found in about 10% of all analysed failures, is breakdown of the glass substrate , when the current path is created from drain to source via light-shield. The SEM picture of the de-processed device (gate dielectric removed) discovering this breakdown mode is shown in Fig. 2.26. Current path is created through the glass substrate. A number of melt filaments are found at both drain/gate and source/gate edges.

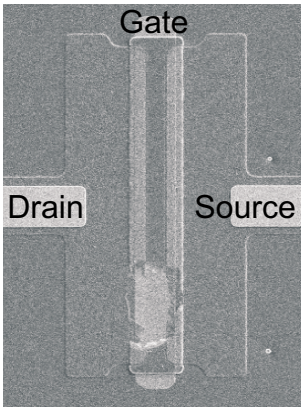

Figure 2.25: SEM photograph showing the breakdown location in the TFT.

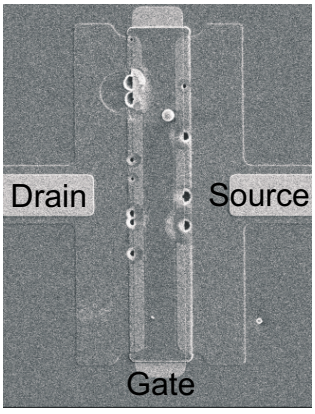

Figure 2.26: SEM photograph showing the breakdown location in the TFT.

2.7 Summary

Experiments were performed on a single grounded gate (gg)TFT to determine TLM failure threshold, in terms of voltage-to-failure profile as the power-to-threshold can not be measured by the TLM system (the TLM current of a single ggTFT is too low). The performance was measured for various values of the channel length and width. A linear relation the breakdown voltage/channel length has been measured. The experiments showed that a degradation of the threshold voltage appears during TLM stress prior to the breakdown. Device level electrical simulations were done to explain the observed degradation mechanisms. The pre-degradation has been related to the created charges localised close to the stressed electrode.

The experiments were continued by using a prolonged ESD stress on a ggTFT, in order to find out the time-voltage relation.

Further, device level electrical simulations have been performed to find out the presence of punch-through and avalanche multiplication. The simulations revealed the presence of the DIBL effect in TFT's, which is more pronounced in the short-channeled TFT's.

Optical failure analysis showed the dielectric breakdown in two modes. The breakdown location is determined; in the long channel devices at the drain, while in the short-channel TFT's it is across the whole channel length.

Chapter 3

Thermal analysis under ESD conditions

This chapter presents the results of a study of the self-heating effects in amorphous silicon thin film transistors. The method of electro-thermal coupled simulations will be explained. The results of two and three-dimensional simulations will be given. The results of the simulations in the static mode will be shown as well as in the transient mode.

3.1 Introduction

Although industrial interest in TFT's in the last years is increased as display industry is developing, this is the first attempt in studying the self-heating effect in amorphous silicon TFT's. Our interest in thermal modelling of TFT's came from our previous experimental study presented in Chapter 2, when a systematical study of electrostatic discharge effects has been done. The devices investigated were top-gate amorphous silicon TFT's with variety of design parameters (channel length and width). Please note that a number of devices is protected by a light-shield (like in Fig. 2.24). Dielectric breakdown, appearing in two variations, is determined by failure analysis. The most often failure mechanism is located in the gate dielectric. In case that breakdown is thermally activated, than it can be assumed that long channel TFT's have lower temperature peak under same biasing, i.e. better temperature dissipation (lower gradient of the temperature across the channel). The applied stress induces, before catastrophic breakdown occurs, degradation of electrical parameters (such as lowering of the threshold

voltage and increasing of the electron mobility), but this degradation is not the direct or only cause of the catastrophic breakdown, as the degradation level is different in different TFT's at the moment of breakdown. The short-channel devices break down early, although their electrical parameters are very little degraded at that point. In other words, different processes lead to dielectric breakdown and degradation. Although it is possible that both of the processes are thermally activated. In analysing sub-threshold slope measured between stress pulses, it is found that creation of positive interface states is responsible for degradation. This result is also validated by means of Silvaco-Atlas device simulations. With the assumption that electrical breakdown is thermally initiated, it becomes interesting to simulate the location of the highest temperature within a TFT. This work on thermal modelling of TFT's uses an approach of two- and three-dimensional circuit simulations. This approach allows that variations of temperature, current and voltages within the transistors active area are calculated.

3.2 Non-isothermal device simulation

This method for simulation of self-heating effects uses an electrical circuit where currents represent heat flow and voltages represent temperatures. The power dissipation of a transistor in the electrical circuit is modelled with a current source in the thermal circuit. Current in the thermal circuit represents the heat dissipation across the device. The principle of this method is shown in Fig. 3.1. The thermal resistance and thermal capaci-

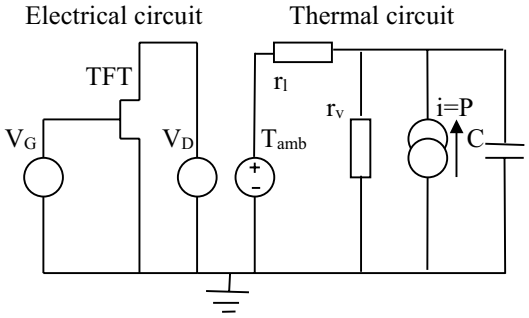

Figure 3.1: Principle of the thermal-electrical circuit simulation method.

tance of the amorphous silicon are modelled in the thermal circuit with an electrical resistor and an electrical capacitor respectively. The thermal circuit is coupled with the electrical circuit by means of the temperature and power dissipation. The voltage at thermal circuit is equivalent of temperature in electrical circuit. The temperature in electrical circuit is involved by change in carrier mobility. The carrier mobility change is approximated by equation [43]:

$$\mu = \mu_0 e^{-\frac{E_a}{kT}} \tag{3.1}$$

where activation energy E_a=0.1 eV, Boltzmann constant $k = 8.6 \cdot 10^{-5}$, T is absolute temperature and μ_0 is chosen so that carrier mobility at $300K$ is $\mu = 0.3\ cm^2$/Vs [13]. The circuit simulator Pstar [40] is used to determine steady state and transient solutions of these coupled circuits. The circuits can be solved in two ways: simultaneously (coupled) and sequentially (uncoupled), as circuit simulator Pstar allows control of electrical mobility by electrical variables. In simultaneous simulations all voltages and temperatures are solved in the same time. In the sequential simulations the electrical circuit is solved first, than the results are used as input parameters for the thermal circuit. The result of thermal simulations is again used as input (temperature) for electrical circuit etc. In this work simultaneous approach is used. Sequential approach is used only during programming process to verify obtained results. The problem with non-isothermal device simulations is that the thermal and the electrical geometric domain are different. The thermally active area is much larger. In three-dimensional simulations it can produce very large number of elements and a long execution time. Often compromise must be made between accuracy of the simulation and computer time, although in this simple TFT's structure should not be a limitation.

3.2.1 TFT modelling using Pstar

Before electrothermal simulations have been performed, it is first checked if a TFT can be simulated with Pstar. The model used in these simulations is Pstar MOS model, level 301, which allows change of transistor's parameters, such as mobility and threshold voltage. To compare simulated characteristics with measured ones, parameters are set at $\mu = 0.3 cm^2$/Vs, V_T=2 V, $L = 100\mu m$ and $W = 1000\mu m$. The simulated characteristic, shown in Fig. 3.2, shows that level of the output drain current is similar to the measured current. It was also checked if carrier mobility behaves according to given equation. It should also be noted that switching characteristics of

crystalline MOS transistors are much better than once of the TFT's, but it is assumed that it would not influence the quality of the simulations, so this model has been accepted.

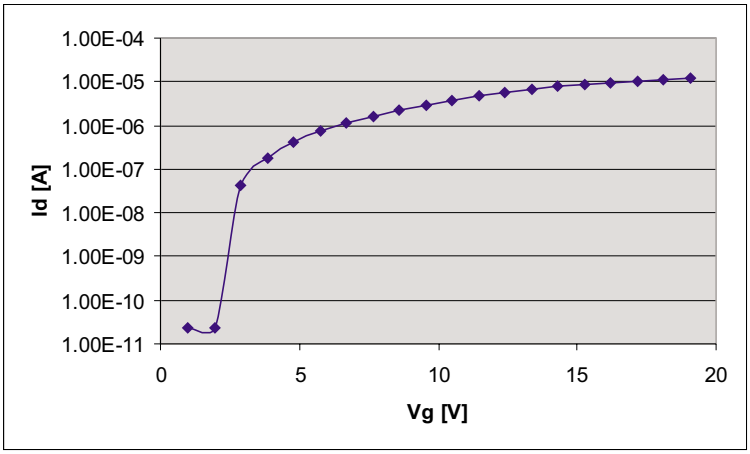

Figure 3.2: Transfer characteristic of TFT simulated by Pstar MOS model.

3.2.2 Electrothermal model

In electro-thermal simulations, current and voltage distributions over a TFT active area are calculated. In that order, the TFT is split up into a number of sections. Depending on the mesh, 2D and 3D simulations are distinguished. In 2D simulations, a TFT is split into number of sections along the TFT's length. In 2D simulations all these sections have the same width, which is equal to the width of TFT itself. In 3D simulations each of these sections is split into number of sections along the TFT's width, allowing calculation of the temperature distribution in both directions of channel length and channel width of the TFT.

In the first stage two-dimensional simulations are performed. Geometrical representation of the simulated structure is shown in Fig. 3.3. The electrically active area of the TFT is split into ten sections (by dashed lines A-K in Fig. 3.3), each with its own current, voltage and temperature. The thermal circuit is created within a thermally active area, which is inevitably larger then the electrically active area, with its own mesh that only coincides with the mesh for electrical circuit in the areas where heat is generated. The electrical circuit of the model is shown in Fig. 3.4. For the electrical

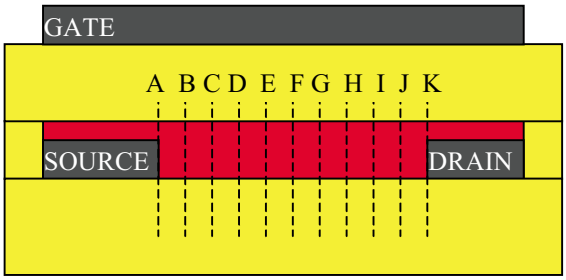

Figure 3.3: Geometrical representation of top gate TFT.

network, a TFT with dimensions $W = 20\mu m$ and $L = 10\mu m$ is modelled with a serial connection of ten TFT's with $W = 20\mu m$ and $L = 1\mu m$.

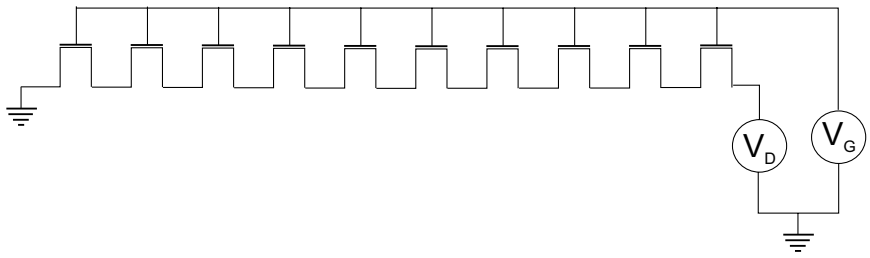

Figure 3.4: 2D electrical model of a TFT.

Before electrothermal simulations started, this concept of modelling of a TFT with serial connection of TFT's had been verified. The same example used in Fig. 3.2 is simulated to compare previous results of simulations of a TFT with the simulation of this model. As shown in Fig. 3.5 (left axis) the simulated output drain current is the same as the current shown in Fig. 3.2. In addition to this model verification, in the same plot it is also shown how the lateral effects are automatically incorporated using this model. Thanks to the fact that voltage on each of TFT's is not equal, current naturally must be equal in the serial connection, then the power dissipation and consequently the temperature are not equally distributed between TFT's in the serial connection. Distribution of voltages at each of

ten TFT's in serial connection (right axis) is shown in Fig. 3.5. Biasing conditions are V_D=10 V, V_G=0-20 V. At the first moment, all drain voltage stays on the last TFT in the row, as the last TFT is at the drain side. As soon as it starts to conduct, the other TFT's start too. After all of TFT's are in the saturation region (V_G >15 V), voltage among them is still non-equally distributed.

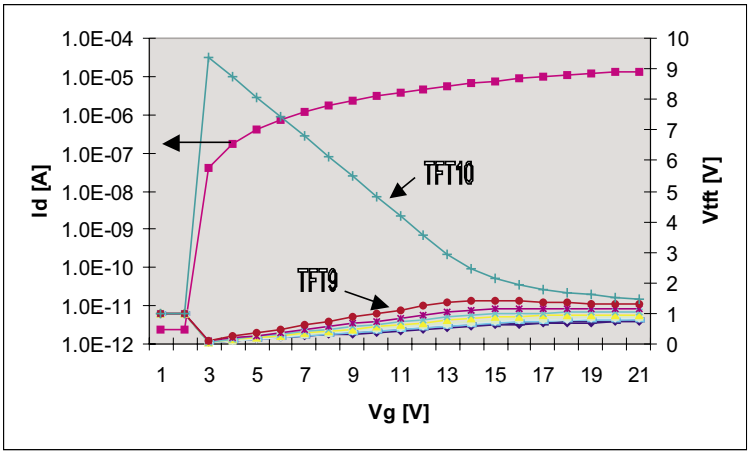

Figure 3.5: Current and voltage distribution among 10 TFT's in serial connection.

As the electrical circuit is verified as satisfying, the thermal circuit is to be built. Although the mesh that is used in this simulation is extremely simple, as it is made manually, the thermal circuit is already more complicated. It comes from the reason that the active area for thermal circuit is larger than the active area for the electrical circuit, as temperature is dissipated into the glass substrate. In this case, only two extra layers surrounding the electrically active area are taken into account. The scheme of the thermal circuit is given in Fig. 3.6. The part of the circuit that is circled represent one section in the electrically active area of TFT. Thermal resistances are coloured in different shades of gray in order to distinguish their different meanings. Resistances at the top central part represent thermal behaviour in electrically active area (white). They are surrounded by a number of lateral resistances that represent the junction between amorphous Si and glass (dark gray). The rest of the circuit belongs to the glass area (light gray). It should be noted that temperature is taken into account only in the bottom part of the device (amorphous silicon layer and under it) and thermal

dissipation through nitride and metal connections has been neglected.

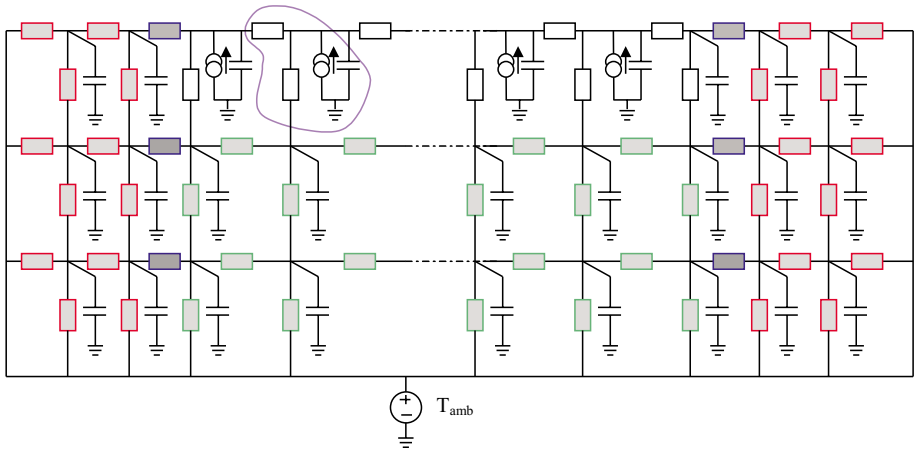

Figure 3.6: Thermal circuit used in 2D simulations.

For each of the circuit elements used in the thermal network a model has to be defined with spatial dimensions as parameters. The dependence of a thermal resistance and capacitance on the spatial co-ordinates is determined by the heat flow equation:

$$C_T \frac{\delta T}{\delta t} = H + \kappa \Delta T \tag{3.2}$$

where C is the thermal capacitance per unit of volume in $JK^{-1}cm^{-3}$, T is the temperature in K, H is the heat generation per unit of volume in Wcm^{-3}, κ is the thermal conductance in $WK^{-1}cm^{-1}$. If we introduce an analogy between the thermal capacitance per unit of volume with electrical capacitance per unit of volume, the thermal conductivity with electrical conductivity, the temperature with voltage and the heat generation with electrical current, than heat equation is analog to the following partial differential equation:

$$C \frac{\delta V}{\delta t} = i + R \nabla V \tag{3.3}$$

For solving this differential equation system must be discrete. In a three-dimensional discrete system current flow is allowed in direction of x, y and z

axis. To solve the equation the boundary conditions must be given. Boundary conditions are determined by means of ambient temperature and input power dissipation. Finally, we can represent the temperature distribution in a network of electrical resistances and capacitances. An elementary volume is represented in Fig. 3.7. As current through the capacitance is $C = \frac{\delta V}{\delta t}$, it

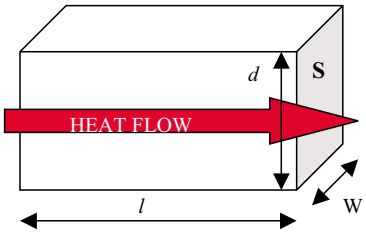

Figure 3.7: Definition of elementary dimensions in a section.

follows that all thermal capacitances must be connected to the ground. As current through resistance is $i = R\Delta V$ then resistances are connected into a network. For the three-dimensional rectangular mesh, the solution for the thermal resistance is:

$$R_{TH} = \frac{l}{\kappa S} \tag{3.4}$$

where l and S are dimensions shown in Fig. 3.7. The heat capacitance is given by:

$$C_{TH} = C_p \cdot S \cdot d \tag{3.5}$$

where C_p is specific heat per volume in $JK_{-1}cm_{-3}$. The thermal resistance at the junction of two materials is calculated direction as a parallel connection of two thermal resistors:

$$R_{TH} = R_{TH1} \| R_{TF2} \tag{3.6}$$

A mesh is generated using the simplest concept of classical rectangular meshing. A rectangular domain is divided into smaller rectangles by a classical mesh. Dimensions used in building of the thermal mesh are up to free choice of the researcher. His choice is of course limited with the computer speed. Physical quantities are calculated within the volume of mesh cubes. One possible choice of mesh dimensions used in this simulation is given in Fig. 3.8. The top layer thickness is set at $360nm$ which is in reality representing

thickness of both amorphous silicon and silicon nitride layer. The thickness of glass layers is set at $1\mu m$, although in reality the thickness of the glass substrate is usually much thicker. The materials involved are amorphous

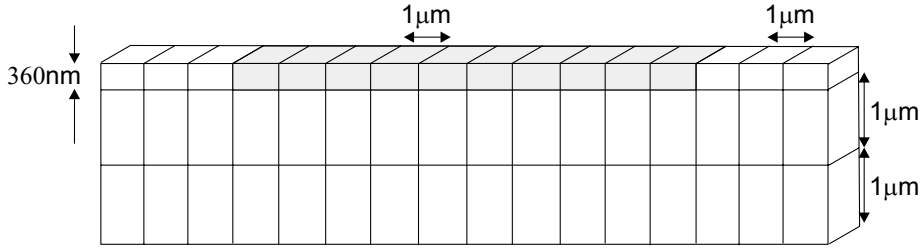

Figure 3.8: Meshing dimensions.

silicon, glass (Corning), metal (Molybdenum or Aluminium) and silicon nitride. Their thermal conductance and specific heat at room temperature are given in table 3.1. In this simulation it is assumed that both thermal conductance and specific heat are temperature independent, for simplicity. It is apparent that these materials have a similar value of thermal conductance, which is very low in comparison with thermal conductance of crystalline silicon. That is the reason why the problem of heating exists in amorphous silicon TFT's, despite the fact that the power dissipation is never high (because of low carrier mobility).

Material	Thermal conductance $[WK^{-1}cm^{-1}]$	Specific heat per unit volume $[JKcm^{-3}]$
α-Si	0.018724	2.3405
Glass	0.01	0.66988
Si_3N_4	0.0187	2.2737
Al		0.921096

Table 3.1: Characteristics of materials.

3.3 Intrinsic thermal-electrical effects in α-Si TFT's

The steady state solution of this simple 2D structure is given in Fig. 3.9. It represents temperature distribution along the channel. The simulated structure is n-type TFT, with electron mobility $\mu = 0.3cm^2/Vs$, $V_T =$

$6V$ and bias conditions are $V_D = 350V$ and $V_G = 50V$. As voltage is applied on drain and the source is grounded, the temperature has the highest peak at the drain side. Moving closer to the source side, the temperature decays. The temperature at the source side has value that is very close to room temperature. Extension of 2D simulation to 3D simulation is obtained

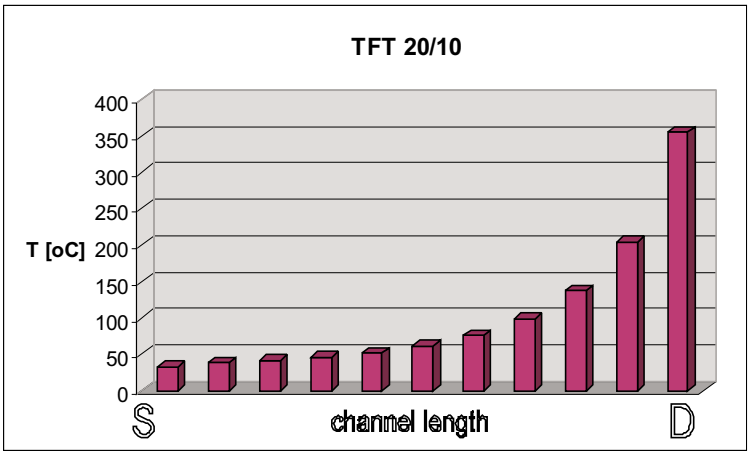

Figure 3.9: Steady state solution for 2D simulation.

by splitting the TFT in the channel width direction. The scheme of the electrical circuit used in 3D simulations is shown in Fig. 3.10. The total channel width is split in 5 rows, which do not interact in the electrical, but only in the thermal circuit. It is possible that electrical current exists in the lateral direction. Simulation of this current would be possible if a TFT would be added between two neighbour nodes in two consequent rows. In this case this lateral current is neglected for simplicity. In our case, a TFT with dimensions $L = 10\mu m$, $W = 100\mu m$ is modelled with a network of 50 TFT's with dimensions $L = 1\mu m$ and $W = 20\mu m$. For building of the thermal circuit for 3D simulation, the same method is applied as in 2D simulations. The only difference is that part of the circuit is added to represent temperature dissipation into direction of new added dimensions. The new part of the circuit has the same mesh used for lateral dissipation in 2D dimensions. The results of 3D simulations obtained under steady state conditions are presented in Fig. 3.11. Transistor dimensions are $L = 10\mu m$ and $W = 100\mu m$. The transistor model is n-type TFT. Biasing conditions for both simulations are: $V_D = 350V$, $V_G = 50V$.

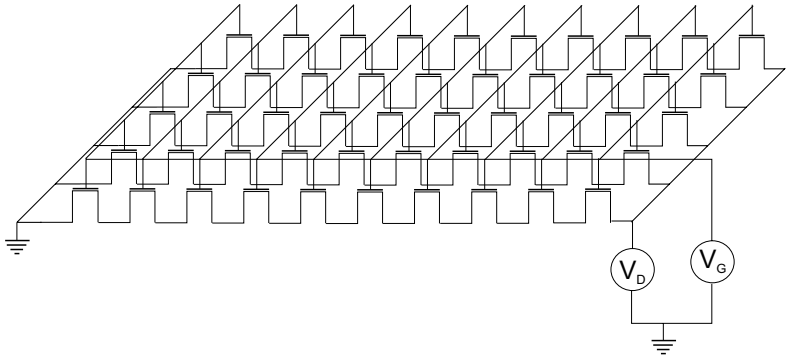

Figure 3.10: Electrical circuit as used in 3D simulation.

3.3.1 Transient simulations for different ESD pulse duration

The result of a transient analysis is given in Fig. 3.12. Firstly, an ESD event is simulated, with voltage pulse of length $100ns$, with rise and fall time of 10 ns, applied on the drain. Gate voltage is $V_G = 50V$, source is grounded. In this time scale self-heating process is not completed, In other words, the temperature has still not come to the value calculated in DC simulation (at the hottest point 325 ^oC). Length of applied drain pulse is increased in steps (100 ns, 200 ns, 500 ns, 1 μs, 100 μs and 1 s) in order to determine when self-heating process is completed. For drain pulse lengths of 100 ns, 200 ns, 500 ns and 1 μs the hottest point temperature is increasing with time and yet is not reached equilibrium. Also, there is not much difference between temperature between rows. The temperature is homogeneously distributed over device. For pulse length of 100 μs, the temperature comes to saturation and the level of temperature is the same as the previous one from DC analysis. It saturates after 15 μs (Fig. 3.12). Finally, for the length longer than that, as it is shown in Fig. 3.12 for pulse length of 1 s, the temperature is constant.

Thermal simulations of TFT's include many approximations, which are not present in reality, so it would be difficult to give a reliable answer to the question what is the temperature level under certain current and voltages. Nevertheless, the distribution of temperature is determined. It can be described as:

- if a voltage is applied on the drain, than the drain becomes the hot region.

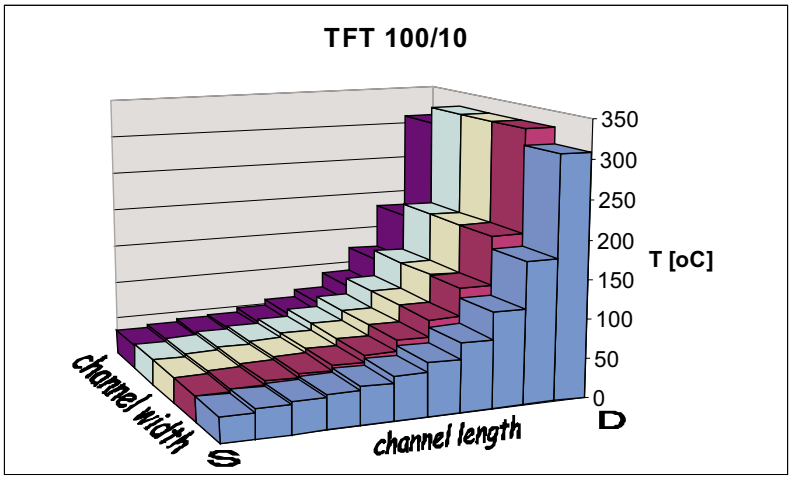

Figure 3.11: Steady state 3D simulation.

- if the same voltage is applied on the drain, then steady state conditions will produce much higher temperatures than transient in a time range of a couple hundreds nanoseconds.

The most important value of this simulation is that the simulated distribution of temperature corresponds to the results shown in the Chapter 2. The question that was not answered in the Chapter 2 is whether the change of breakdown with the change of the stress time is related to the thermal heating. The transient simulations of the self-heating are the link we need to completely unveil the process of ESD failure in TFT's. A relation between Fig. 3.13 and section 2.4.1, where it was shown how the breakdown voltage depends on the stress duration. If we relate the experimental facts with the results of the transient simulations, we can state that after the TFT enters thermal equilibrium and constant temperature is established, the breakdown voltage will become constant.

It was mention earlier in section 2.4.2 that there are two distinguished regions of the damage creation over time. There is a region when the damage threshold decreases with time ($t < 100\mu s$ and a region when the damage threshold stays constant although stress time is increased, as shown in Fig. 2.19. That behaviour was extracted from the experimental results and it can be explained with the help of the Fig. 3.13. Namely, the damage creation is a thermal process. Therefore the amount of the created states depends on

the temperature of the system. Therefore the threshold of damage creation depends on the stress time due to the fact that the temperature in the system depends on the stress time as well. For very short stress times ($t < 100\mu s$) the temperature of the system changes with time (Fig. 3.13). After 100 μs the temperature of the system is constant with increasing the stress time, which means that if the stress time is longer than that, the process of damage creation starts always with the same voltage.

3.3.2 Self-heating in TFT's with different channel length

Electro-thermal simulations of the TFT's with variations of the channel length have been performed in order to show the temperature distribution over the TFT area in the short and long TFT's. The biasing conditions are: gate voltage V_G=60 V and drain voltage V_D=100 V. These biasing conditions are chosen to show the heat generation in the most severe case. The simulations were performed under assumption that the heat generation is equally distributed in all four lateral directions over glass area.

The area surrounding the devices was the same in all simulations. Only the channel length was varied, while the channel width was constant, as well as the drain and the source metal contacts widths. The simulated structure is designed according to the top-gate device built on a glass substrate and from the top side passivated over all device area, used in the experimental procedure. The temperature distribution shown in Fig. 3.14 is the temperature of the glass substrate in the first layer under the amorphous silicon layer. In Fig. 3.14 the channel length area has on the x-axis a finer grid than the surrounding substrate. The temperature distribution over TFT's shown in Fig. 3.14 is similar in all four cases. The simulations show that the temperature peak is located always at the drain side. Across the channel length, the temperature decreases from drain to source. In case of short devices the distribution is very much uniform across the channel length. For the channel length of $L = 4\mu m$ (Fig. 3.14), the simulation shows that the TFT is overheated. The simulated temperature is impossibly high ($\Delta T = 2400^oC$), so it implies that in the reality the TFT would be already broken down. Fig. 3.14 shows that in the TFT with $L = 6\mu m$ the temperature is relatively high ($\Delta T = 120^oC$). The device with $L = 10\mu m$ suffers much lower heating ($\Delta T = 28^oC$). Finally, the device with the length $100\mu m$ is not heated ($\Delta T < 1^oC$). The simulations confirm that short channel devices suffer from more pronounced thermal heating due to the larger localised power dissipation.

3.4 Summary and future work

Electro-thermal coupled simulations have been performed to find out if a TFT under the ESD stress suffers from self-heating. The simulation method uses an electrical circuit coupled with a thermal circuit. The thermal circuit is an electrical circuit where currents represent heat flow and voltages represent temperatures, a current source represents the power dissipation. The simulation method has been explained, 2D simulations have been performed in DC and 3D simulation have been preformed in DC and transient regime. A number of simulations has been preformed for TFT's with different channel length and for different ESD pulse durations. It was concluded that the temperature peak in a grounded gate TFT stresses on the drain is located at the drain side of the α-Si:H channel. As expected, our simulation results indicated that the self-heating is much more pronounced in short-channel TFT's. Simulation results also reveal that the time-constant of a TFT is 15 μs, prolonging the stress after 15 μs will not increase the self-heating. The simulations prove that, upon specifying a critical temperature at which failure is declared, the breakdown voltage of a TFT under ESD conditions changes with the channel length/temperature and the temperature/ESD duration relation.

As TFT's are very simple devices from the point of view of their geometrical design, they are rather easy to simulate. For given examples, the execution time of transient 3D simulation is about 30 seconds. It is due to the fact that only rectangular mesh is used, but also due to very simple simulated structure. It is possible to refine this work by:

- using a better mesh (by Lumex or any similar program as mesh generator)
- using design structure which would be more similar to the real structure (including metal lines for drain, source, gate and light-shield which would act as a heat sink in the thermal circuit)
- taking into account the feedback effect of the local device temperature on the thermal conductivity and specific heat
- simulating TFT's with different channel length, and check if experimentally obtained result that higher breakdown voltage (i.e. lower temperature peak) corresponds to longer channel length
- thinking about a TFT structure that overcomes the self-heating problem and increases the breakdown capability of TFT's and that can be

used in the ESD protection structures (this issue is reported in section 3.3)

- changing pulse length in the transient simulations with different pulse length, rise and fall time. Also it could be possible to determine when the temperature will reach saturation, i.e. time constant of heating up the system.

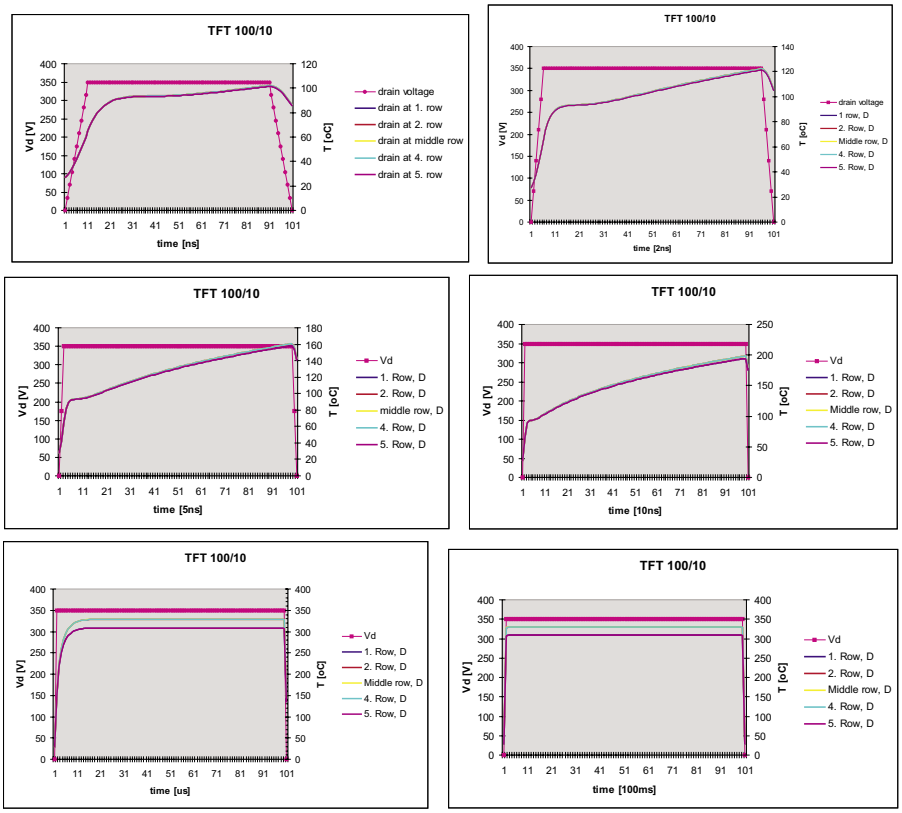

Figure 3.12: Transient 3D simulation calculated at the five points at the drain side for different pulse duration a.) stress time 100 ns, T_{max}= 100 ^oC, b.) stress time 200 ns, T_{max}= 120 ^oC, c.) stress time 500 ns, T_{max}= 160 ^oC, d.) stress time 1 μs, T_{max}= 200 ^oC, e.) stress time 100 μs, T_{max}= 330 ^oC and f.) stress time 1 s, T_{max}= 330 ^oC.

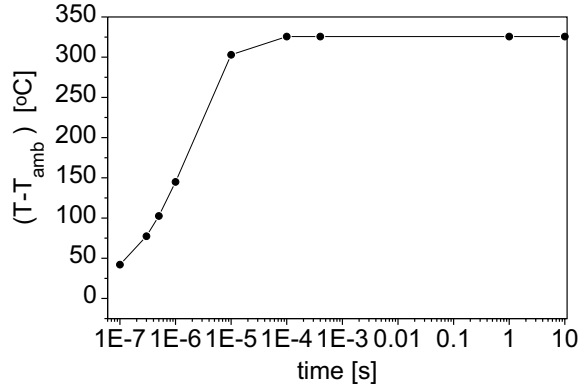

Figure 3.13: Transient thermal simulations showing the temperature rise at the hottest point in the TFT for different TLM pulse lengths.

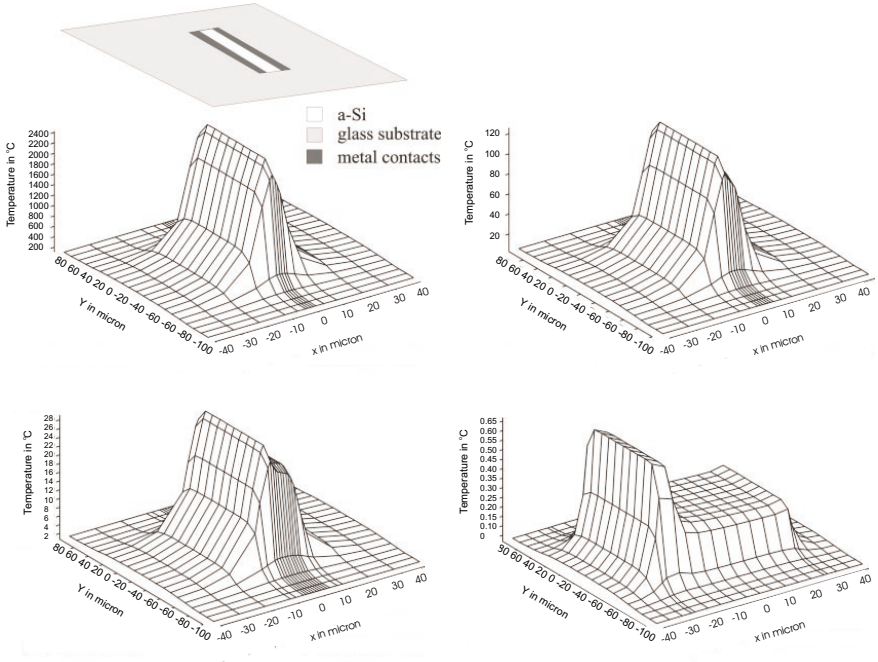

Figure 3.14: Thermal simulations showing the temperature distribution in the TFT's with different channel length (L= 4, 6, 10 and 100 μm).

Chapter 4

Band-gap density of states under ESD stress

In this chapter intrinsic properties of the amorphous silicon layer in a TFT under ESD stress conditions will be analysed. The density of states within band gap induced by ESD stress will be investigated. A method for calculation of the density of states will be presented and then used to calculated the density of states before and after applying ESD stress.

4.1 Theory of band-gap density of states

The atomic network of amorphous silicon is disordered and can have all range of silicon bonds, such as covalent bonds, week bonds, dangling bonds and due to the presence of hydrogen also silicon-hydrogen bonds. There are certain energies in the band gap which corresponds to the specific silicon bonds. Not more then two electrons with different spin could have the same energy level, therefore the energies of the bonds are spread all over the band gap. These bonds still obey a certain distribution. In the first place, bonds within the band gap could be divided into tail states and deep states. Tail states are located next to the edges of the conductance and valence bands. They appear due to the silicon week bonds. Deep states are located as the name says deep into the band gap. They are due to the dangling bonds. States close to the conductance band are equivalent to donor states. They are be charged positively. The closer to the conductance band, the more positive charge they have. States close to the valence band are equivalent to acceptor states. They can be negatively charged. Therefore states in the

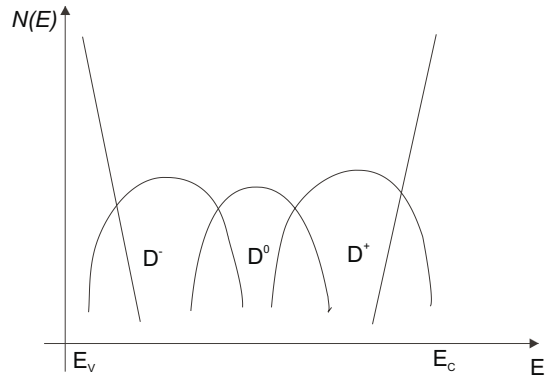

Figure 4.1: Energy gap states in amorphous silicon.

middle of the band gap are neutral. The distribution of the tail states is represented by a linear function and the distribution of the deep states by a sum of Gaussian functions, as it is shown in Fig. 4.1. The energy gap $E_c - E_v$ is typically around 1.8 eV at room temperature. In hydrogenated amorphous silicon the majority of defects are passivated with hydrogen, reducing the density of the deep states to typically $10^{16}\ cm^{-3}$.

There are different models developed to describe numerically density of states. The method for determing the density of states function $N(E)$ throughout most of the energy gap, which will be used in this thesis, is based on field-effect conductivity measurements.

4.2 Field-effect method for DOS estimation

An analytical method, which correlates the density of states within the energy band gap and field-effect conductivity measurements, was firstly proposed in the seventies [35]. Shortly, from the measured $I_D(V_G)$ characteristic, the amount of space charge induced by voltage V_G can be calculated. Since then, the method is further enhanced by many authors [24], [50], [12], [27], [20]. Powell [42] gave an overview of different variations of this method, and a discussion of the approximations introduced in them, such as constant space-charge density and zero-temperature statistics. It was shown that from field-effect conductance measurements only the broad features of the density of states can be determined and a unique N(E) is not identifiable. Later on [30], it was shown by Fortunato et al. that a class of methods called approximate methods of directly extracting the DOS [24],

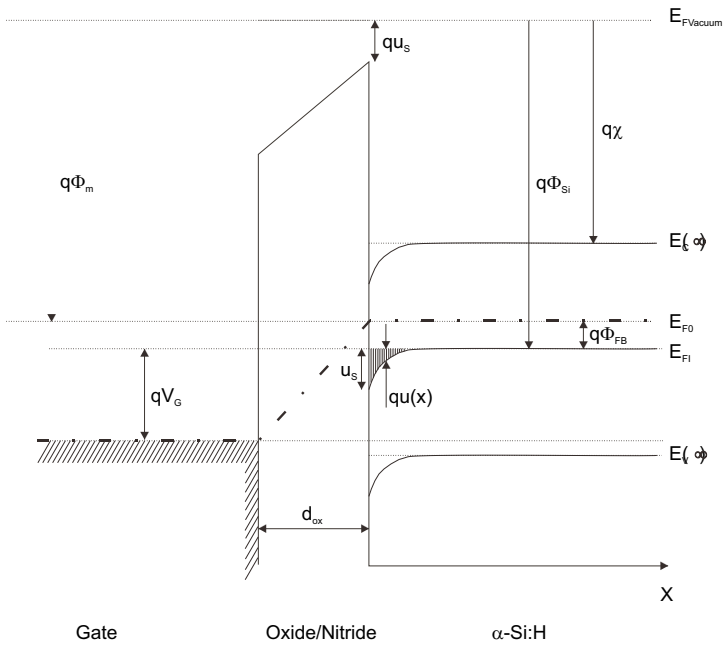

Figure 4.2: Graphical representation of the energy bands under positive gate voltage.

[60] retain a reasonable degree of accuracy. In this thesis Suzuki's method is used [60] for estimation of density of gap states due to the influence of the surface states. The method will be described briefly.

The surface potential u_s, the voltage across the oxide V_{ox}, and the work function difference between the gate material and the amorphous semiconductor V_{FB} are related with the gate voltage by:

$$V_G = V_{ox} + V_{FB} + u_s \tag{4.1}$$

The band bending in the surface space-charge layer of the α-Si is defined by:

$$u_x = \frac{E_C(\infty) - E_C(x)}{q} - \frac{E_F(\infty) - E_F(x)}{q} \tag{4.2}$$

A schematic representation of the energy bands in the TFT under the positive voltage on the gate is shown in Fig. 4.2. Relation between the gap states $N(E)$ and the band banding $u(x)$ is expressed from the Poisson's

equation:

$$\frac{d^2u(x)}{dx^2} = -\frac{\rho(x)}{\epsilon} \tag{4.3}$$

$\rho(x)$ is space charge density at the depth x in the bulk of amorphous silicon due to the local Fermi-level shift of $q \cdot u(x)$, ϵ is dielectric constant of amorphous silicon. At low temperatures, $\rho(x)$ is related to the gap state density distribution by:

$$\rho(x) = -q \int_{E_{FSi}}^{E_{FSi}+q\cdot u(x)} N(E)\mathrm{d}E \tag{4.4}$$

where E_{FSi} is equilibrium Fermi level in Silicon ($x \to \infty$) and q is elementary electron charge. After replacing space charge density by zero-temperature statistics, the gap state density is obtained from 4.3:

$$N(E_F + qu) = \frac{\epsilon}{2}\frac{\delta^2}{\delta(qu_s)^2}\left[\left.\frac{du}{dx}\right|_{x=0}\right]^2 \tag{4.5}$$

where u_s is surface potential in the amorphous silicon. Knowing that electric field is given by:

$$\left.\frac{du}{dx}\right|_{x=0} = -\frac{\epsilon_{diel}}{\epsilon}\frac{V_{diel}}{d_{diel}} = -\frac{\epsilon_{diel}}{\epsilon}\frac{V_G - V_{FB}}{d_{diel}} \tag{4.6}$$

where ϵ_{diel} represents dielectric constant of the gate insulator, d_{diel} is its thickness. Voltage across the gate dielectric V_{diel} is expressed by gate voltage V_G and the flat band voltage V_{FB}, regarding to equation 4.1. Flat bend voltage is difference between metal work function and Si work function in case when energy bands are flat, e.g. no gate voltage is applied (Fig. 4.2). Substituting 4.6 into 4.5 the gap density of states can be calculated if the function between gate voltage and the surface potential in the semiconductor is known. This function is obtained from the measured field-effect data by the sheet conductance $G = \frac{I_{DS}}{V_{DS}}\frac{1}{\frac{W}{L}}$:

$$\delta G = \frac{G_0}{q^2(V_G - V_{FB})}\frac{\epsilon}{\epsilon_{diel}}\frac{d_{diel}}{d}\left(\exp\left(\frac{qu_s}{kT}\right) - 1\right)q\delta u_s \tag{4.7}$$

Before applying, the method is validated in a way. The Silvaco numerical simulator [14] is used as a reference for validation of the analytical method. The developed algorithm is used on Silvaco's simulated transfer characteristics and the result is later compared with the DOS from the Silvaco's input

file. It is concluded that this method gives absolutely correct result for the tail states but not for the deep states. In other words, some DOS parameters can be extracted from the calculated curve, such as slope of the tail states distribution, density of states at the conduction band edge and the position of the tail states peak. However, the level of the deep states concentration is underestimated. The reason for that is that zero-temperature approximation is used for the local space-charge density. Another difficulty with field-effect based DOS calculations is that for calculating the DOS over the band gap, below and above Fermi level, one must have both p-channel and n-channel TFT's [49]. The problem is also that the range of energies within which the DOS is calculated is normally much smaller then the energy gap itself. In spite of these uncertainties, the model is found useful for a rough DOS estimation, especially if only a comparison of density of states before and after stressing is needed. The calculation of DOS from field-effect conductance measurements is very sensitive to flat-band voltage. Therefore, the flat band voltage determination has been a subject for discussion. It was determined in different ways [54]. In this chapter the flat band voltage at the surface was determined as the gate voltage at which the onset of the field-effect conductance occurs [60]. Namely, we assume that current conduction occurs in the very shallow layer at the amorphous silicon/silicon nitride interface. The flat-band voltage at interface is per definition the difference between metal work function (gate) and amorphous silicon work function in case when energy bands are flat. It is known from the defect pool model that energy bands deep in the amorphous silicon are never flat [12]. Consequently, the "flat band voltage" at the interface is now the difference between metal work function (gate) and amorphous silicon work function in case when surface potential is equal to zero. As surface potential is equal to zero, it means that there are no surface charges and consequently the field-effect conductance is also equal to zero. When the gate voltage exceeds the flat band voltage, the surface potential increases, which means that current conduction sets-in. In TFT's with silicon nitride as gate dielectric the flat band voltage is negative, assuming that there is no presence of fixed charges. The flat band voltage determined in this way was compared with the flat band voltage from Silvaco simulator and the results were in complete agreement.

4.3 DOS estimated before and after ESD

In Fig. 4.3 the calculated DOS after initial TLM pulse and the calculated DOS after a series of stepped 500 ns TLM stress pulse up to 420 V is plotted. Fig. 4.3 shows an increase in the density of deep gap states and tail states in the upper part of the band gap after ESD stress pulse just one step before breakdown was applied on the drain. Therefore that is the worst case of the change in the density of states. In contrast, in Fig. 4.4 a moment of the states creation when the ESD stress just exceeds the stress threshold is presented. Namely, in Fig. 4.4 the calculated DOS after the initial TLM pulse is compared to the calculated DOS after a series of 500 ns TLM pulses up to 240 V. It can be noted that only the number of the deep states is slightly enhanced, whereas the number of the tail states is not changed at all. Thus, it can be concluded that deep states are more sensitive to ESD stress then the tail states. Fig. 4.4 also shows the density of sates calculated after an annealing experiment. Next to the plots previously explained are two DOS curves calculated before and after another series of TLM stress (up to 240 V), repeated after an annealing cycle. TFT's are annealed at 250 ^oC for 2 h and cooled down to the room temperature without applied bias. Annealing reproduced the original density of states. It is obvious that the states in the band gap could not be annealed by temperature annealing.

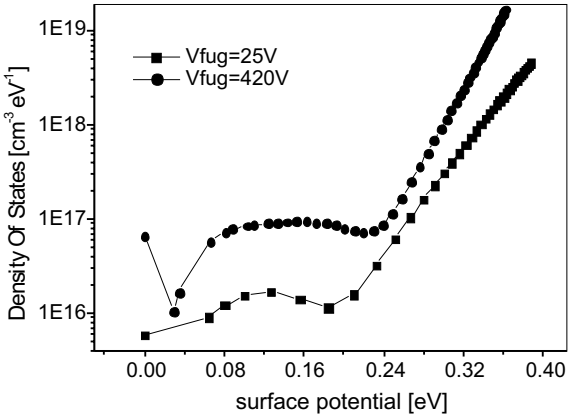

Figure 4.3: Density of states in the upper band gap calculated before and after ESD stressing.

It is shown in this section that ESD stress prior to catastrophic breakdown can induce damage in the DOS of amorphous silicon. If a stepped

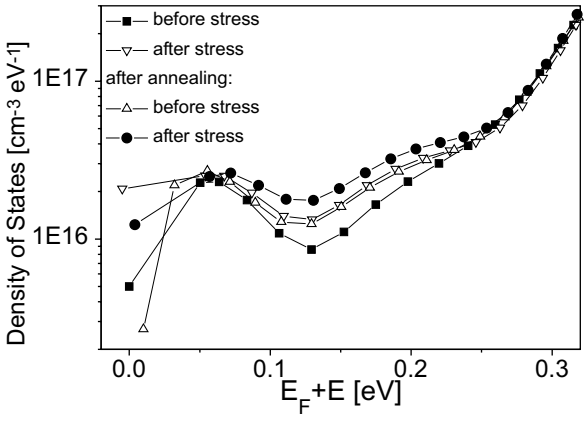

Figure 4.4: Density of states calculated in order to show the effect of annealing on the states created due to ESD stress.

positive ESD stress is applied to the TFT's drain, the number of deep states and the tail states in the upper part of the band gap increases. During TLM experiments the DOS in amorphous silicon gradually changes with every ESD stress exceeding threshold. When ESD stress is low only the deep states density increases, but if ESD stress is further increased the density of tail states increases as well. The created deep states could not be removed by dry annealing to 250^oC. This is an important conclusion and it has to be correlated with the experimental findings from Chapter 2. It means that the pre-breakdown degradation of threshold voltage and transconductance that occurs under lower ESD stresses (Chapter 2) is, at least in some extent, due to the creation of gap states in the amorphous silicon. Comparing the results of the annealing experiments from section 2.2.6 and the DOS calculations of the annealed TFT as from Fig. 4.4, we can conclude that the transconductance change is not related with the creation of the density of states in the amorphous silicon. Namely, the transconductance is proved to be annealed and the change in the DOS is not. The reason for the change of transconductance has been found in accumulation of the positive charge at the silicon/nitride interface in location close to the stressed drain electrode. Having that in mind, and the fact the the DOS calculations assumes the homogenous distribution along the channel, it can be concluded that the total amount of the states in the amorphous silicon channel remains constant during and after thermal annealing, but the distribution of the charges along the channel may be changed.

4.4 Summary

To summarise, we have calculated the density of states in the band gap of α-Si:H TFT's before and after applying ESD stress. The calculation uses a field-effect technique. The calculations showed that a stepped TLM stress creates an amount of the gap states. Initially the states are created in the mid-gap. If the stress is increased also the number of the tail states increases. Thermal annealing proved not to be able to remove the ESD stress induced states.

Chapter 5

Dealing with ESD in a TFT circuit - a fingerprint sensor

In the previous chapters an ESD event is evaluated in a single TFT. In practice we often have to deal not with a single TFT, but with a TFT in an electrical circuit. Nevertheless, the knowledge gained testing a single TFT's behaviour under ESD stress provides us a basis that is needed when we have to deal with a TFT circuit. In this chapter an example will be given of ESD related considerations when making a TFT circuit. The chosen system is a fingerprint sensor. The sensor is developed in our laboratory. The manufacturing process will be explained. The behaviour under ESD stress will be analysed. A solution for ESD protection will be proposed.

5.1 Introduction

A fingerprint is unique for each of us. Therefore it is since the middle of the nineteenth century used to identify a person. Nowadays a small electronic fingerprint sensor could be used to provide automatic recognition of individuals. It can be used to protect access to, for example, mobile electronic devices such as mobile phones or laptop computers, instead of a PIN (personal identification number) code, a key or a password. The area of possible application is very wide. The whole recognition system has to satisfy in the first place extraction of the features of a finger (the sensing element), and secondly matching and accuracy of the characteristics of an individual with previously recorded characteristics is needed.

Different types of the electronic fingerprint sensors are currently in use. Some of the possible image capture principles are:

- Solid state sensors: based on the principle of capacitive coupling or temperature differences. Since this technology was introduced in the late 1990's, it is increasingly applied.
- Ultrasonic sensors: using acoustic waves. This technology is still in its infancy and has not yet been widely used.
- Optical sensors: reflection principle or with a tactile sensitive light-emitting foil. Optical technology is oldest, and is demonstrated and proven technology, but the optical sensors are bulky and costly.

In this chapter we will deal with the α-Si:H TFT sensor with capacitive coupling, as this is from ESD prospective an interesting option.

5.2 Capacitive principle

The capacitive fingerprint sensor in thin film technology was developed in Philips Research Laboratories, Redhill, UK, [32], back in 1994. Nowadays it is commercially manufactured by companies like Veridicom (OpenTouch), SGS Thomson (TouchChip), Infineon (Fingertip), Sony (Puppy FIU-700). It is commonly known that the capacitive fingerprint sensor has a very good image quality but a poor durability due to ESD.

A fingerprint sensing device is a row/column array of sense elements which are coupled to a driving circuit. The sense elements are addressable by the drive circuit. An output from the sensing circuit in analysed in the recognition system. Characteristical data is compared with stored characteristical data for identification and verification purposes. A simplified schematic diagram of the array of the sense elements with the addressing circuit is shown in Fig. 5.1.

5.2.1 Working of the sense element

Each sense element contains a sense electrode and a switching device (e.g. a TFT) for active addressing of that sensing electrode. The sense electrodes of the sense elements are covered with an insulating layer, for example of silicon nitride or polyimide. If a person touches the sensor a capacitor is formed between the finger and each sensing plate. These capacitances are sensed by the sense circuit by applying a potential to the sense electrodes

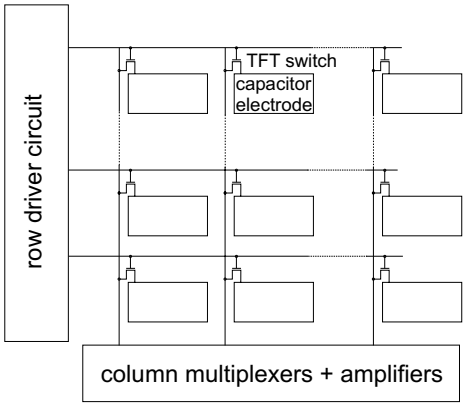

Figure 5.1: A simplified schematic diagram of the sense elements together with associated addressing circuitry.

and measuring charging characteristics. Depending whether a ridge or a valley of a finger touches the sensor surface, the capacitor will have a higher or a lower value. A schematic representation of a sense element is shown in Fig. 5.2. The pixel plate is precharged to the value V_p. The capacitance of

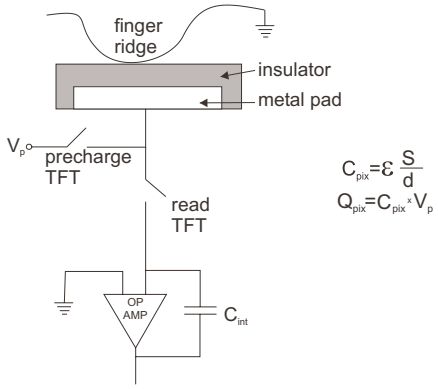

Figure 5.2: Schema of the capacitive fingerprint sensor.

the pixel is determined by the pixel plate area S and the distance between the pixel plate and the finger d. The amount of charge at the pixel plate is proportional to the precharge voltage and the pixel capacitance, $Q_{pix} = C_{pix} \times V_p$. An operational amplifier with capacitive coupling is used to

integrate the charge. The output current is further handled by column multiplexers.

5.2.2 Fabrication of the capacitive fingerprint sensor

We made the capacitive fingerprint sensor based on thin film technology. The sensor is based on the bottom gate (inverted-staggered) α-Si:H TFT. The TFT's were n-channelled, with a silicon-nitride gate insulator. A schematic cross-section of a fingerprint cell is given in Fig. 5.3. As the thin film technology is used in well established technologies such as liquid crystal display devices, and as such it is described well (see for example [71]), here the technology of making the capacitive fingerprint sensor will be described only briefly.

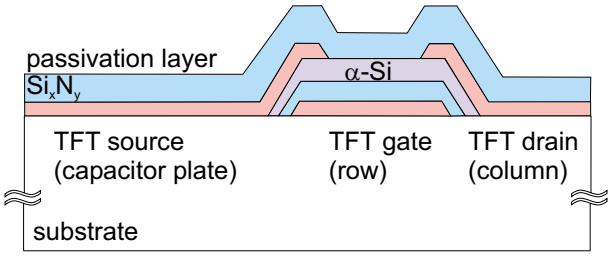

Figure 5.3: Cross section of a pixel in the capacitive fingerprint sensor.

The fabrication process involves six photolithographic processes. These processes are listed in Table 5.1. Fig. 5.4 shows diagrammatically how the

mask	layer	material	thickness [nm]
1	gate metallisation	Al	300
2	etch stop	SiNx	350
3	drain and source implantation	α-Si:H	300
4	opening bottom metallisation layer	SiNx	300
5	top metallisation	Al/Mo	300
6	passivation	SiNx	350

Table 5.1: TFT process flow with layer materials and thicknesses.

amorphous silicon TFT (coupled gate TFT, as used in the ESD protection structure) are fabricated.

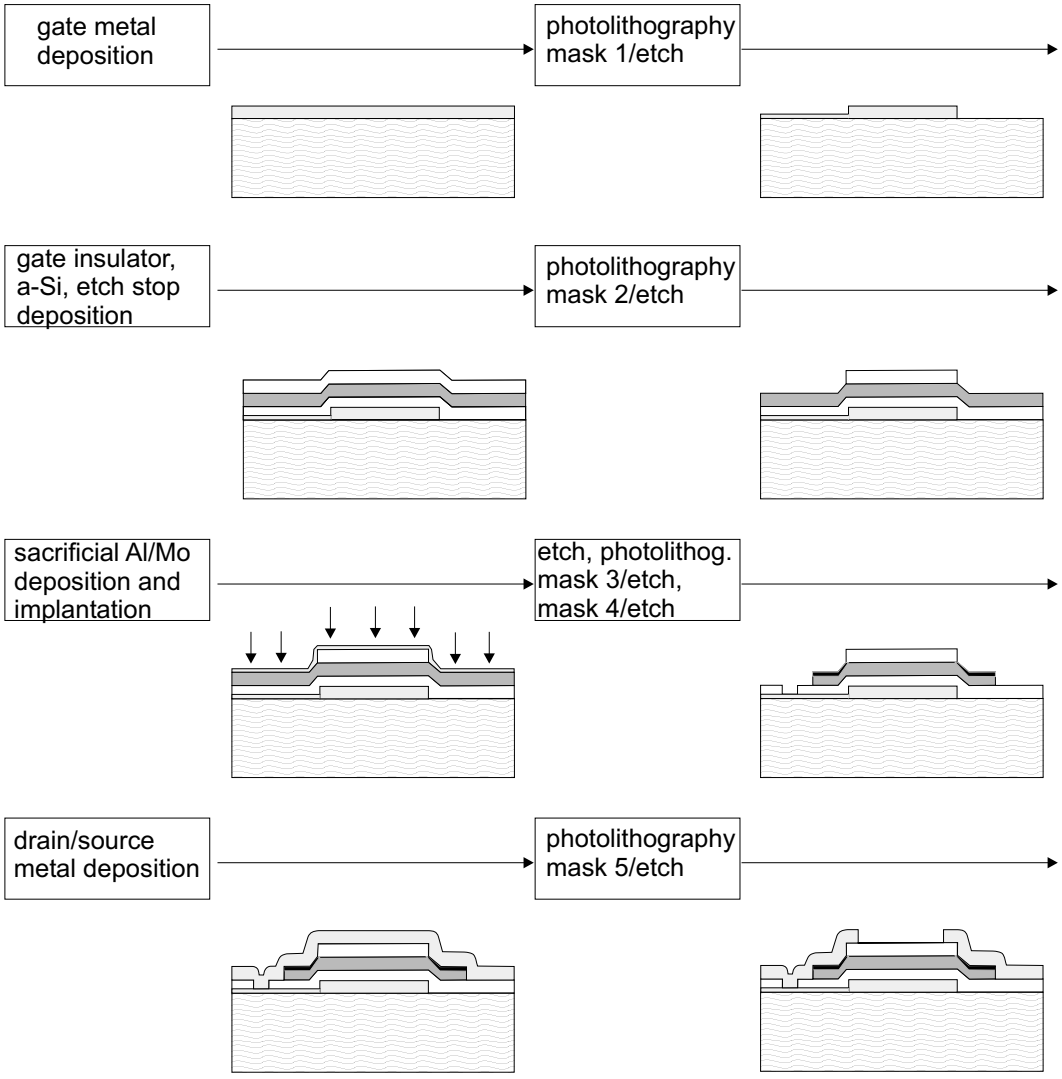

Figure 5.4: Coupled gate amorphous silicon thin film transistors fabrication process. Note that the last (passivation) photolithographic step is skipped.

As substrate material we used a Si wafer with a thick (1 μm) layer of thermally grown SiO_2. For the deposition of Al and Mo we chose sputtering. For the deposition of amorphous silicon and silicon nitride we used PECVD (Plasma Enhanced Chemical Vapour Deposition). The deposition temperature was 250 ^oC and the discharge frequency 13.56 MHz. Three layers (SiNx as the gate dielectric, α-Si:H as the TFT channel and SiNx as the etch stopping layer, protecting the channel from the following etching processes) are deposited without breaking the vacuum. Wet etching was used for etching of all layers, except for the second metallisation layer made with Molybdenum. To make a highly doped α-Si:H for the source and drain contacts, ion implantation through a thin (10 nm) Al layer, or 20 nm Mo layer was used. Implantation through Mo layer produced a better contact. We implanted both phosphorus and arsenic. Phosphorus implanted TFT's gave lower contact resistance. We also made a variations with the dose and energy when implanting phosphorus in order to optimise the implantation parameters for source/drain contacts. The devices were annealed at 280 ^oC for 1 hour.

5.2.3 Characterisation of α-Si:H and SiN:H films

The thicknesses of the films are determined by spectroscopic ellipsometry. The thickness of the α-Si:H layer is estimated at 295 nm (mean value) and the thickness of the SiN:H layer is estimated at 373 nm. Also the refractive index of SiN:H was measured and it showed the value of 1.71, which implies that the quality of the SiN:H is relatively good, as the value of the refractive index of the stoichiometric silicone nitride is about 2.

The structure of the α-Si:H layer has been verified by X-Ray Diffraction (XRD). Fig. 5.5 shows the measured XRD spectra of α-Si:H before and after thermal annealing at 280 ^{o}C during 1 hour. We see that there are no visible spots of the polycrystalline Si on XRD data. Scattering from very small "pre-crystalline" areas is visible. There are no visible effects of annealing on the state of material.

The composition of the SixNy:H layer has been determined by X-ray Photoelectron Spectroscopy (XPS). The results show that the ratio between silicon and nitride is Si:N=1:1. The stoichiometric silicon nitride would have Si:N=1:1.33. The result implies that the composition of the silicon nitride could be improved. The presence of hydrogen is also determined by XPS. Hydrogen is found in 12.5 %. The target value is 14%, so this could be improved as well.

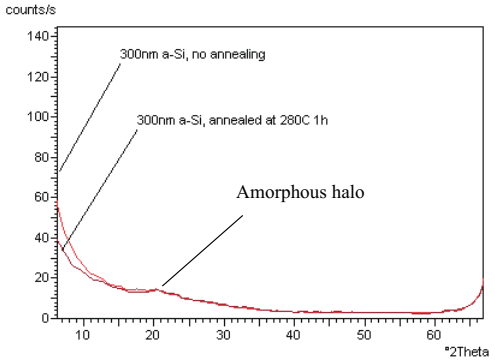

Figure 5.5: XRD scan of α-Si:H layer before and after thermal annealing.

5.2.4 Electrical measurements of deposited structures

On the wafer with a fingerprint sensor a number of testing structures , such as TFT's and capacitors, ESD protection chains, etc. was deposited in order to fully understand the performance of the fabricated sensor. Electrical measurements performed on these testing TFT's and on a pixel in the sensor matrix will be described in this section. Electrical measurements on the ESD protection chains will be shown in section 6.4.

TFT's with different W/L ratios were deposited. In Fig. 5.6 and 5.7 measured output and transfer characteristics of a TFT with W/L=100 μm/12 μm are shown. From the measured characteristics electron mobility and threshold voltage are calculated. The threshold voltage is determined from the interception of linear fit of the linear part of the transfer characteristic in the linear regime of working with the x-axis (V_D=0.1 V). The value of the threshold voltage for the given TFT (Fig. 5.7) is 2.8V. From the same linear fit of the transfer characteristic in the linear regime of working, the field-effect mobility in linear regime μ_l is determined by Eq. 1.3. The calculated value is μ_l=0.37 V/cm^2. The field-effect mobility in the saturation regime μ_s is calculated by fitting a straight line through $\sqrt{I_D}(V_G)$ curve measured in the saturation regime under V_D=10 V. The μ_s is 0.26 V/cm^2. For an ideal transistor, the field-effect mobilities calculated in both the linear and the saturation regime should be equal. But due to the neglection of the series resistance and also due to imperfect linear fitting a mismatch between μ_l and μ_s happens in practice.

The electrical characteristics of a pixel of the fingerprint sensor matrix measured before it was passivated are shown in Fig. 5.8. The figure shows

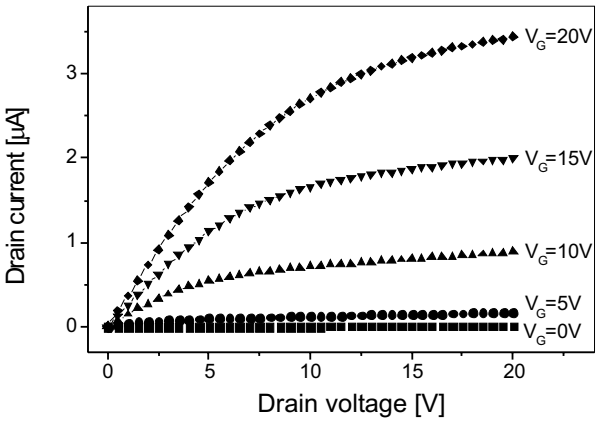

Figure 5.6: Output characteristics I_D/V_D under different gate voltages V_G=0, 5, 10, 15, 20 V of a TFT with W/L=100/12.

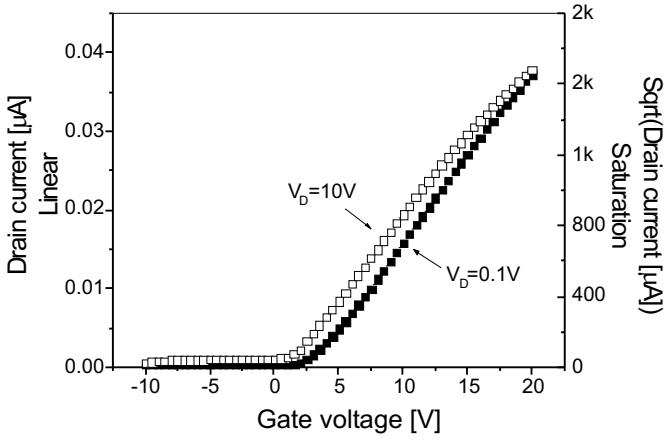

Figure 5.7: Transfer characteristics I_D/V_G under different drain voltages V_D=0.1, 10 V of a TFT with W/L=100/12.

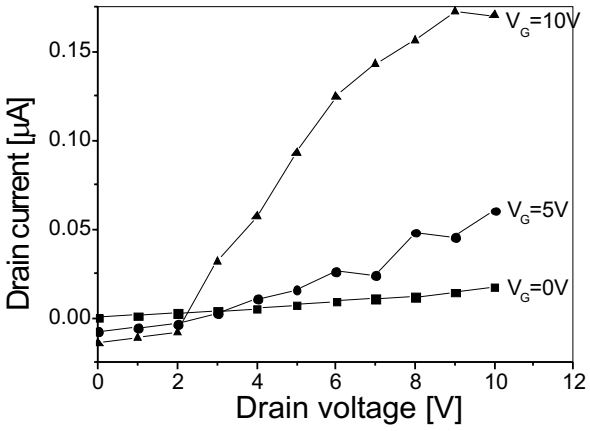

Figure 5.8: Output characteristics of a TFT switch in the fingerprint sensor matrix.

that the TFT in the matrix does operate as a switch. The dimensions of the TFT's in the matrix are W/L=21 $\mu m/8$ μm and therefore the level of the drain current is proportionally lower then in Fig. 5.6.

5.3 Description of the ESD problem

In a capacitive fingerprint sensor a possible ESD zap is applied either directly to the capacitive sensing element by the person who is using it or during the assembly process by a machine. The latter problem is successfully solved (for more information see Section 6.1) using the diode/TFT chains, and shortening all columns and rows during the manufacturing.

In the case when an ESD zap is applied directly to the sensing element, it is very difficult to find a good solution to protect the circuit. Under ESD stress, a possible current path goes through the top capacitance down to the ground Fig. 5.9). The elements in this path that have to be protected against ESD are:

1. the capacitor
2. the column "read" TFT
3. the amplifier circuits.

The most difficult task is to make the capacitor (actually the top dielectric layer) ESD insensitive. The idea is that the top layer must not be fully insulating. A resistive path must exist.

One solution that comes to mind immediately is to construct protection rings, i.e. walls of a conductive material connected to the ground around each pixel. These walls are generally obtained by gold electroplating in order to prevent oxidation [34] or of copper encapsulated by ruthenium, which is well known as a contact material and whose oxide is conductive [51]. This solution would certainly protect the sensor against the ESD up to a certain level, but it will introduce some additional problems. First is that the number of photolithographic masks will be increased, making the sensor more expensive (for applications like mobile phones it is very important to keep the price low). In some cases it can cause water penetration from the sensor surface to the active area [34].

Another possible solution is to make good choice of material used for the top dielectric layer. It should satisfy three conditions: to give ESD protection, to avoid charge loss in the capacitor and to not allow reduction of effective resolution. The easy solution for the last condition is good choice of the capacitor dimensions. In case the dimensions of the capacitor are: area $A = 50\mu m$ x $50\mu m$, insulator thickness $d = 500nm$ and distance between two cells $x = 10\mu m$ then the ratio of resistances in lateral and vertical direction is $R_s/R_p = 1600$. This ratio should provide good effective resolution of the sensor, as the lateral component of the current is almost negligible. Also, it may be possible to use material which is conductive in only one, for example vertical and not in lateral direction.

To avoid charge loss it is desirable to keep the insulator thin. This may counteract to the ESD robustness of the layer. The effect of the resistive layer may be presented as a parallel connection of a capacitor and a resistor, as it is shown in Fig. 5.9. Considering ESD conditions, the resistance R_p will take the ESD current (the current through R_s may be neglected as sufficiently lower). We have to determine how large this resistance should be in order to protect the surface layer and also not to influence too much the operation of the circuit under both DC and ESD conditions. There are two issues that have to be mentioned. First is that the current through the surface layer will produce power dissipation, $P = V_{Rp}^2/R_p$, which leads to heating. To simulate thermal behaviour of the surface layer would be straightforward using Silvaco tools, if the material (which will be used for the capacitor) were included in the simulator. We can also translate the conclusions from our experience with thermal simulations on TFT's stresses in the drain, Chapter 3. If the resistive layer is a moderate thermal conductor it can be expected that the peak of the temperature distribution will be at the surface, and that the peak of the temperature in the resistive layer

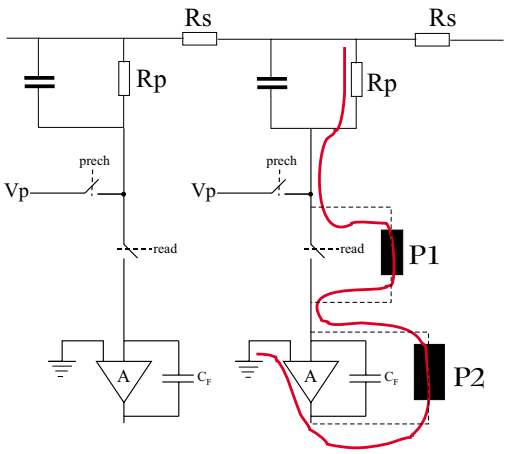

Figure 5.9: Current path in the capacitive fingerprint sensor.

will be lower when the layer is thicker (R_p higher). On the other hand, this resistive material could be a very poor thermal conductor or a very good thermal conductor. In both cases the thickness of the resistive layer would not play a role at the temperature distribution, as in the former case the temperature would be localised at the surface, and in the latter case the temperature would be transfered without losses to the rest of the sensor. Another issue important for ESD protection is that the current through the resistor R_p should produce a voltage drop sufficiently large to provide that the voltage on the TFT switch, which is directly connected to the surface layer via a metal plate, is never higher then the breakdown voltage of the TFT gate dielectric layer? In our case that is 330 nm Si_xN_y, having around 350 V breakdown voltage. In this way the TFT switch would be protected and the element P1 in Fig. 5.9 would not be needed.

Considering the ESD protection under the TFT switch (Fig. 5.9), it would be necessary to design the protection devices that will provide the path to the ESD current. It seems to be the second most important issue, after setting a proper material for surface. If this part of the sensor would be realised also in amorphous silicon thin-film technology, choice of the elementary structures for building a ESD protection would be very limited. The devices that one could use for protection elements P1 and P2 are only non-snapback type of protection structures, like:

- chains based on TFT's used as diodes - made by coupling the gate

and the drain directly together. This structure is already successfully used for each of the input and output terminals at the edge of the glass substrate. A more detailed examination of a similar structure will be presented later in the chapter 6.

- TFT's - as this devices never go to snapback, they can be used only in a non-breakdown mode. Normal MOS design can be used, as well as GC TFT (Gate coupled TFT) (Fig. 5.10). Considering transient regime, an appropriate choice of R and C would help to provide that TFT would turn-on only under a ESD zap.

- It would be also possible to use TFT's with a thick gate dielectric, to increase the breakdown voltage. A specific structure based on thin film technology could be designed and implemented for the protection element P1/P2 in Fig. 5.9.

- High voltage TFT. For the switch a high voltage TFT (with the drain extension L_D, as shown in Fig. 5.11) could be used. It would be used in connection to the resistor R_p with its drain, and would ensure that the electric field in the gate dielectric is such that TFT can withstand higher voltages. Instead of typical breakdown voltage of 350 V, it could be easily increased up to 600 V, as reported in [25].

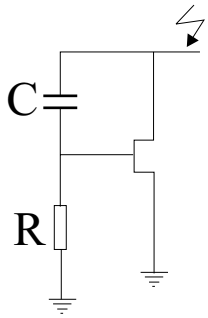

Figure 5.10: Gate coupled TFT.

5.3.1 ESD robust concept: resistive or pressure sensing?

As it was already explained in the previous section, the simplest (from the manufacturing point of view) way to protect the capacitive fingerprint

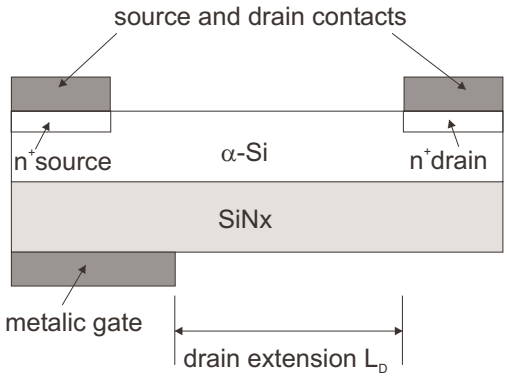

Figure 5.11: High voltage TFT.

sensor from the electrostatic charge of the human operating the sensor is to provide a current path to the ground introducing a material which would provide both good dielectric properties to allow for the capacitive sensing and good resistive properties for giving the "low"-resistive path for the ESD current [6]. It is a difficult task to optimise the material properties to satisfy all necessary conditions.

Another possible solution is to change slightly the concept of the sensor and to use resistive instead of capacitive sensing. The basic schema of the circuit could remain similar as in Fig. 5.9. Instead of the integrator an operational amplifier would be used for the amplification of the signal. The problem with the resistive sensor is that the current path would have to be closed through the human body. Although that is an almost negligible effect, many people would object to this approach.

The idea of the resistive fingerprint sensor could be also combined with the pressure sensing, using the piezo-resistive effect. In the piezo-resistive effect the electrical resistance of silicon changes with external pressure. At constant temperature, the resistance R of a semiconductor element of area A, length l, resistivity ρ is $R = \rho\frac{l}{S}$. When the element is strained (e.g. pressed) the resistivity changes by an amount:

$$\Delta R = (\frac{\delta R}{\delta l})\Delta l + (\frac{\delta R}{\delta \rho})\Delta\rho + (\frac{\delta R}{\delta A})\Delta A = \frac{\rho}{A}\Delta l + \frac{l}{A}\Delta\rho + \frac{\rho l}{A^2}\Delta A \qquad (5.1)$$

$$\frac{\Delta R}{R} = \frac{\Delta l}{l} + \frac{\Delta\rho}{\rho} - \frac{\Delta A}{A} \qquad (5.2)$$

A CMOS compatible micromachined tactile fingerprint sensor has been

reported in [39]. It would also be possible to use this approach in amorphous and polysilicon thin film technology. Piezoresisistive properties in polysilicon are affected by microstructure (fabrication process) and electrical properties (doping level). Unfortunately the micromachining part of the circuit would be quite expensive. The rest of the circuit is very simple, composed from passive components only. This concept is ESD robust, as the micromachining part, which is in direct contact with the human body, is not electrically active.

5.4 Summary

We have manufactured a capacitive fingerprint sensor with α-Si:H TFT's used as switches. The design, the process flow and the test measurements have been showed in this chapter. The sensor is used for an theoretical ESD analysis. The behaviour under an ESD stress has been described, and possible ESD solutions have been discussed. Several ideas for an ESD robust fingerprint sensor have been proposed.

Chapter 6

TFT based ESD protection

This chapter will be focused on testing and analysing of ESD protection devices based on thin film transistors. A number of varieties of protection structures made with coupled gate TFT's will be tested. Circuit simulations of a TFT matrix without and with ESD protection will be presented. Based on the testing and the simulation results a proposal of how to improve ESD protection in TFT circuits will be given.

6.1 Introduction

The ESD protection of a TFT based electrical circuit has to be efficient during the manufacturing and the application of the circuit from all potential sources of the creation of electrostatic charge. It should be noted that the design of any ESD protection is focused in two directions. First, electrostatic charging has to be prevented and second, the design of the protection structure should be optimised in such a way that there is no damage up to a certain stress level, the functionality of the product is not affected too much and it should not use to much area.

In this thesis we will not discuss preventing of the electrostatic charging. Only a few general remarks should be noted. TFT LCD's are built from a multi-layer structure on a glass substrate. Most of the processes in the TFT LCD's production combine movements, friction and separation of this glass substrate with other materials. Those processes are the cause for the generation of an electric charge at the surface of the glass. One of the main generators of the electric charge in the TFT LCD production process is the act of separation of the glass substrate from a metal surface (chuck) on which

it is laying during processing. The separation of the glass from the metal chuck creates an amount of electric charge in the glass according to the triboelectric theorem. The best method to prevent this type of ESD danger in to prevent it on-line [28], but that task will not be analysed here. One other way to prevent the electrostatic charging during the manufacturing is to short all row electrodes and all column electrodes by a shorting bar. That would protect the displays during the processing, although after the scribe and break process, when the shorting bars are separated from the active matrix, the glass plates become very vulnerable to ESD and this substrate can be easily charged during handling. One way to reduce the problem is the coverage of unused glass surface by dummy metal. The dummy metal creates equipotential surfaces and prevents the glass from being charged.

In this chapter the attention will be focused on the ESD protection, by gaining knowledge by measurements, modelling and simulations. The problem will be discussed in general, and similar analysis can be applied for any TFT matrix used in, for example, liquid crystal displays, for telecom applications, in automotive industry or in sensors. Each of these applications has some specific working conditions that has to be taken into account when one is designing an ESD protection circuit. These conditions will be shortly described. Knowing the conditions in which the circuit will operate will help to determine which method should be chosen for ESD testing and which criteria the ESD protection circuit has to satisfy.

TFT's used in telecom application (e.g. mobile phones) suffer from an additional restriction when we are talking about ESD protection. Namely, there is always a significant leakage through the ESD ring at the operational voltage. And in mobile phones power consumption is very important [41]. Therefore the leakage currents that are allowed in LCD's where a constant power supply is present are actually not allowed in telecom applications.

TFT's are also often used for displays in car industry, where they are built in the control panel. High quality of these displays is requested, considering the price of the car. Acceptable number of pixel defects is very low. ESD protection is in this application very important [72].

TFT's used for applications in sensors often have some very specific requests. For example, the problem of the capacitive fingerprint sensor is already described in Section 5.3.

A general solution will not be given in this chapter, as the problem with all its variations is too complex, but a number of relevant recommendations that should be taken into account while designing a TFT based ESD protection structure will be given.

6.2 Basic of ESD protection design

A successful ESD solution is not trivial. A number of good individual ESD components should be put together so that they cover all possible ESD zap conditions. Two possible approaches can be used for ESD protection design:

1. Random path approach: To find experimentally (by means of ESD testing + failure analysis) the Random Path of ESD current. When the weakest link is found, the layout is fixed and the new circuit is forwarded to the next iteration of testing and failure analysis. Hopefully, after several iterations of testing and re-designing, one could expect that desired ESD protection will be realized.

2. Current path approach: To provide a designated path by which ESD current can be discharged. The designated path has very low impedance, comparing with the other possible current paths. Designing the current path, it is important that the remaining voltage between the pins is sufficiently low, such that dielectrics are not damaged. This current path usually consists of devices in a working chain. In crystalline devices, a device used in this chain might be either breakdown-type (such as grounded gate MOS) or non-breakdown type device. As amorphous silicon TFT's do not work as breakdown devices (for example, crystalline MOS devices are used in snap-back regime - when parasitic bipolar transistor is switched on and they can handle large current while keeping voltage constant at a certain value), the only possibility is to use non-breakdown devices, which operate near their normal operating regime and are therefore easy to predict and simulate.

In this chapter, we will combine the two methods. First the TFT circuits (LCD) will be tested by means of TLM and the failure analysis will be performed in order to find the random path of ESD current. Further, the TFT matrix will be modelled and simulated in the circuit simulator Pstar. Changing the design in the simulated model, a wanted ESD current path will be created. The current path approach is more designable and systematic, and therefore is considered as better, and in this section we will put more attention on this solution.

6.3 Testing of ESD protection structures in TFT AMLCD's

In this section the results of ESD (TLM) testing on α-Si:H TFT based reflective AM LCD's, manufactured by Philips Mobile Display Systems, Kobe, Japan, will be presented and discussed. The displays are manufactured for

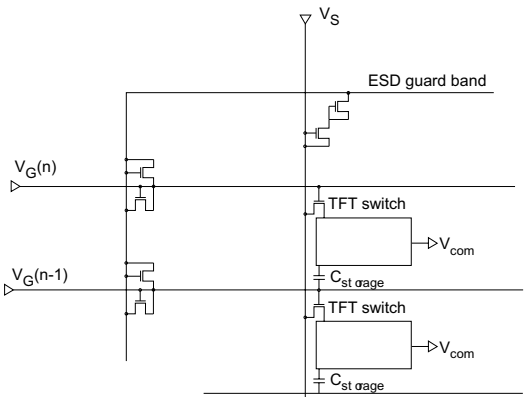

Figure 6.1: Electrical scheme of the display with the protection band type A.

use in telecom applications and handheld computers. One of the major causes for display failures during manufacturing is ESD (1-2 % out of total 10 %). It has been found that the leakage current of the ESD protection ring during normal operation of the display gives rise to power dissipation. Three types of reflective TFT panel are evaluated (A, B, C) in order to find out which one has the best performance from the point of leakage currents and also from the point of ESD protection.

In type A we have two types of ESD protection. The electrical scheme of the display A is shown in Fig. 6.1. The ESD protection of the gate lines consists of a guard band to which all gate are connected via TFT's that have the gate connected to the drain (gate coupled TFT's). The structure has two TFT's that are connected in a parallel connection from the gate line to the guard band. There is one TFT in each direction so that if the potential on a particular line exceeds a certain value one of the TFT's will turn on giving a leakage path. This structure is called "Single TFT, single ring, double sided". A drawback here is that the TFT's turns on at a rather low voltage so that the ESD guard band will give a leakage current, which corresponds to the power dissipation of the order of 1mW in normal operation. The ESD protection of the source lines has two TFT's in a serial connection from the source line to the guard band. A disadvantage of this structure that it provides protection for only one (positive) polarity of the stress pulse. This protection is named "Double TFT, single ring, single sided".

To reduce the leakage current these structures have been modified. In

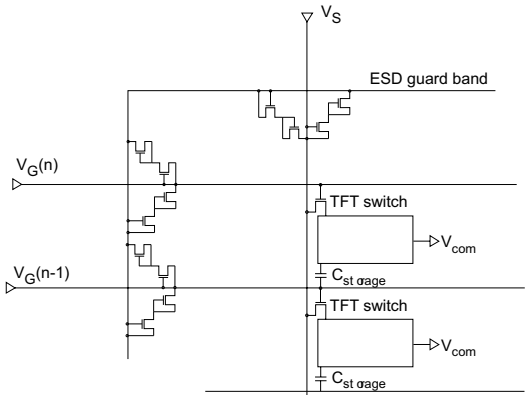

Figure 6.2: Electrical scheme of the display with the protection band type B (double TFT protection between gate or source bus and guard band).

type B two series of two TFT's in a parallel connection are used. The idea is that if the voltage is shared between two TFT's, then during normal operation each of the TFT's will stay off. During an ESD event they will also share the stress, which also can improve the ESD protection. The scheme of the display B is shown in Fig. 6.2. This type of protection is called "Double TFT, single ring, double sided".

Type C splits the guard band into two, as shown in Fig. 6.3. The TFT's between a gate/source bus and the guard band 1 are activated if a positive stress is applied on the bus, and the TFT between a gate/source line and the guard band 2 is activated if a negative ESD stress is applied. This structure is named "Double TFT, double ring, single sided".

Testing of the displays will be carried out in two steps, first the whole display matrixes will be tested in order to find out the breakdown voltage, the failure spot and if possible to determine the random path of ESD current. Second, the ESD protection structures itself will be tested apart of the display matrix in order to clarify their performance under ESD biasing conditions.

6.3.1 TLM testing of the display matrix

All three display types are tested by means of a TLM tester, in order to find out which structure is most effective in suppressing ESD effects. First the results of the testing of the panel will be presented. TLM measurements showed a breakdown voltage of around 380 V. Stressing by means of TLM

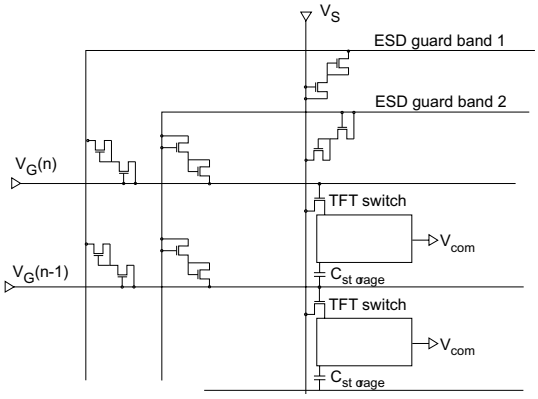

Figure 6.3: Electrical scheme of the display with the protection band type C (double guard band).

voltage was continued long after breakdown in order to make the failure spot clearly visible. The pre-breakdown degradation is not known, as the leakage current measurement did not show any increase prior to the breakdown. After TLM testing was finished, the displays were optically examined in order to find the breakdown spot. After examinations under microscope, it could be concluded that always the TFT protection structures and only in one case the pixel TFT in the matrix are broken down. The conclusion is that the protection structure breaks down first. Only in the case when TLM voltage is continued several times after the breakdown the TFT in the display matrix will be affected.

TLM measurements were continued on the panel B (Double TFT, single ring, double sided). Breakdown voltage was identified by the TLM measurements, but in several cases it was difficult to observe the breakdown spot on the panel. If it was possible, then often the breakdown spot was located not in the TFT active area but at the line crossing between the stressed gate/source line and the guard band.

Finally, the panel C (Double TFT, double ring, single sided) was measured. The breakdown voltage was around 380 V, and the breakdown spot could not be identified in the TFT area, but only at the crossing of the stressed gate/source line and the guard band.

In the measured samples, the breakdown spot is found sometimes in the protection structures, sometimes in the circuit; sometimes in the TFT active area, sometimes in the metallisation lines crossing. One example of

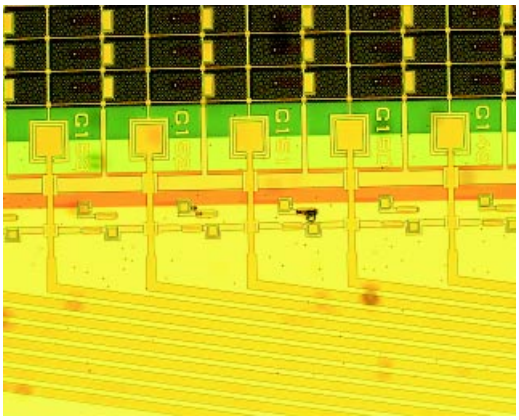

Figure 6.4: Protection structures left and right from the stressed gate line are broken down.

the failure spot (a broken TFT in the protection structure), measured on the display type A, is shown in Fig. 6.4.

The breakdown voltages are at the expected level for the given gate dielectric thickness and the channel length. It implies that the breakdown is dielectric breakdown, which appears either in the TFT active area or at the crossings of the bottom and top metallisation layers (gate and source lines). There is no difference in the protection under the TLM stress between different protection structures in the TLM breakdown voltages. A comparison of measured TLM breakdown voltages is given in Fig. 6.5. The question arises why the pixels in the matrix are not protected for the voltages higher then 380 V. Also, it is not clear why there is no difference in the breakdown voltages whithin the different structures. Whether the ESD structures do not work as they should, or if they do work as planned, then the design of protection is not good. To answer this dilemma, first the protection elements will be tested and second, the design of the ESD protection will be re-considered using Pstar simulations.

6.3.2 Testing of ESD protection structures

The ESD protection structures are tested to study their ESD behaviour without any disturbance of the matrix. The structures are firstly measured with a Parameter Analyser HP4145B in order to determine their regime of working/switching on, and later the protection structures are ESD tested

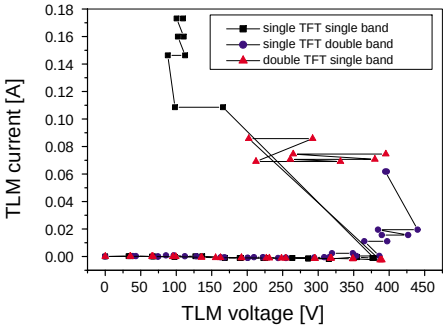

Figure 6.5: Comparison of measured TLM breakdown voltages for protection structures A, B, C.

by means of a TLM tester.

The results of the measurements by means of the Parameter Analyser are shown in Fig. 6.6. The voltage is increased from 0 to 100 V and the current is measured. Usually, when testing protection devices, current is forced, as a snapback cannot be studied in a voltage force mode. For these devices however, there is no snapback. The protection elements from different display types are presented together in order to compare their working. The plot shows that the display type A "Single TFT, single ring, double sided" switches on first and produces the highest current. The current characteristics is degraded (saturated at the level of approximately 1 mA) after 60 V. The display type C "Double TFT, double ring, single sided" switches on also very fast and works well until 80 V when it also starts to saturate. The display type B "Double TFT, single ring, double sided" switches on considerably later, and does not go into the high current regime or saturation.

To have a clearer explanation of working of these ESD protection structures, they were tested in the following way. The stress is applied either on the gate or source line, while the other line (source or gate) was floating, and the protection ring was grounded. In this case we expect to test the protection device itself. The result of the measurements are as follows.

As for the display type A the ESD structure for gate line differs from the ESD protection structure for the source line, therefore the results of testing will be plotted separately for each of this two structures, Fig. 6.7 "Single TFT, single ring, double sided" and Fig. 6.8 "Double TFT, single

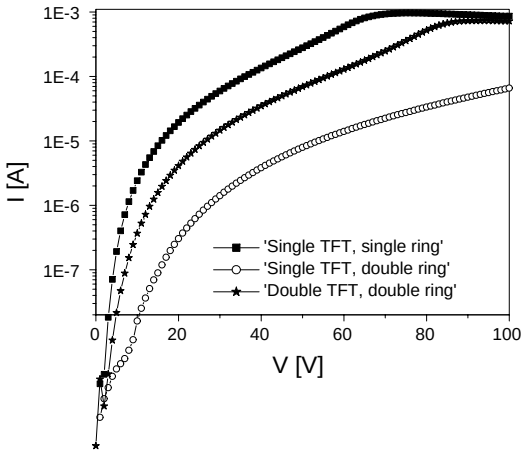

Figure 6.6: Measurements of the protection structures by means of Parameter Analyser HP4145B.

ring, single sided". There is a difference between these two structures in the measured TLM breakdown voltages. The structure with two TFT in series on one side of the source line showed the breakdown voltage of 260 V, and the structure with one TFT connected with its gate and drain and one TFT connected with its source between the gate line and the protection band showed the breakdown voltage of approximately 160 V. Also the leakage currents were monitored during the TLM stressing. The leakage current measured before breakdown from the side of the source line (two TFT in a serial) were in order of $2 \cdot 10^{-11}$ A, and the leakage current measured from the gate side (two single TFT's) were in order of $5 \cdot 10^{-10}$ A.

The display type B "Double TFT, single ring, double sided", has equivalent structures from both gate and source bias line. Therefore only the results of testing protection structures from the source line will be shown. It can be seen from the Fig. 6.9 that the breakdown voltage under TLM stress is considerably higher then in the display A, it is approximately 330 V. The leakage current before the breakdown is in order of $3 \cdot 10^{-10}$ A.

Finally, the display type C, "Single TFT, double ring, single sided" showed a TLM breakdown voltage of 310 V and the leakage current before the breakdown of $3 \cdot 10^{-11}$.

The conclusion from the measured samples is that the single TFT has a lower TLM breakdown voltage then the serial connection of two TFT's. There is a big difference in the measured leakage current as well. A compar-

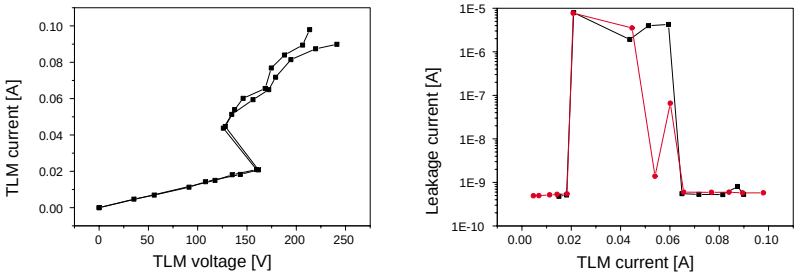

Figure 6.7: TLM current and leakage current measurements during TLM stress on "Single TFT, single ring, double sided" structure.

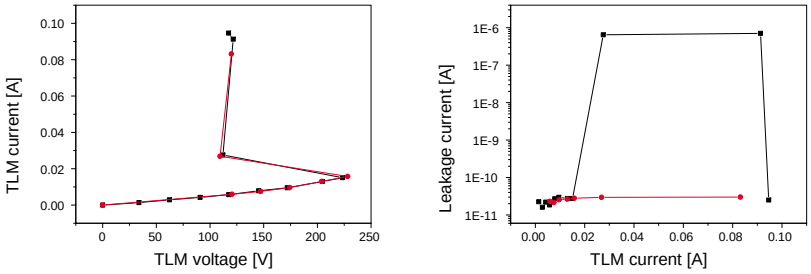

Figure 6.8: TLM current and leakage current measurements during TLM stress on "Double TFT, single ring, single sided" structure.

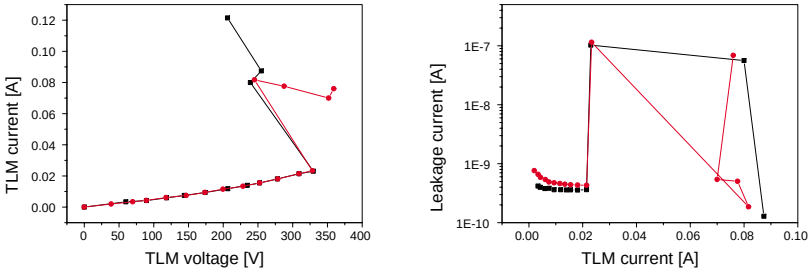

Figure 6.9: TLM current and leakage current measurements during TLM stress on "Double TFT, single ring, double sided" structure.

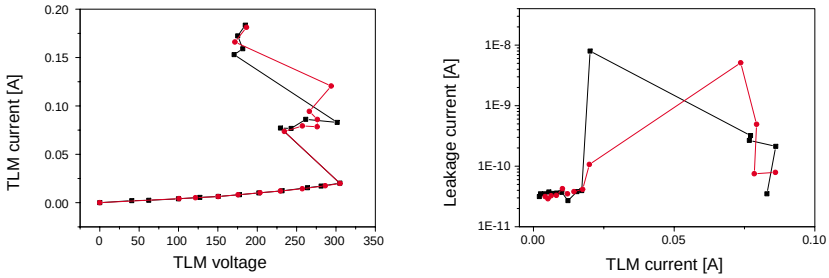

Figure 6.10: TLM current and leakage current measurements during TLM stress on "Double TFT, double ring, single sided" structure.

ison of the results of the TLM testing on ESD protection structures isolated from the display matrix is shown in Table 6.1.

ESD protection structure	Breakdown voltage under TLM	Leakage current (between TLM pulses, before breakdown)	Turn-on voltage (corresponding $I = 100\mu A$)
1. SSD	160 V	500 pA	25 V
2. DSS	240 V	20 pA	36 V
3. DSD	330 V	300 pA	120 V
4. DDS	310 V	30 pA	56 V

Table 6.1: Comparison of ESD protection structures. Structure 1. SSD: Single TFT, single ring, double sided; Structure 2. DSS: Double TFT, single ring, single sided; Structure 3. DSD: Double TFT, single ring, double sided; Structure 4. DDS: Double TFT, double ring, single sided.

If we now compare the breakdown voltages of the tested ESD protection structures (Table 6.1), we can conclude that the breakdown voltages of the structures 1, 3 and 4 fulfil the expectations, as the single TFT structure (1. SSD) has the lowest breakdown voltage. Two TFT's in series (structures 3. DSS and 4. DDS) have a breakdown voltage that is almost two times higher (that is desirable and as expected). Surprisingly, the breakdown voltage of the structure 2. DSS does not obey the rule:

$$V_{BR}(\text{TFT chain}) = \text{No. TFT's} \cdot V_{BR}(\text{single TFT}) \tag{6.1}$$

The breakdown voltage here is decreased due to some influence of the par-

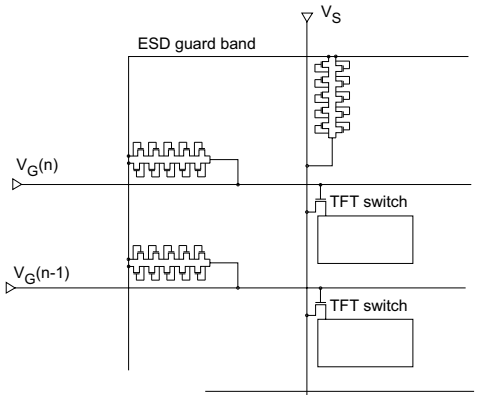

Figure 6.11: TFT's chains in the fingerprint sensor.

asitic structures, as we know that the TFT's are the same in all structures.

Of course one wants to have the breakdown voltage as high as possible and increasing the number of TFT's we could improve it, but increasing the number of TFT's would also lead into the same increase of the turn-on voltage. In other words, one wants to have turn on voltage optimised: it has to be higher then the display operational voltage (otherwise the leakage is too much), but on the other side not too high.

The leakage current, measured at 20-25V (operational voltage for the display), should be kept as low as possible, as mentioned earlier. It can be noticed that the excessive leakage comes always from the symmetric chain. Actually, if the symmetric chain is split in two guard rings, the leakage is dramatically decreased. It is not quite clear why the leakage is related with the design/geometry of basically the same protection structure, but it is clear that the leakage can be avoided simply by separating the chains.

6.4 Testing of TFT chains in fingerprint sensor

Chains of five TFT's in a serial connection (Fig. 6.11) are used for each row and column protection. The chains are connected to a single guard ring [1]. Single protection chains were designed on the test part of the sensor. The chains were built in three variations of TFT's, with channel width and length of $160\mu m/64\mu m$, $80\mu m/32\mu m$ and $40\mu m/16\mu m$. The chains were tested,

[1]The structure described in this section belongs to the same fingerprint sensor as described in the section 5.3.

applying the stepped voltage up to 100V on the one side of the chain, having the other connection grounded. The result of the measurements is shown in Fig. 6.12.

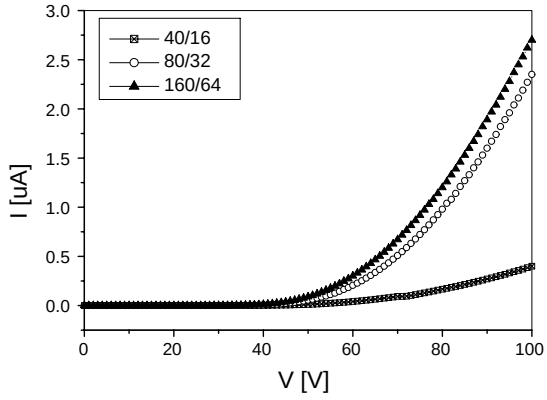

Figure 6.12: Measured characteristics of TFT's chains with different channel widths and lengths.

From the Fig. 6.12 it can be seen that all of the three chains switch on at about the same voltage of 40 V. That is consistent with the measured threshold voltage of a single TFT. The larger TFT's produce a higher current under the same voltage. The current is in the order of μA.

6.5 ESD stress on the gate of α-Si:H TFT's

In addition to the experiments with the ESD protection structures already presented in this chapter and to the experiments on the drain of a single TFT presented in Chapter 2, experiments with TLM stress on the gate of a single TFT are performed for the sake of clarity of the ESD event in a TFT circuit. When a TFT is exposed to an ESD stress, the zap comes either on its drain/source (TFT's are symmetrical from this point of view) or on the gate. Stressing on the drain is already explained in the previous chapters and in this section ESD stressing on the gate will be investigated.

TFT's with the channel width and length of $100\mu m/20\mu m$, $75\mu m/15\mu m$ and $40\mu m/8\mu m$ were tested by means of TLM. Between the stresses the transfer characteristic was measured. The results of these measurements

are shown in Fig. 6.13 for a series of TLM stress of 500ns applied on a TFT with W/L=100μm/20μm. Any W/L could have been taken as the graphs are all the same. Apparently the behaviour of tested TFT's does

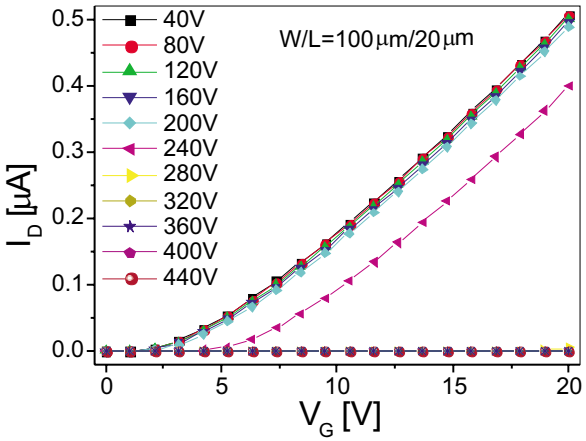

Figure 6.13: Transfer characteristics of the TFT with W/L=100μm/20μm monitored during a TLM series on the gate.

not depend on the channel width or length. Namely, TFT's with different channel widths and lengths gave the same response under the TLM stress on the gate. This result is logical and was expected. If a TLM stress is applied on the gate, while the drain and the source are grounded, there is no drain current in the channel. On the other side, due to the high gate voltage, the electric field in the gate insulator is high. If the electric field exceeds the critical value the dielectric starts to leak and if the field is increased further it breaks down. In SiN_x the critical field when the leakage current sets in is 4-5 MV/cm and the breakdown field is 12 MV/cm. In our TFT's it means that under 240 V TLM stress on the gate the wearing-out of the dielectric sets-in, and the dielectric breaks down at 320 V TLM stress on the gate. These voltages do not depend on the channel length and width but only on the gate thickness.

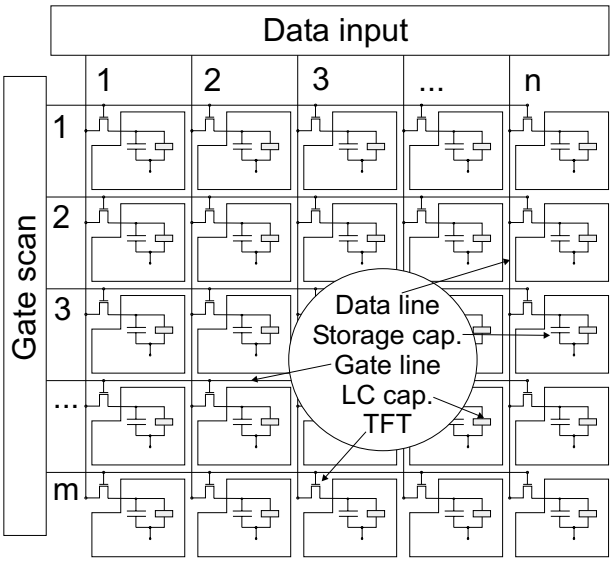

Figure 6.14: Schematic diagram of a TFT LCD.

6.6 Discussion on improvement of TFT based ESD protection

6.6.1 Modelling and simulation of TFT displays for ESD performance

The electrical response of the TFT LCD's without and with ESD protection under ESD stress will be modelled and simulated in this section. An imaginary TFT display is analysed, as presented in Fig. 6.14. It has n columns (data lines) and m rows (gate lines). Therefore $n \times m$ pixels of which each has a TFT, a storage capacitor C_s and a liquid crystal capacitor C_{LC}. The storage capacitor may be present but it does not have to, as it is intended to improve the retention characteristics of the signal charge [71]. It can be found in literature in two variations, as from the pixel to the ground or from the pixel to the gate line [38]. The display operates one line at a time - video signals are fed to the data lines simultaneously through a data buffer during the gate turn-on time. The scan voltage pulse applied to a certain (say, i-th) gate line opens the gates of the TFT's connected to the line. The signal voltage is then applied to the pixel electrode of each dot on this gate line.

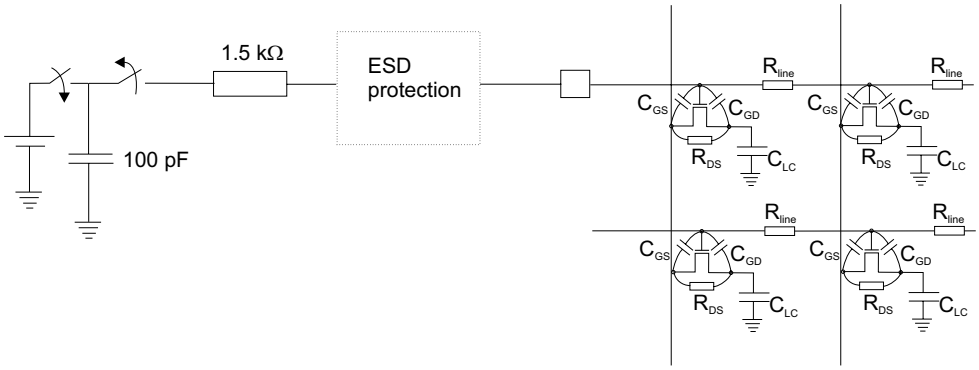

Figure 6.15: Human body model testing of a α-Si:H TFT circuit.

To start to analyse a TFT display on the ESD performance, we will add a modul of an ESD tester, as commonly used in the IC industry, to the TFT LCD. The ESD test most commonly used in industry is human body model. As it was already explained in 2.1.1, a 100 pF capacitor is charged by a voltage of a few kV, typically 2 kV, at most 6 kV, and through a resistor of 1.5 kΩ, which represents the skin of a human, it is discharged to the electrical circuit under test. The current response is determined by the equivalent resistance and the capacitance of the circuit, but the peak current under 2 kV HBM stress can not be higher than 2 kV/1.5 kΩ=1.33 A. The goal of ESD protection is to make the circuit able to withstand this current. The way how the protection is built develops with the development of IC processes. In the IC's with the channel length $l < 0.25\mu m$ the main protection element was a grounded gate (gg)MOS transistor in the snapback mode. When in the snapback mode a typical ggMOS is able to withstand the 1.4 A current holding the voltage fixed at $10 - 12V$. But it was proven in Chapter 2 that a ggTFT does not work in this way. It does not hold the voltage and can not be used in this way. Therefore the knowledge of the ESD protection in IC's can not be applied in a TFT display.

What happens if we apply the same HBM to an α-Si:H TFT circuit? This situation is shown in Fig. 6.15. We assume we deal with a small circuit of 250×250 pixels, and a HBM voltage of $2kV$. We also assume that the pixel capacitance is $1pF$. At this point we will neglect the storage capacitance. The parasitic capacitances of the gate/source and the gate/drain overlapping area and the intrinsic TFT capacitance are assumed to be $100fF$. Therefore the total capacitance from the gate line to the ground is a serial

connection of C_{TFT} and C_{LC}, $C_{pixel} = \frac{1}{1/C_{TFT}+1/C_{LC}} = 90fF$. The total capacitance of the line under test would be a parallel connection of 250 pixel capacitances with $C_{tot} = 250 \cdot 90fF = 2.27pF$. For start, let's assume that resistance of the metal line is zero. Therefore the voltage of 2 kV from the HBM capacitor of $100pF$ would be distributed between the human body capacitance and the equivalent capacitance of the matrix. The voltage in the matrix would be equal to:

$$V_{pixel} = \frac{C_{HBM}}{C_{tot} + C_{HBM}} \cdot V_{HBM} = 1.95kV \tag{6.2}$$

This is an approximation of the voltage stress that comes to a pixel if there is no current shunted to the ground. In most often case the number of pixels in a row is much larger which means that the voltage on a pixel would be less. Still, the current through the circuit is too low to provide a sufficiently high voltage drop on the human body resistor, and the voltage on the line under ESD zap is too high. A current discharge element is needed, or another way to reduce the voltage. Obviously the problem is not simple and the parasitics may not be neglected. To answer this question electrical simulations are performed and the current of the TFT during and ESD stress is calculated. The resistance of the metal line must not be neglected. In this way a transmission line is created which has a very long delay time. The pulse propagates down the gate line which is represented by the $C_{pixel}R_{pixel}$ circuit, and the rectangular input pulse is delayed and distorted as it travels along the gate busline [71]. The gate delay is defined as the time when the pulse height at the end of the line reaches 90% of the input pulse amplitude and it depends on the length of the gate line l_g by the equation:

$$t_d \approx RCl_g^2 \tag{6.3}$$

The first pixel is therefore first exposed to the ESD stress, and the last pixels are in this way protected. The prediction is that under the ESD stress the most of the failures is located in the first columns. This is actually confirmed by experiments on the thin film diode displays [4]. It also could be confirmed by means of electrical simulations.

Estimation of parasitic elements

For the electrical simulations an estimation of parasitics of both the metallisation and the TFT's will be introduced. From the modelling point of view, wires have three important characteristics: resistance, capacitance (electrical energy) and inductance (magnetic energy). Wires are represented as a

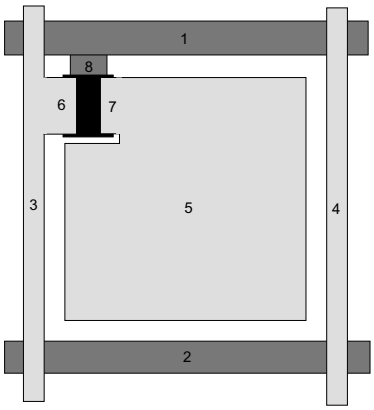

Figure 6.16: Layout of a pixel. 1 and 2 - bottom metallisation, 3 and 4 - top metallisation, 5 - pixel plate, 6 - source, 7 - drain, 8 - gate.

distributed RC(L) circuit. Inductance effects are very small and it is mostly ignored. However, it can be important for noise and it will be also included in the ESD simulations. Modelling of an active TFT matrix consists of two sub-models, the pixel cell model and the model of the TFT switch itself [2]. A model of the TFT for use in circuit simulators has been given by Shur [26], [53].

In Fig. 6.16 a schematic of an imaginary pixel is shown. From Fig. 6.16 it can be seen which parasitic elements are present. The total active area is $100 \times 100 \mu m$. In Fig. 6.16, 1 and 2 are gate lines (bottom metallisation layer - light gray), 3 and 4 are source lines (top metallisation layer - dark gray), 5 is pixel plate, 6 and 7 are the source and the drain of the TFT switch, respectively and 8 is the TFT's gate. In this analysis, only the most important parasitic elements will be considered. Parasitics consisting of structures obliquely to each other and effects between structures more than one pixel away are not considered. The main effects are the resistance of 1, 2, 3, 4, 5, 6, 7, the inductances of 1, 2, 3, 4, and the capacitances 3-5, 5-4, 6-8, 8-7, 1-3, 1-4, 2-3, 2-4. Unfortunately, it is not possible to measure most of the parasitics. Therefore, they will be estimated by calculation.

As first, the resistance of the aluminium and molybdenum/chromium lines is estimated. Resistance is the easiest to calculate as the current is confined to the material. The intrinsic resistance is pretty small, unless if we think about very long lines. The value of the resistance of the bottom

Al wires is estimated from the equation:

$$R_{pixel} = R_{\square}\frac{l_{pixel}}{w_{\text{Al line}}} = 1.5\Omega \tag{6.4}$$

where $l_{pixel} = 50\mu m$ is the length of the metal line between two pixels, $w_{\text{Al line}} = 8\mu m$ is the line width. The sheet resistance of the aluminium line is $R_{\square} = 0.12\frac{\Omega}{sq}$. The parasitic resistance of the source bus is estimated in the similar way to value of $R_{bus} = 40\Omega$. The drain bus is made of MoCr, which has sheet resistance of $R_{\square} = 1.6\frac{\Omega}{sq}$, and the width of the line is $w_{\text{MoCr line}} = 4\mu m$. The resistance of the pixel plate is 6Ω.

The inductive coupling is much more complex to analyse. Inductance calculation is based on Maxwell's equation. The estimate is very difficult because it depends on where the currents flow. But the problem in this case will be reduced, because the inductances are not expected to have much influence in this analysis. The self inductance of a straight conductor with depth small compared to the length and width can be approximated by [63]:

$$L = \frac{4\mu_{m0}}{D}\pi[sinh^{-1}(\frac{l}{w}) - 1] \tag{6.5}$$

where μ_{m0} is magnetic permeability of free space $4\pi 10^{-7} H/m$.

The capacitance coupling is mostly a nearest neighbour issue. The parallel plates approximation can be used in most of the cases (always when the dimensions of the plates are larger then the distance between them).

$$C = \frac{\epsilon_0\epsilon_r}{d}S \tag{6.6}$$

Fringe capacitances will be neglected in this model.

Other parasitics come from the TFT itself. These are the parasitic capacitances (overlap between the source/gate and the drain/gate) and the parasitic resistances (series resistance of the source and the drain). The dimensions of the TFT switch are: channel length 20 μm and width 6 μm, gate dielectric thickness 330 nm, gate/source and gate/drain overlapping area 2 μm, threshold voltage $V_T = 2$ V, electron mobility $\mu_0 = 1cm^2/Vs$. Gate/bulk capacitance is neglected as there is no bulk contact, plus the value is not much higher then the overlapping capacitances, and it can therefore be assumed that it would not change much the simulation results.

In Table 6.6.1 the names of the parasitics are indicated and the calculated values are given. The model of the circuit consisting 3 rows and 3 columns is presented in Fig. 6.17.

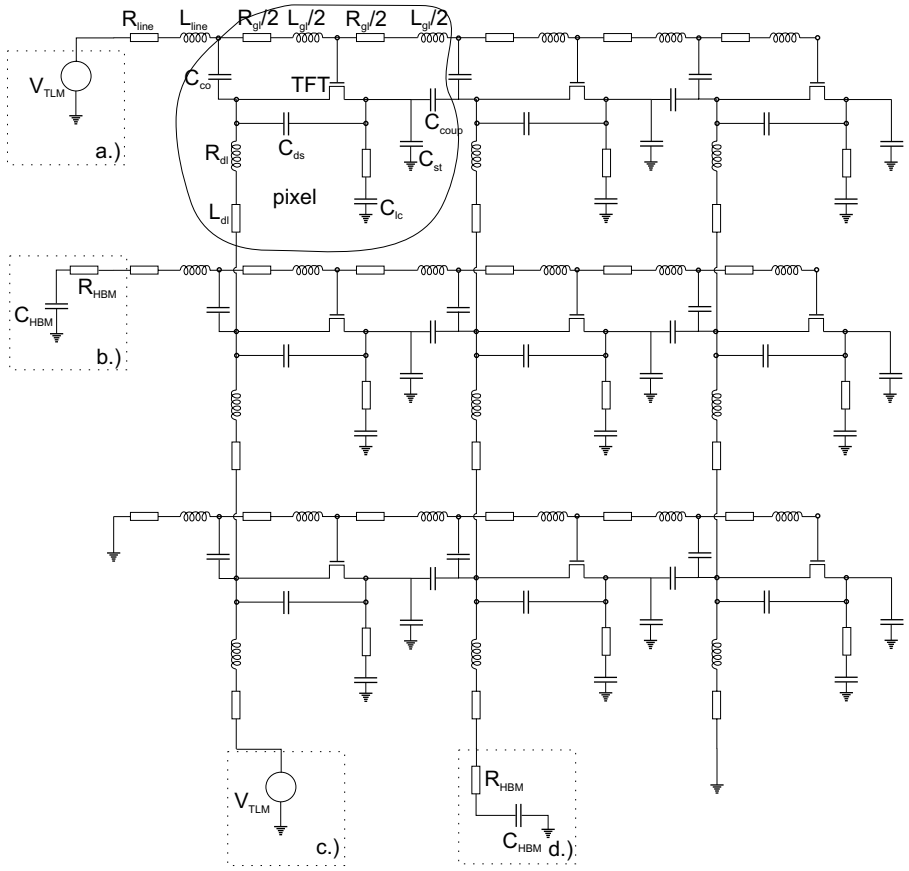

Figure 6.17: Equivalent circuit of a circuit with 3 rows and 3 columns. a.) TLM generator connected to the gate line. b.) HBM to the gate line. c.) TLM to the source line. d.) HBM to the source line.

Name	Explanation	Value
R_{gl}	resistance of 1,2	1.5 Ω
R_{dl}	resistance of 3,4	40 Ω
L_{gl}	inductance of 1,2	177 pH
L_{dl}	inductance of 3,4	232 pH
C_{co}	cap. between 1 and 3,4	6.3 fF
C_{ds}	cap. between 3 and 5	4 fF
C_{coup}	cap. between 5 and 4	5 fF
R_{pix}	res. of pixel plate	6 Ω
C_{st}	storage capacitor	1.5 pF
C_{LC}	liquid crystal cap.	127 fF
C_{GDO}, C_{GSO}	TFT overlapping cap.	8.26 fF
R_d, R_s	drain and source serial res.	8.5 Ω
R_{line}	res. of long input line	10 Ω
L_{line}	ind. of long input line	500 pH

Table 6.2: Specific parasitics of one pixel, names and values.

Electrical simulations of a TFT LCD without ESD protection

Simulations have been executed with Pstar. Simulations of TLM and HBM have been carried out on the model shown in Fig. 6.17. If the ESD pulse, either TLM or HBM, was supplied to one of the rows/columns, all other rows and columns were grounded.

The results of the simulations are shown in the following pages. Firstly the results of the simulation by means of TLM are given. The stress duration is 100 ns, with the rise/fall time of 5 ns. The results are presented through:

- Drain current of the TFT's.
- Propagation of the voltage along the row (TFT's gates nodes).
- Propagation of the voltage along the column (TFT's drain nodes).

In Fig. 6.18 the results of the simulation supplying a positive TLM voltage on the first row are shown. From Fig. 6.18 it can be concluded that the current through TFT's in the first row is almost equal, it is rather high during the stress rise and fall time (2 mA) and it is decaying from 0.5 mA to 0 A during the stress. This level of current is rather high for a TFT. The currents in all other rows are zero. Considering the voltage propagation along the row under stress, we can conclude that the stress voltage is almost

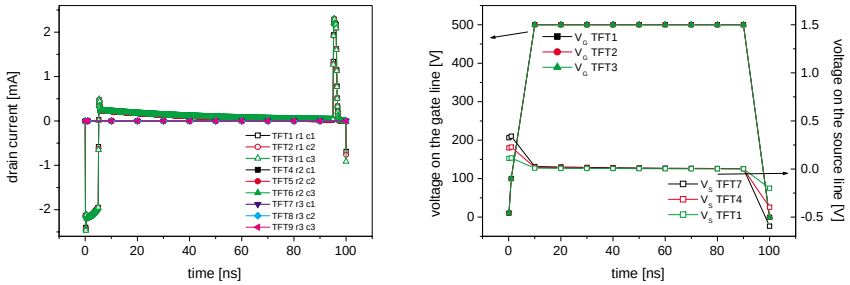

Figure 6.18: TLM testing on the gate line of a α-Si:H TFT circuit.

equal along the row, it is 500 V, as the delay can not be noticed in the row consisting only 3 pixels. The level of voltage is catastrophically dangerous for the TFT's dielectric. This will not change if the row would contain even several hundred pixels. Under this level of voltage a TFT would have to breakdown. The propagation of the voltage along the drain line is also shown in Fig. 6.18. The voltage is distributed along the line but the level is very low (< 600 mV) and can not be harmful for the circuit.

In Fig. 6.19 the results of the simulation with negative TLM voltage are given. The current of the TFT's is only during the stress rise/fall time, during the pulse the current is zero. That is because the gates are under negative voltage. The voltage along the row under stress is constant at -500 V. The same conclusion is that the gate dielectric breakdown can be expected. Along the columns the voltage is zero, except for the rise/fall time.

If a positive TLM voltage supply is connected to the source line, the results are slightly different. The current appears only in the TFT's in the column under stress, and only during the rise time, during the fall time the gate is biased negatively and there is no current. The level of the current is high (-170 mA). The voltage along the rows appears only during the stress rise/fall time. The voltage along the column propagates with a reasonable delay, as the parasitic resistance of the source line is rather high comparing to the gate lines. The level of the voltage along the column is 500 V.

If a column is stressed by a negative TLM stress then the situation is opposite and similar with the results of the simulation with positive TLM stress on the gate line. The TFT is working under stress producing the drain current of approximately 10 mA. The voltage on the source line is 500

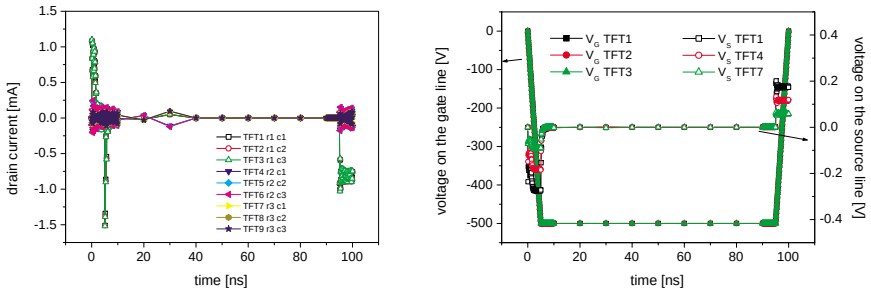

Figure 6.19: TLM testing on the gate line of a α-Si:H TFT circuit.

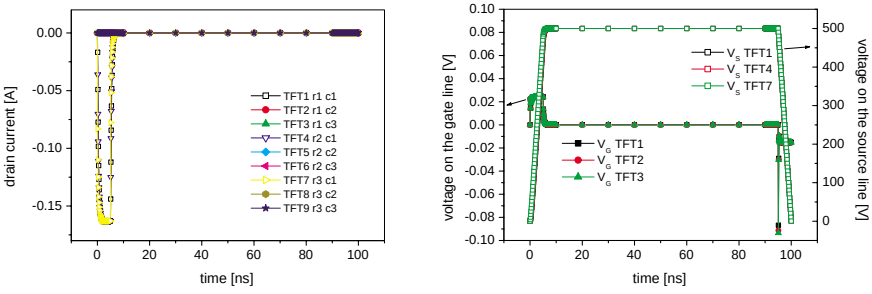

Figure 6.20: TLM testing on the source line of a α-Si:H TFT circuit.

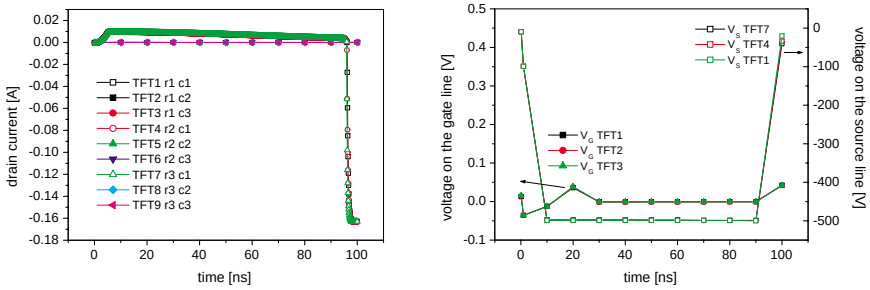

Figure 6.21: TLM testing (negative voltage) on the source line of a α-Si:H TFT circuit.

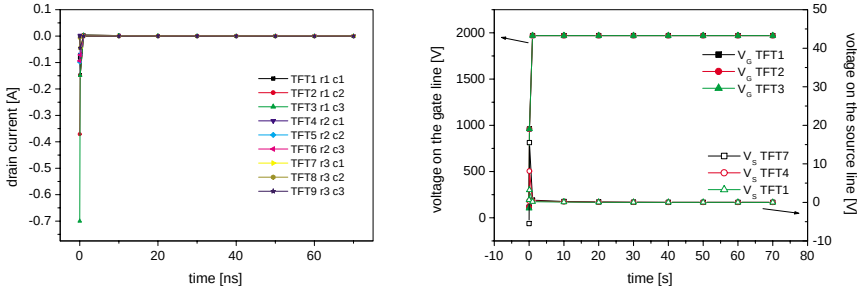

Figure 6.22: HBM testing on the gate line of a α-Si:H TFT circuit.

V.

If HBM stress is supplied to the gate line, through a capacitor of 100 pF pre-charged with 2×10^{-7} C (2 kV) and a resistor of 1500 Ω then a situation as presented in Fig. 6.22 happens. Full discharge of the HBM capacitor is not possible as there is no current path to the ground in the circuit. The voltage is redistributed and the voltage on the gate line is almost equal to 2000 kV, as the equivalent capacitance of the matrix is very small compering with 100 pF HBM capacitance. The peak current through TFT's is -155 mA.

If the HBM capacitor is connected to the source line, the decay time is longer, as the source line has a larger resistance, as shown in Fig. 6.23. The peak current in the TFT's is also higher (-600 mA) and the voltage

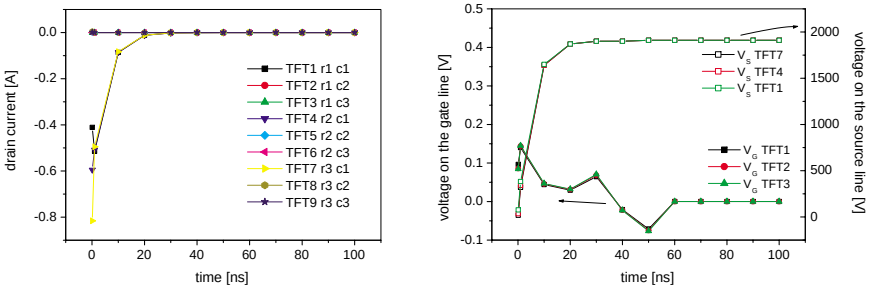

Figure 6.23: HBM testing on the source line of a α-Si:H TFT circuit.

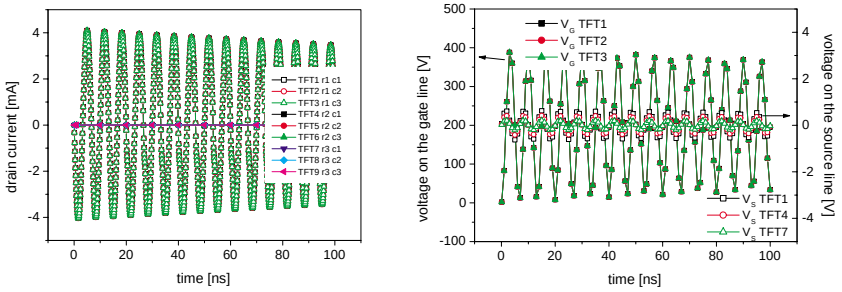

Figure 6.24: MM testing on the gate line of a α-Si:H TFT circuit.

distribution is slightly different. The voltages along the stressed source line are 1900 V. If the Machine model (MM) is used to test the gate line, the distribution of the currents and voltages in the circuit is as shown in Fig. 6.24. In the MM a capacitor of 200 pF is charged up to 200 V and through a inductor of 7.5 μH is discharged to the circuit. The voltage on the stressed line rises up to 400 V, which is above the breakdown voltage. Clearly some protection is needed.

Simulations with protection elements

Finally a simulation of the LCD with the protection as used in the tested samples is given. The chosen type of protection is "Double TFT, double sided, single ring". The results of the simulation with a positive TLM stress

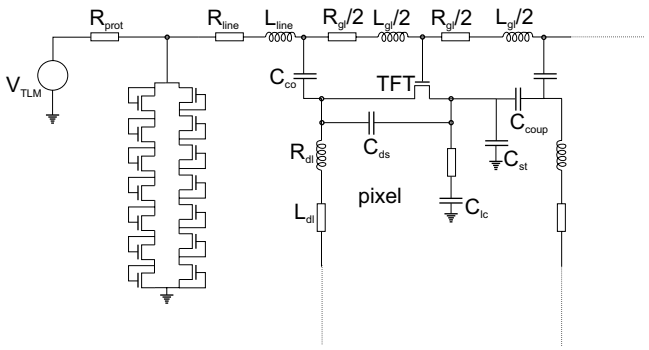

Figure 6.25: Schematic representation of ESD protection structure.

on the gate line are repeated on the circuit with ESD protection. The results are compared with Fig. 6.18 and they are completely the same. Apparently the protection element does not have any impact on the circuit response under an ESD stress. The TFT's in the ESD protection structure do switch on under the ESD stress, and they conduct certain level of current. This current has not any effect on the final voltage on the line. The resistance of the line is too low to produce sufficient voltage drop along the line.

The conclusion from these simulations is that the most important issue when designing an ESD protection in TFT LCD's is to find way to reduce the voltage along the stresses gate/source line, as this is the most dangerous issue that appears during an ESD event in AMLCD's. A resistor has to be introduced along with the TFT chain in the way as shown in Fig. 6.25.

A simulation of TLM stress with ESD protection as in Fig. 6.25 is shown in Fig. 6.26. The value of resistor R_{prot} is chosen at 200 Ω. In Fig. 6.26 both the stress voltage of TLM voltage generator and the voltages along the row under stress are shown. It is clear that the voltages on the TFT's gates are dropped down to 150 V, which is under the edge of breakdown. In this way the TFT's are fully protected from the TLM stress of 500 V. In order to protect the circuit from a higher voltage, the value of resistance R_{prot} should have been enlarged.

Unfortunately the drawback of this protection is that the leakage currents of the protection TFT's would cause a drop of the voltage along the line during the normal operation too, and a leakage current itself is detrimental in battery operated equipments (displays in mobile phones are always on, even in the standby mode). For example, if the leakage current of the chain is 0.01 mA (thinking of 1000 rows/columns each with a protection

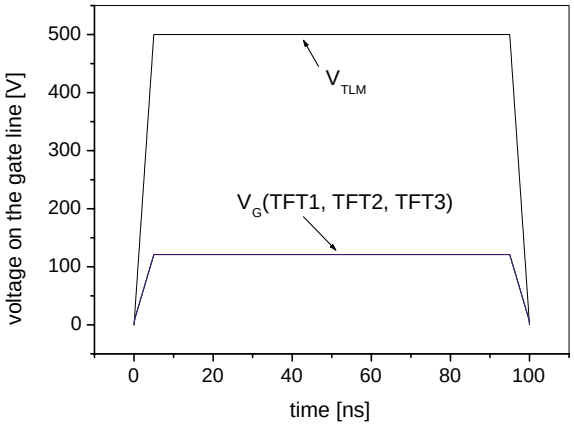

Figure 6.26: Voltage propagation along the stressed gate line with $R_{prot} = 200\Omega$ and $V_{TLM} = 500V$.

TFT chain), we can expect to see a voltage drop of $\Delta V = 200\Omega \cdot 0.01$ mA= 2 mV. In some applications, like automotive or TV/computer screen, that does not give problems, but in the mobile phones that could be a strong disadvantage.

If HBM stress is supplied, the TFT chain offers in this case quite enough ESD protection, as the resistance of the human body model itself (1500 Ω) is enough to suppress the voltage along the line. If the human body capacitor is charged up to 2 kV, then the voltage on the TFT's gates in the stressed row has its peak at 60 V. The resistor $R_{prot} = 200$ V in series with $R_{HBM} = 1500$ kV has only marginal influence. It has to be noted here that the simulated TFT's have an increased electron mobility and therefore they conduct a much larger current then the real α-Si:H TFT's.

If we consider Machine Model (MM), simulating handling by equipment (robots, testers, transportation equipment), as explained earlier in 2.1.1, then the situation is again similar with the TLM. The resistance of the MM is zero, but there is 0.75 μH inductor in series, and the resistance R_{prot} is needed to provide the voltage drop. The voltage distribution along the row under MM stress with the protection chains and the protection resistor is shown in Fig. 6.27. If the value of 200Ω is chosen for R_{prot}, the circuit would be able to withstand the MM stress of 200 V, which is standard for this test, and even much higher MM stress.

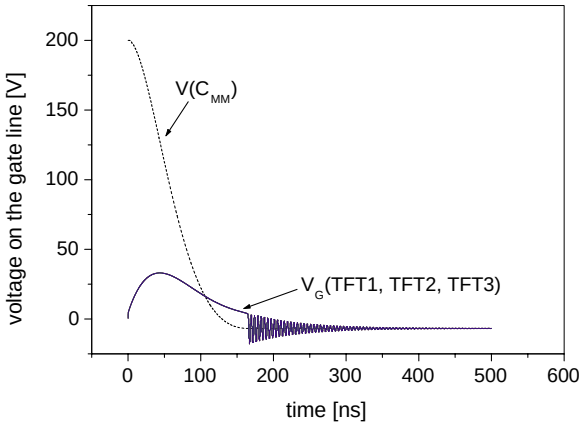

Figure 6.27: Voltage propagation along the stressed gate line with $R_{prot} = 200\Omega$ and $V_{MM} = 200V$.

These simulations are providing a good explanation of the real ESD event, but still, many parameters are only approximated and can not be used directly for the ESD design. For example, the ESD protection of the displays tested in Section 6.3.2 conduct a current of only 0.02 A when stresses by 300 V TLM stress. If we assume that HBM stress is supplied, with 2kV HBM voltage. To provide a voltage drop of 1.7 kV, (so that the circuit would be supplied with 300 V, which is bellow the breakdown voltage and would produce the current of 0.02 A) we need a resistor of $R = 1700V/0.02A = 85k\Omega$ and may influence the proper operation of the matrix although the matrix gives only capacitive loading. This is a quite large resistor and it would be difficult for realisation. The best way is to increase the current of the TFT chain by factor 10, using the TFT in the chain with W/L ration 10 times larger then currently used, and the protection resistor of 8.5 kΩ. This resistor would be easily realised with ITO transparent metallisation layer, which has a very large sheet resistance ($500\ \frac{\Omega}{sq}$).

It is obvious that the design of ESD protection has to satisfy many requirements to be efficient under different ESD tests. The solution that will respond satisfactory well under all ESD tests would be ideal. Among all possible solutions one that would give the best response under the test which is the most adequate for a specific application would be the favourite. It is

our assumption that for large displays the best ESD test would be Charged device model (CDM). The reason is that the large glass substrate becomes easily charge during the fabrication process. On another hand, the displays are during their operation integrated in components, which are normally ESD protected, and they are very rarely exposed to external ESD stress. The glass substrate can be represented as a large capacitor connected to the TFT circuit charged up to certain level, which will be discharged as soon as the circuit touches the ground.

6.6.2 Improvement of TFT chains

The conclusion from the previous section is that TFT chains are very important element for design of ESD protection for TFT displays. Improving the TFT chain would reflect on the quality of ESD protection. The most important parameters of the TFT chain are: turn-on voltage, on-current, leakage current, turn-on time. These parameters have to be optimised for a specific application. Few remarks could be given for that purpose.

How many TFT's? It is a question of the breakdown and the turn-on voltage. One TFT in the chain is too little, as it has the turn-on voltage low and the leakage current therefore high. For the leakage current and the breakdown voltage is recommended to have as much TFT in the chain as the breakdown voltage allows. Therefore, if the TFT display can tolerate a stress voltage as high as 50 V without damage, and if the TFT's have the threshold voltage of 5 V, then as much as 10 TFT's in the chain would be recommended.

Which W, L? Reducing the channel length under 9 μm the breakdown voltage of the TFT's in the chain reduces too, which can produce an increase of the leakage current and in this way disturb the operation of the TFT display. Therefore it is recommended to have the length of at least 9 μm. As for the channel width, increase of the W/L ration will produce in increase of the current of the chain, which may be of importance for the voltage drop on the protection resistor, or human body resistor.

Symmetrical chain? Symmetrical chain is proved to give an increase of the leakage currents and therefore it is recommended to split the guard band in two in case if the size of the protection is not important, as it consumes some more space on the glass substrate.

6.7 Summary

As a first step to the development of design guidelines for ESD protection of TFT LCD's, the sensitivity of TFT LCD's with four different protection structures was investigated by means of a TLM tester. The results showed that the four different ESD protection structures did not produce any difference in TLM sensitivity of TFT LCD's. Therefore, testing was continued by testing the ESD protection structures only, isolated from the TFT LCD's. The four ESD protection structures showed variations of the TLM breakdown voltage, which were in all cases lower then the previously measured TLM breakdown voltage of the TFT LCD's. It was concluded that the ESD protection do not have impact on the TLM response of the displays. The only effect of a broken ESD protection could have been detected in the TLM curve of the display as a very small increase of the TLM current.

To find out why different ESD protections do not produce difference in the displays TLM sensitivity, a TFT LCD display has been modelled and simulated by means of a circuit simulator. The TFT LCD has been simulated with and without ESD protection structure, and on HBM, MM and TLM stress. The circuit parameters used in the model have been estimated for an imaginary TFT LCD. Therefore there is a difference between the measured and simulated ESD sensitivity levels. Still, the simulation helps to explain the behaviour of the tested displays under the TLM stress. It was found that the ESD protection structure based on a TFT chain only, as in the tested TFT LCD's, does not act as a protection under ESD stress. The structure has to be improved introducing a resistor in series to the data line, which would be large enough to provide a sufficient voltage drop, such that the voltage on the line never exceeds 300 V.

Finally, it was analysed how a protection structure can be optimised, in sense of an improved TFT chain in series with an optimised resistor.

Chapter 7

Summary and recommendations

7.1 Summary

Although amorphous silicon thin film transistors (α-Si:H TFT's) have a very low electron mobility and pronounced instabilities of their electrical characteristics, they are still very useful and they have found their place in the semiconductors industry, as they possess some very good properties: they can be deposited under low temperature and over a large area, and they are very cheap. It is proved from practice that electrostatic discharge (ESD) is one of the most important issues in thin film electronics. It jeopardises reliable operation of thin film transistors, firstly during the manufacturing process in the cleanroom, and also in some cases during their operation. Having a large on-resistance, α-Si:H TFT's are very difficult from the point of ESD protection, as it is difficult to sink the current. Another difficulty for the ESD protection is that they are also built on an insulation substrate. Finally, the testing methods and the design rules that are already developed for the silicon integrated circuits are not applicable on the amorphous silicon TFT's. Therefore an original design has to be created in order to protect TFT circuits from the electrostatic discharge.

This work addresses the study of electrostatic discharge stressing in thin film transistors. Therefore, coupled gate α-Si:H TFT's have been exposed to various experiments with ESD, in order to analyse their behaviour under ESD stress. It was established that "soft" degradation appears prior to breakdown. This soft degradations is visible through a threshold voltage shift (decrease). This consequently implies a leakage current increase. This

degradation is due to ESD stress created states in the amorphous silicon band gap. It was also shown that the breakdown voltage is linearly dependent on the channel length in short-channel TFT's, and that it is constant for the channel lengths longer then 9 μm. Breakdown in long TFT's is due to a high electric field in the gate insulator. In the short TFT's punch-through and avalanche breakdown occurs.

Self-heating in the TFT's with different channel lengths and also under ESD stress of different pulse duration has been simulated. It is proved that short channel TFT's suffer from the effect of self-heating, while in long channel TFT's that it is reduced. The time needed to reach a temperature equilibrium in a TFT is around 15 μs. Pulses shorter then this (ESD pulses) will not induce as large effect of self-heating as the long ($> 15\mu s$) ones.

A good example is a fingerprint sensor which has to be able to deal with the static charge accumulated in a human body. A sensor has been design and manufactured. The effect of ESD has been analysed.

Finally ESD stress in a real TFT circuit has been tested and evaluated. The general conclusions are:

- TFT's in a grounded gate configuration do not show a useful snap-back regime. Catastrophic (thermal) breakdown of the gate dielectric happens at dielectric breakdown voltages, which implicitly means that further circuits are not protected.

- TFT's used as diode in a chain have to be used in series with a resistance. Its function has to be optimised in order to decrease the voltage in the circuit below 300 V. Therefore the TFT's used in chain have to be designed to conduct as large current as possible.

7.2 Recommendations for future research

There are plenty issues that need more attention designing ESD protection structures for AMLCD's, or other TFT based devices. Design rules from already developed ESD protections in IC technolgy are often simply translated in thin film technology. In practice, these ESD protections in thin film technology, often based on only one, very simple and surely not satisfactory ESD protection device, a TFT/diode chain, does not provide sufficient level of protection.

Testing of single TFT's behaviour under ESD stress showed that TFT's with a longer channel length have higher breakdown voltage. This property should be kept in mind when designing protection structures. ESD

protections with optimised TFT's should be manufactured and tested. To further improve the breakdown voltage, special high voltage TFT's with the drain extension could be built. Increase of the channel length in protection TFT's must be followed with an increase of the channel width. To increase the current by a larger W/L ratio, wide channel TFT's should be used.

ESD protections in AMLCD's has to be improved by means of a serial resistor and an improved TFT chain in parallel. It is recommended to make inherent use of long lines for realisation of the serial resistor R_{prot}. A good usage of ITO, high resistive metallisation layer, would help to increase the input line resistance.

It is highly recommended to introduce ESD testing and ESD standards in large area electronics. HBM and MM testing of displays should became a standard procedure.

ESD testing by means of CDM instead of TLM measurements set-up would be a very interesting experiment. First reason is that TLM set-up is very difficult for ESD testing of TFT's, as in some cases the TLM current is too low to be measured. But also, CDM model could give a better emulation of reality in which TFT's operate. This assumption is build on the fact that AMLCD's are very easily charged during the manufacturing process.

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Samenvatting

Amorf-silicium dunne film transistoren worden nog steeds veel gebruikt in de halfgeleider industrie, ondanks dat deze devices een erg lage elektronen mobiliteit hebben en uitgesproken instabiel zijn voor wat betreft hun elektrische eigenschappen. Er zijn nl. ook enkele goede eigenschappen: depositie kan plaatsvinden onder lage temperaturen en over een groot oppervlak. Bovendien zijn ze erg goedkoop. Uit de praktijk komt naar voren dat elektrostatische ontlading (electrostatic discharge, ESD) een van de belangrijkste problemen in de dunne film elektronica is. Het staat een betrouwbare werking van dunne film transistoren in de weg; in de eerste plaats tijdens het produktie proces in de cleanroom, maar in sommige gevallen ook tijdens gebruik. Vanwege hun hoge weerstand zijn α-Si:H TFT's moeilijk te beschermen tegen ESD en het is moeilijk om de stroom omlaag te brengen. Een andere moeilijkheid van betreft ESD bescherming is het feit dat ze op een isolerend substraat zijn gebouwd. Tot slot zijn de test methoden en ontwerpregels die ontwikkeld waren voor de silicium geïntegreerde circuits niet bruikbaar voor α-Si TFT's. Voor de bescherming van TFT circuits tegen ESD zal moeten worden omgezien naar een alternatief ontwerp van de devices.

Dit werk behelst de studie naar elektrostatische stress in dunne film transistoren. Hiertoe zijn gekoppelde gate α-Si:H TFT's blootgesteld aan diverse experimenten met ESD om zodoende hun gedrag onder ESD stress te analyseren. Vastgesteld is dat "zachte" degradatie plaatsvindt voor breakdown. Deze zachte degradatie is zichtbaar vanwege een verschuiving in de drempelspanning (verlaging). Dit heeft een verhoging van de lekstroom tot gevolg. Deze degradatie is te wijten aan door ESD stress gecreëerde states in de amorphous silicon band gap. Tevens is aangetoond dat het breakdown spanning lineair afhankelijk is van de channel lengte in korte kanaal TFT's, en dat deze spanning constant is voor kanaal lengtes groter dan 9 μm. Breakdown in lange TFT's is te wijten aan een hoog elektrisch veld in de gate isolator. In korte TFT's vindt punch-through en avalanche breakdown

plaats.

Zelfverwarming in de TFT's met verschillende channel lengtes alsmede onder ESD stress met verschillende pulsduur is gesimuleerd. Het is bewezen dat korte kanaal TFT's te lijden hebben onder zelfverwarming, terwijl dat effect gereduceerd is in lange kanaal TFT's. De tijd die benodigd is om een temperatuursevenwicht te bereiken bedraagt ongeveer 15 μs. Korte pulsen (ESD pulsen) wekken minder zelfverwarming op dan lange pulsen (¿15 μs).

Een goed voorbeeld is de vingerafdruk sensor, die bestand moet zijn tegen de statische lading die is opgebouwd in het menselijk lichaam. Een dergelijke sensor is ontworpen en gebouwd. Het effect van ESD hierop is geanalyseerd.

Tot slot is ESD stress in een werkelijk TFT circuit getest en geëvalueerd.Uit het resultaat blijkt dat een weerstand aan de TFT kettting moet worden toegevoegd voor een efficiënte ESD protectie. Het ontwerp van de protectie dient te worden geoptimaliseerd om de spanning in het circuit te verlagen tot 300 V. Dit betekent, dat de TFT's in the ketting een zo groot mogelijke stroom moeten kunnen voeren.

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13. **N. Tošić Golo**, T. Jenneboer, T. Mouthaan "Capacitive fingerprint sensor in amorphous silicon thin film technology", poster, SAFE'02, to be presented.

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