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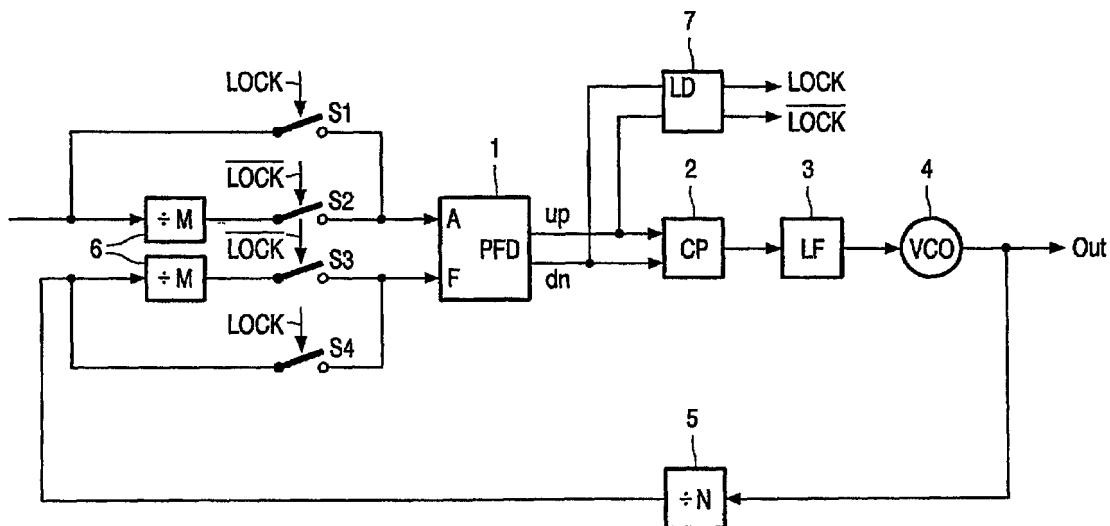
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(54) Title: PHASE-LOCKED-LOOP WITH REDUCED CLOCK JITTER



(57) Abstract: The present invention relates to a phase-locked-loop (PLL) circuit and a method for controlling such a PLL circuit, wherein the frequency of an input reference signal and the frequency of a feedback signal derived from an output oscillation signal are divided by a predetermined rate to thereby reduce the frequency at a phase detection means (1) of the PLL circuit. The dividing step is inhibited in response to a detection of a phase-locked-state of the PLL circuit. Thus, after phase-lock has been achieved, extra reference dividers (6) added to decrease the comparison frequency are removed from the loop to thereby enable increase in the loop bandwidths and decrease in the dividing ratio within the loop.

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