High-Performance Deep Submicron MOSTs With Polycrystalline-(Si,Ge) Gates

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Abstract

High-performance poly-$Si_{0.7}Ge_{0.3}$ gate PMOST and NMOST, compatible with conventional CMOS processing, are manufactured for devices with L_{eff} down to 0.15μm. For PMOST we observe a ~20% increase in saturation current and improved subthreshold slope from 81mV/dec to 75mV/dec wile off-state currents and short-channel effects are comparable to conventional devices. No influence of poly-$Si_{0.7}Ge_{0.3}$ on the performance of NMOS transistors gates is observed.

Introduction

In deep submicron MOS transistors high substrate doping levels are needed to avoid short-channel effects and subthreshold leakage. This results in a decreased carrier mobility and hence lower current drivability (I_{DS}^{sat}) of the devices. The situation can only be partly improved by changing channel profile ("super-steep retrograde" or "ground plane" channel designs) to reduce the channel dopant concentration. This cannot solve, however, the problem of high subthreshold currents due to low threshold voltage (V_T). An alternative approach is based on the gate workfunction change. The change of the gate-to-semiconductor workfunction difference $\Delta\Phi_{MS}$ allows one to reduce uniformly the surface channel doping while retaining the V_T at the same level as for poly-Si gate. The resulting decrease in the effective transverse electric field towards the Si-SiO_2 interface as well as removal of the scattering centres from the channel leads to a higher carrier mobility and an increase of the I_{DS}^{sat}. Reduction in the channel doping level also improves the I_{on}/I_{off} ratio since the subthreshold swing decreases with depletion layer capacitance. Additionally, the body-factor K goes down – a property which can be utilised in low-voltage CMOS applications to prevent the threshold voltage variations with the substrate potential.

Recently, polycrystalline silicon-germanium alloy (hereafter referred to as "poly-SiGe") has been suggested as a promising material for a single p-type gate CMOS process [1] and has also been studied for deep submicron NMOST [2]. The poly-SiGe films are compatible with standard CMOS processing, they provide comparable n- and better p-type dopants activation and, most importantly, an increase in Ge mole fraction induces a significant decrease in the p-type poly-SiGe workfunction [1]. However there have not been reported any results for deep submicron PMOS and NMOS devices.

We present here a comparative study of deep submicron PMOST devices fabricated in a conventional way (with poly-Si gate) and with poly-$Si_{0.7}Ge_{0.3}$ as a gate material. We show that a substitution of poly-$Si_{0.7}Ge_{0.3}$ for poly-Si leaves the main processing steps unchanged while it delivers a ~20% increase in I_{DS}^{sat} and improves the subthreshold slope S from 81mV/dec to 75mV/dec with off-state currents and short-channel effects at a comparable level. The body factor K decreases by more than 25% for submicron devices. At the

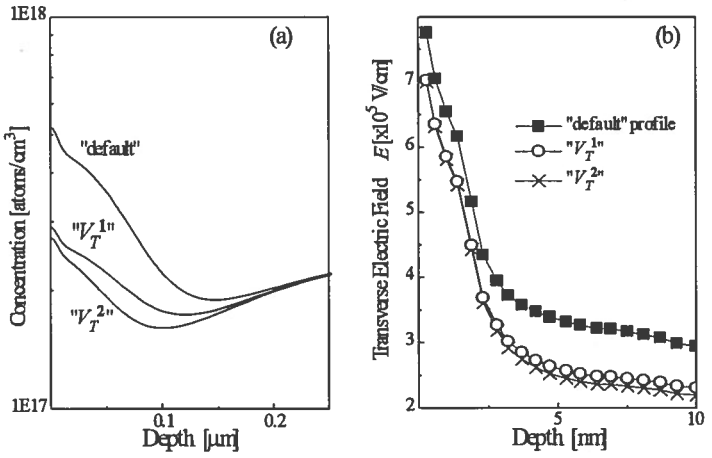

Fig. 1 (a) Channel doping profiles used in this study as simulated by TMA-SUPREM-3; "default" As V_T implant is 2.5×10^{12}@70keV, "V_T^1"- 1×10^{12}@70keV, "V_T^2"- 0.7×10^{12}@50keV. (b) the effective transverse electric field towards the Si-SiO_2 interface as calculated on the basis of profiles in (a) with -1.8V applied to a p-type gate.

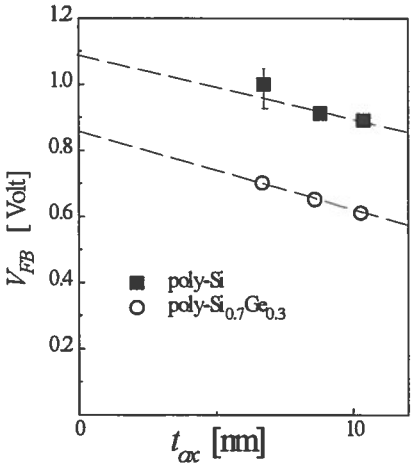

Fig. 2 Flat-band voltage $vs.\ t_{ox}$ for poly-$Si_{0.7}Ge_{0.3}$ capacitors. $\Delta\Phi_{MS}$ is determined at $t_{ox} = 0$. The thinnest gate oxide sample with poly-Si gate exhibit boron penetration which is not observed for poly-$Si_{0.7}Ge_{0.3}$ sample.

same time, deep submicron NMOSTs are not influenced by the use of poly-$Si_{0.7}Ge_{0.3}$ as a gate material. The results are of special importance to low-voltage applications of high-performance deep-submicron CMOS devices.

Experimental

Apart from the gate formation trajectory, the processing sequence for devices was similar to [3], featuring LOCOS isolation and optical lithography. The gate oxide is 4nm thick. The poly-Si and poly-$Si_{0.7}Ge_{0.3}$ layers were deposited at 625°C and 460°C, respectively, using an LPCVD reactor to obtain columnar polycrystalline films with grain size 200nm and 100nm. After gate patterning with HBr/HCl plasma shallow source/drain extension and thick SiO_2 spacers were formed followed by HDD implantations: BF_2^+ ions of 2.5×10^{15} cm^{-2} dose and 20keV energy for PMOSTs and As^+ 5×10^{15} cm^{-2} at 40keV for NMOST. Rapid thermal anneals of 50s at 950°C (for PMOSTs) and 20s at 1000°C (NMOSTs) were used to anneal the implantation damage, diffuse and activate dopants in the gate and source/drain regions.

Results and discussion

A. Numerical simulations

To estimate the performance improvements with introduction of the poly-$Si_{0.7}Ge_{0.3}$ as a gate material we have numerically simulated the resulting PMOSTs processing sequence using a TMA SUPREM-3 simulation tool. The simulated channel profiles with "default" (for poly-Si gate) and reduced channel implants for poly-$Si_{0.7}Ge_{0.3}$ devices (to get the same nominal V_T assuming the $\Delta\Phi_{MS}$ to be 0.2 eV – see below) are shown in figure 1(a). Figure 1(b) shows calculated values of the transverse electric field in the PMOST channel region. On the basis of the effective field mobility model [4] one can calculate a resulting increase of the I_{DS}^{sat} for devices with alternative channel profiles to be ~ 13%. We stress here that if a poly-$Si_{0.7}Ge_{0.3}$ gate is used with these profiles it should result into the same V_T values as with a poly-Si gate with higher "default" profile. The simulations also predict the decrease in the subthershold swing S to be about 15%.

B. Poly-$Si_{0.7}Ge_{0.3}$ as a gate material

Figure 2 shows the $\Delta\Phi_{MS}$ measured from flatband voltage variations with t_{ox} on PMOS capacitors with 30% Ge content to be ≈ 0.2 eV. No boron penetration is observed for poly-$Si_{0.7}Ge_{0.3}$ gates while it is present in the poly-Si gate with the thinnest oxide. The difference is believed to be caused by the slower boron diffusion in the poly-SiGe as compared to poly-Si.

The summary of dopant diffusion and de-activation results in poly-$Si_{0.7}Ge_{0.3}$ gates are presented in figures 3 and 4. Boron activation is higher [5] while the diffusion and deactivation rate are slower than in poly-Si creating thus preferable conditions for good gate activation. Arsenic diffuses faster in poly-$Si_{0.7}Ge_{0.3}$ but deactivation is similar to poly-Si.

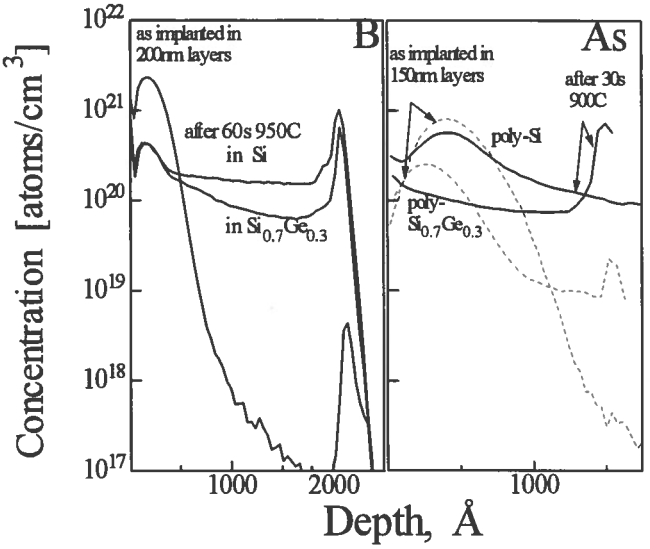

Fig. 3 SIMS profiles of dopant diffusion in poly-Si and poly-$Si_{0.7}Ge_{0.3}$ after RTA anneals of B and As implantations.

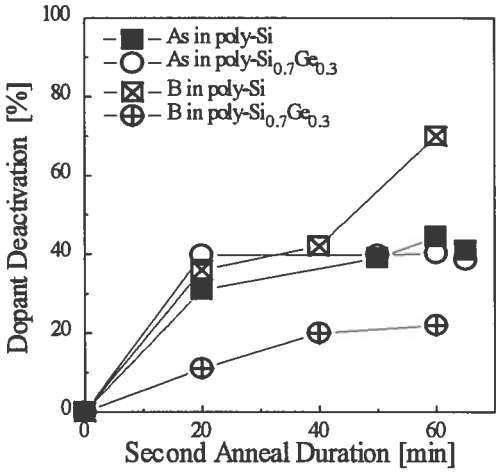

Fig. 4 Deactivation percentage of dopants in poly-Si and poly-$Si_{0.7}Ge_{0.3}$ after an extra anneal of 750°C

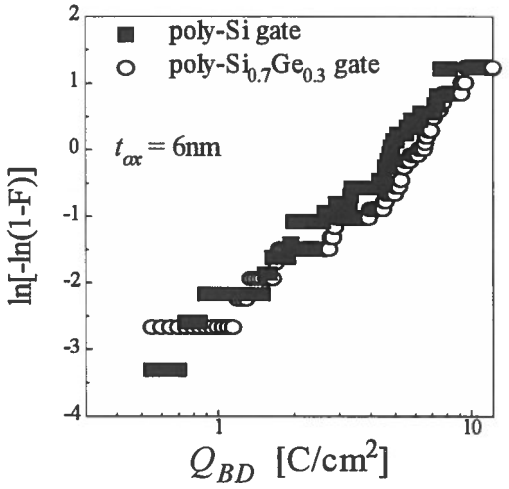

Fig. 5 Q_{BD} measurements of fifty 0.64mm² -large capacitors with poly-Si and poly-$Si_{0.7}Ge_{0.3}$ gates after 60s 950°C anneal

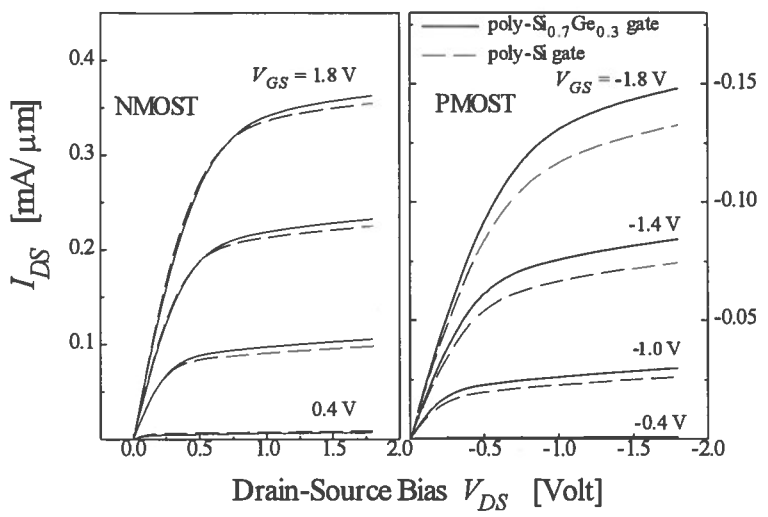

Fig. 6 Typical I_{DS}-V_{DS} characteristics of NMOS and PMOS transistors with L_{eff}=0.18μm with poly-Si and poly-$Si_{0.7}Ge_{0.3}$ gates.

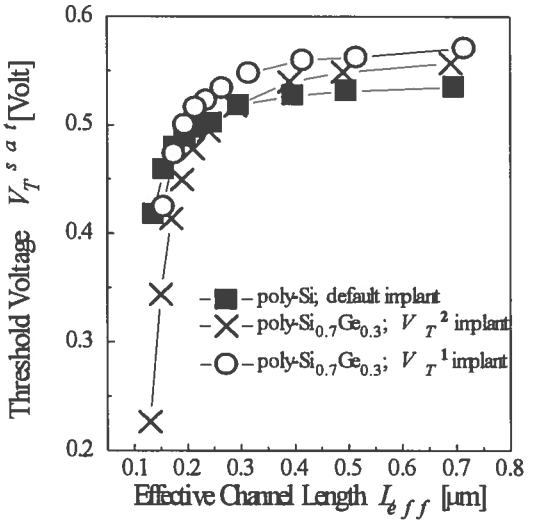

Fig.7 Saturated V_T (V_{DS} = –1.8V) roll-off comparison for PMOST

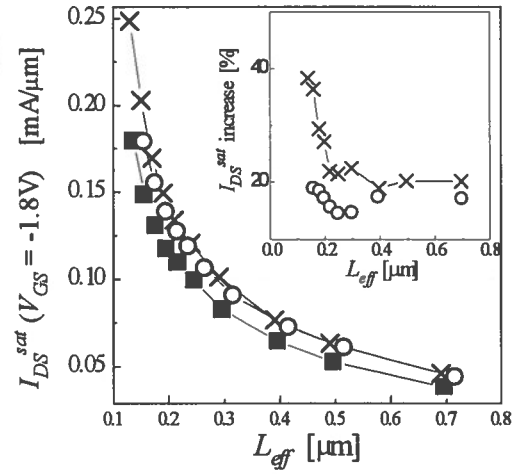

Fig. 8 Current drive increase vs. Effective channel length. Notations are the same as in figure 7

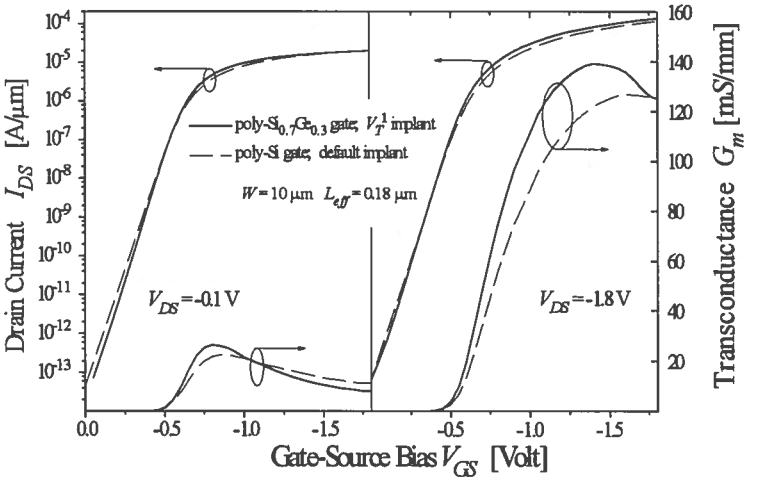

Fig. 9 Typical subthreshold characteristics and transconductance of the PMOSTs

Figure 5 presents the results of Q_{bd} measurements confirming the gate oxide is of excellent quality when poly-$Si_{0.7}Ge_{0.3}$ are used.

Altogether, the processing window for formation of good *n*- and *p*-type gates can be found. The *C-V* measurements on both NMOST and PMOS structures have shown that 200nm-thick poly-Si and poly-$Si_{0.7}Ge_{0.3}$ have similar gate depletion values with *p*-type poly-$Si_{0.7}Ge_{0.3}$ gate having the best dopant activation.

C. Electrical measurements

Figure 6 shows typical I_{DS} vs. V_{DS} characteristics for poly-Si and poly-$Si_{0.7}Ge_{0.3}$gates for PMOS (with "V_T^1" channel profile) and NMOS devices with L_{eff} of 0.18μm and 4 nm gate oxide. For PMOSTs the threshold voltage for both devices is measured to be– 0.48V, its dependence on L_{eff} is depicted in figure 7: the variant with poly-$Si_{0.7}Ge_{0.3}$ gate and

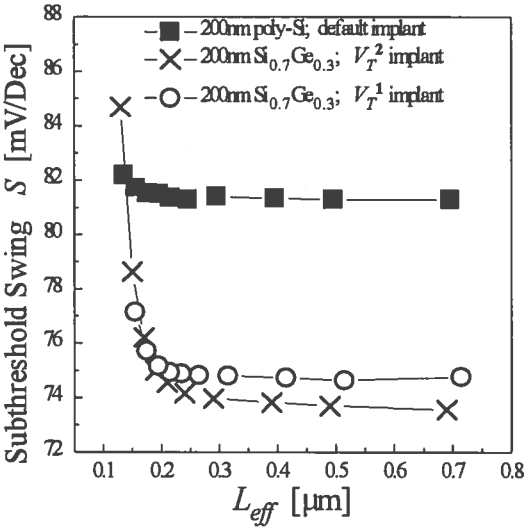

Fig. 10 Subthreshold swing improvement for poly-$Si_{0.7}Ge_{0.3}$ gated PMOSTs

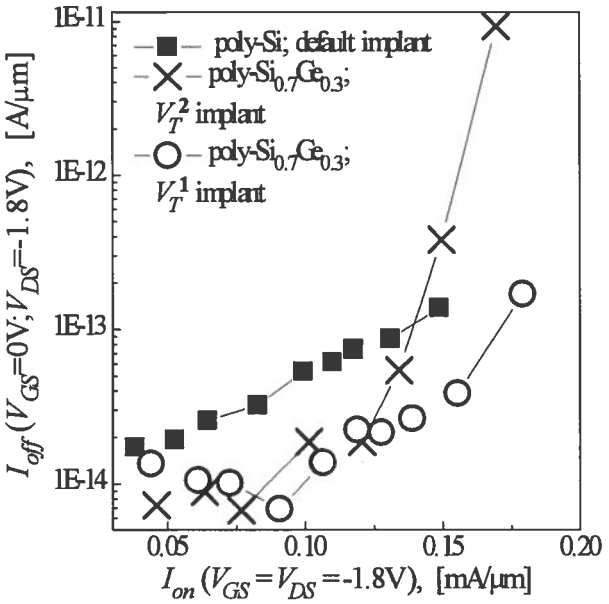

Fig. 11 I_{on}/I_{off} comparison for poly-Si and poly-$Si_{0.7}Ge_{0.3}$ PMOSTs

the deeper implant (V_T^1) has comparable short channel effect immunity as the reference device with high substrate doping. At the same time devices with somewhat shallower and lower dose V_T implant (V_T^2) exhibit much worse roll-off behaviour. This clearly demonstrates how sensitive deep submicron devices can be to the exact channel profile. NMOS devices show at least as good saturation current and V_T roll-off behaviours as their counterparts with conventional poly-Si gates.

A 15-20% increase in I_{DS}^{sat} is observed for PMOSTs with poly-$Si_{0.7}Ge_{0.3}$ gates and V_T^1 implant for effective gate lengths down to 0.15μm (see inset to figure 8). This is combined with a 10% increase in a channel transconductance G_m^{max} confirming the expected from simulations increase in the channel carrier mobility. A significant rise of the I_{DS}^{sat} for devices with V_T^2 channel profile corresponds to the increase of the leakage current induced by low threshold voltage for small devices.

The subthreshold characteristics of the devices with poly-$Si_{0.7}Ge_{0.3}$ are clearly improved (figure 9), this is further reflected in figure 10 where S is plotted vs. L_{eff}. Here, again, a sharp increase of the subthreshold slope value in the region of low L_{eff} is caused by the appearance of comparatively strong off-state leakage currents.

The I_{on}/I_{off} ratios are presented in figure 11. For a given I_{off} the devices with poly-$Si_{0.7}Ge_{0.3}$ gates deliver, in general, highest I_{on}. To benchmark the performance of the PMOST devices we compare our values on poly-$Si_{0.7}Ge_{0.3}$ gate devices with L_{eff} of 0.18μm to the previously reported data on optimised CMOS with poly-Si gates of similar length [6] and conclude that for a given off-state current value devices with poly-$Si_{0.7}Ge_{0.3}$ gates deliver significantly better performance.

Note also that extremely low values of the off-state currents coupled with small subthreshold voltage swing values allow one to use the poly-$Si_{0.7}Ge_{0.3}$ PMOSTs in low-voltage CMOS applications: by fixing the I_{off} at a certain value, the V_T can be brought down by careful optimisation of the channel profile to allow for the use of low power supply voltage. At the same time the reduction of the V_T will result in an increase of the I_{DS}^{sat}. This optimisation scenario has been performed by TMA SUPREM-3 process simulator together with MINIMOS4 2D device simulator. Both simulators have been calibrated to the presented here experimental data. The results show that the PMOST devices with poly-$Si_{0.7}Ge_{0.3}$ gates will combine excellent short-channel behaviour with higher than 0.3mA/μm I_{DS}^{sat} values for the 100 pA/μm I_{off} criterion. Thus, using of poly-$Si_{0.7}Ge_{0.3}$ as a gate material a high-performance low-voltage CMOS can be realised where matching in performance between NMOS and PMOS transistors is significantly improved as compared to the CMOS with standard poly-Si gates.

Due to the lower channel doping level the body-factor K is also significantly lower in the PMOS devices with poly-$Si_{0.7}Ge_{0.3}$ gates (see figure 12). This can also be useful in low-voltage applications where the influence of the substrate potential fluctuation on the V_T can be reduced.

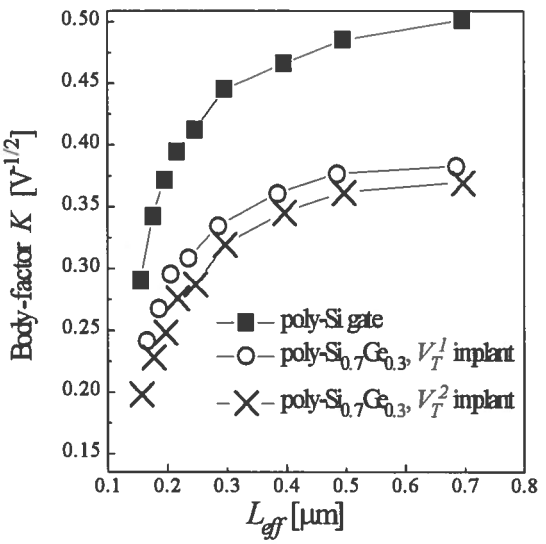

Fig. 12 Body-factor comparison for PMOSTs with poly-Si and poly-$Si_{0.7}Ge_{0.3}$ gates

Conclusions

We have successfully manufactured deep submicron MOS transistors using poly-$Si_{0.7}Ge_{0.3}$ as a gate material. Full compatibility with existing CMOS processing is achieved. In PMOSTs a 20% increase in current drive, significant improvement of the subthreshold swing, I_{on}/I_{off} ratio and body factor have been observed. At the same time good control over short-channel effects has been achieved by the channel profile optimisation for these devices. Poly-$Si_{0.7}Ge_{0.3}$ gates do not influence the performance of NMOS transistors. These results could provide a basis for implementation of

high-performance low-voltage deep-submicron CMOS process.

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