REALISATION OF A 0.25 μm NMOSFET USING Ge_xSi_{1-x} (x<0.4) AS GATE MATERIAL

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ABSTRACT

The realisation a 0.25 μm NMOSFET using arsenic implanted Ge_xSi_{1-x} as gate material, with minimal changes in an existing process is reported. The etching of this gate material does not pose a problem and the underlying thin gate oxide is hardly attacked. We will show good transistor characteristics for both a 6nm and a 4.5 nm oxide thickness. V_T roll-off is comparable for the poly-Si and poly- Ge_xSi_{1-x} gates.

INTRODUCTION

Polycrystalline germanium-silicon is an interesting material for applications as gate material in deep submicron CMOS technology [1,2]. The fact that this material is one of the very few potential candidates for mid gap gate materials which is compatible to existing silicon CMOS technologies, make this an interesting material. So far it has not yet been shown that it is indeed possible to make these very small devices in an existing process with only minor changes in the process flow.

EXPERIMENTAL

The 200 nm thick layers of Si and Ge_xSi_{1-x} gate material are deposited in a conventional hot-wall LPCVD reactor, using a mixture of SiH_4 and GeH_4 on 6" wafers covered with either 6 or 4.5 nm gate oxide. Polycrystalline Si was deposited at T=620^{o}C and p=0.2 mBar. To obtain smooth Ge_xSi_{1-x} layers it was necessary to reduce the deposition temperature to 460^{o}C for x<0.4. The deposition pressure was increased to p=0.6 mBar for x<0.3 and p=1.3 mBar for x~0.4. In the case of the lowest Ge percentage these layers were amorphous. The layer with 40% Ge was microcrystalline.

The etching was done in a standard HBr/Cl_2 plasma etch. The transistors were processed with a $5*10^{15}$ As/cm^2 gate implantation. The activation anneal was performed in an RTA system for 20 sec at 1000^{o}C in N_2 ambient. Until the silicidation the processflow was identical for all gate materials. The first anneal of the

silicidation process, to achieve the C49 phase, was reduced 50^{o}C for all the Ge_xSi_{1-x} gates (x>0). The second anneal was kept the same as for the standard Si gate processing, and was not optimised. Some details about the processing can be found in [3].

RESULTS

Etching

The etch rate of GeSi alloys increases with the Ge content, thus increasing the selectivity to the underlying SiO_2. It is possible to achieve good etch profiles with acceptable etch times and almost no loss in gate oxide thickness for alloys up to x=0.4. Figure 1 shows the etch rate versus the Ge content using a HBr/Cl_2 plasma etch for a 200 nm thick polycrystalline gate using a hard oxide mask. On non structured wafers we have determined the etch rate of the TEOS masking layer to be 41nm/min=0.68nm/sec. Figure 2 shows a typical etch profile for a $Ge_{0.2}Si_{0.8}$ alloy. The profile is similar for both the Si and the other GeSi alloys.

Diffusion

Small nonstructured Si and $Ge_{0.3}Si_{0.7}$ samples, doped with $5*10^{15}$ As/cm^2, 40 keV were annealed simultaneously in an RTA system for 30 seconds at 700, 800, 900 and 1000 ^{o}C. In figure 3 the diffusion profiles of arsenic in $Ge_{0.3}Si_{0.7}$ and Si as determined by SIMS are shown. The diffusion of As in $Ge_{0.3}Si_{0.7}$ is faster than in poly-Si an does not seem to be a problem, this in contrast to the diffusion of boron in GeSi PMOS devices. For the 30sec 1000 ^{o}C anneal outdiffusion of the arsenic is observed, showing the necessity of a capping layer. Good diffusion is obviously necessary to prevent gate depletion. In our MOS processing the anneals to activate and diffuse the dopant in the gate was 20 sec at 1000 ^{o}C for all gate materials.

Silicidation

Little information about the silicidation of poly-GeSi exists. Preliminary experiments have shown that the first anneal of the silicidation process should be reduced approximately 50 degrees, to achieve a C49 phase. This means that also the source/drain areas are silicidized at lower temperature. The second anneal is kept the same for all materials. The S/D resistance does not seem to be affected by this reduction in temperature. It will be necessary to optimise the silicidation process further, especially for the higher Ge contents because of the roughening of the layers (increase with Ge content) and the effectiveness of the silicidation reaction.

Electrical characteristics

Hall measurements have shown that the sheetresistance of $Ge_{0.3}Si_{0.7}$ is larger than that for Si whereas the Hall mobility and the Hall activation are both smaller. From CV measurements we have found gate depletion (taken +2.5 and -2,5V from V_{fb}) to be 17% for a Si gate, 12% for $Ge_{0.2}Si_{0.8}$, 12.6% for $Ge_{0.3}Si_{0.7}$ and 16% for $Ge_{0.4}Si_{0.6}$, the

latter two curves are shown in figure 4. Different levels in gate depletion can be caused by different diffusion and dopant activation levels. Since the activation in Si is higher we must assume that the higher gate depletion in Si is caused by slower dopant diffusion, see figure 3.

Figure 5 and 6 shows the saturation and subthreshold characteristics of 0.25 μm NMOS devices (W=10) with Si and Ge_xSi_{1-x} with 6nm gate oxide thickness. The higher I_d for $Ge_{0.2}Si_{0.8}$ and $Ge_{0.3}Si_{0.7}$ can be explained from the difference in gate depletion. The smaller I_d for $Ge_{0.4}Si_{0.6}$ can be explained from the fact that the effective gate length is approximately 10% larger for this gate material. This might be caused by the difference in etch rate. In figure 7 the dependence of the threshold voltage on the channel length is shown for $0<x<0.4$, the very small shift in V_T (~30mV) can be explained from the difference in electron affinity between Si and Ge_xSi_{1-x}, but this could also be caused by "normal" fluctuations in the process .

We have also substituted the 6nm gate oxide by a 4.5 nm gate oxide. The other process steps remained the same. Also in this case we have obtained good saturation and subthreshold characteristics indication that for these gate oxide thickness' no fundamental problems seem to arise, see figure 8 and 9.

CONCLUSIONS

We have shown that it is possible to fabricate 0.25 μm NMOSFETs using Ge_xSi_{1-x} as gate material with little changes in an existing process without losing gate oxide quality for 6 and 4.5 nm gate oxide thickness'. The diffusion of As in Ge_xSi_{1-x} is faster than in Si. Although in Ge_xSi_{1-x} a lower activation is achieved the gate depletion stays within reasonable limits. Care must be taken in the silicidation steps, the anneal temperatures must be reduced and further research is necessary to optimise this process step.

ACKNOWLEDGMENTS

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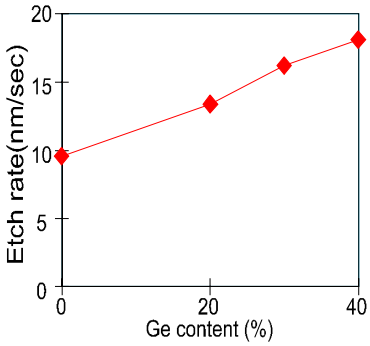


Fig 1: Etch rate versus Ge content using a HBr/Cl_2 plasma etch

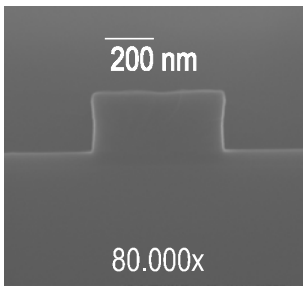


Fig 2: Typical etch profile $Ge_{0.2}Si_{0.8}$

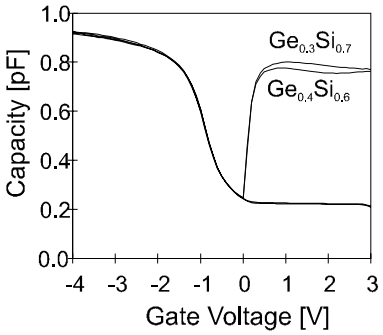
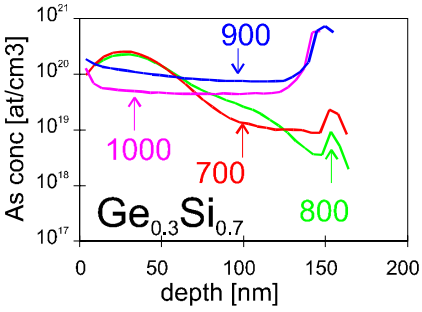


Fig 4: Quasi static and high frequency CV measurements for t_{ox}=6nm



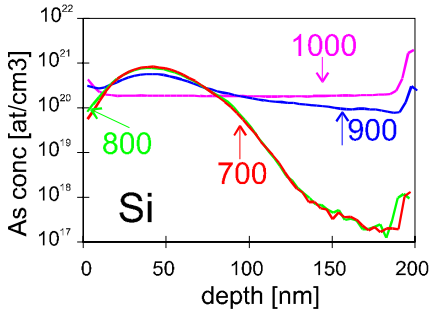


Fig 3: Diffusion of 5E15 As in $Ge_{0.3}Si_{0.7}$ and Si after 30 sec N_2 RTA anneals

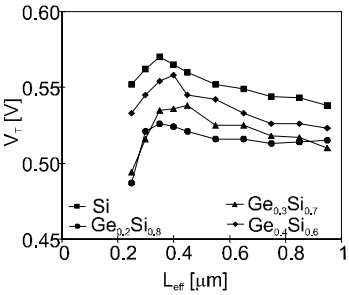


Fig 7:Dependence of the theshold voltage on the gate length

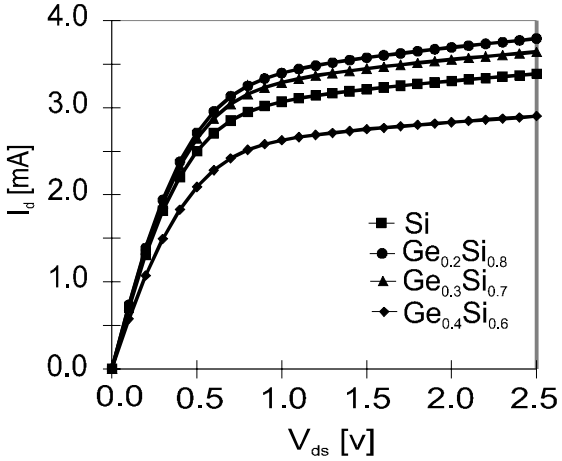


Fig 5:Saturation characteristic of a 0.25μm device with t_{ox}=6nm at V_g=2V

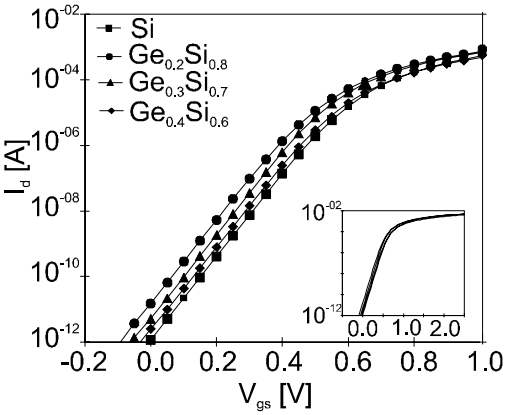


Fig 6:Subthreshold characteristic of a 0.25μm device with t_{ox}=6nm at V_{ds}=1V

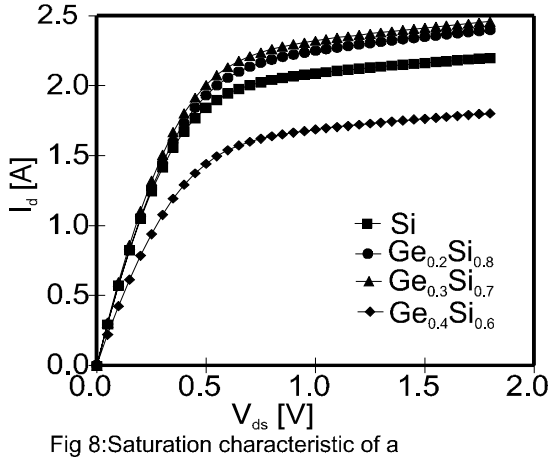


Fig 8:Saturation characteristic of a 0.25μm device with t_{ox}=4.5nm at V_g=1.4V

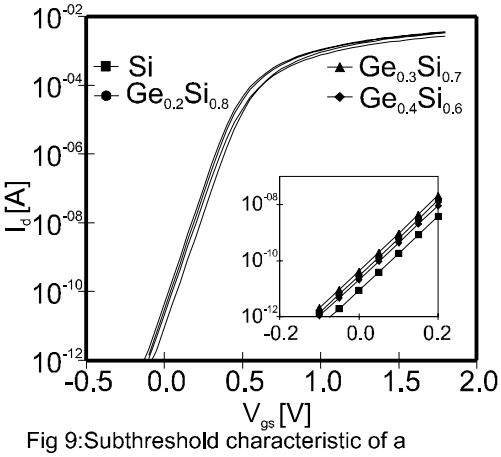


Fig 9:Subthreshold characteristic of a 0.25μm device with t_{ox}= 4.5 nm at V_{ds}=1V