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Nanopores Created using an Internal Shadowmask Process

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***Abstract*— We report on the manufacturing of nanopore through-holes by heating gold nanoparticles on a silicon oxide (SiO_2) sheet, suspended in a silicon-rich nitride membrane (SiRN). Membrane patterning is performed using self-alignment by an internal shadow mask based process. A benefit of this approach is the ease at which downscaling of the lithographic features can be achieved. With a single alignment, a shadow mask is etched and metal is deposited. The nanopore through hole is then created after heating. In this paper this scalable technique is applied to create non-buckled membranes by combining the compressive and tensile stress components in a SiO_2/SiRN bilayer. Theory on the bilayer stresses is given in order to characterize the buckling. The nanopore through holes are characterized using ionic current measurements and electron microscopy techniques.**

Keywords— solid-state nanopore formation; gold nanoparticles; silicon oxide; silicon rich nitride; shadow mask

I. INTRODUCTION

The use of nanoporous membranes offers possibilities for example in sieving and filtration of liquid or gaseous mixtures [1,2]. A regular distribution of nanopores can be of interest in schemes where quantification of the content of such liquids or gaseous mixtures is important [3]. Moreover, a membrane with just a single nanopore, when in the order of <2nm in diameter potentially has the ability to serve as sequencing tool for deoxyribonucleic acid (DNA) [4].

In this research nanopores in a membrane were manufactured by heating a gold patch on a silica membrane to 1064°C ±5°C, a scheme that was reported in previous publications. [5,6] Nanopore creation in bulk SiO_2 has been characterized but a transfer of this technique to a membrane appeared problematic due to buckling of the membrane as a result of the heat treatment. Incorporation of the stress components of SiO_2 and SiRN allows creation of non-buckled membranes. [7]

To overcome the problem of membrane buckling, a 40 nm thick SiO_2 layer suspended in a 200 nm thick silicon nitride membrane will be used. [8, 9]The heating of a SiO_2 membrane to high temperatures will result in an increase of compressive stresses in the membrane. [10] However, since the SiO_2 is suspended in SiRN in this case, it is expected the compressive stress is compensated by the tensile stress in the SiRN.

Compared to established nanopore fabrication techniques, for example electron beam writing and ion beam milling, our method enables fast, high volume processing and omits the use of complex equipment. [11,12] For characterization of the nanopores created by heating gold nanoparticles, high resolution scanning electron microscopy (HRSEM), transmission electron microscopy (TEM) and ionic current measurements through the nanopores will be performed.

II. MATERIALS AND METHODS

Manufacturing

The processing steps used for manufacturing are given in figure 1. We use a 380 µm thick silicon (100) wafer. A SiO_2 layer of 40 nm is grown on each side by dry oxidation at 1000°C, followed by deposition of 200 nm thick silicon nitride. To create the membranes from the SiO_2/SiRN bilayer, the backside of the wafer is patterned by photolithography. Olin 907-17 positive photoresist is spin coated on the surface after which the wafer is UV-exposed for 4 seconds with a dose of 12 mW/cm^2. Development takes place in OPD4262 for 2 x 45 seconds followed by dry etching of the SiO_2/SiRN bilayer. (Plasma etch, time: 4 minutes, 5 sccm O_2, 25 sccm CHF_3 sccm, 10mTorr, 60W). Afterwards the photoresist is stripped in nitric acid (HNO_3) and the SiO_2/SiRN bilayer functions as a mask for the silicon etch in potassium hydroxide (KOH 25%, 75°C). The KOH etches 350 µm deep so that a silicon layer of 30 µm remains. The substrates are cleaned using RCA2 solution (H_20:HCl:H_2O_2, 80°C) to remove KOH residue from the substrate, followed by low-pressure chemical vapor deposition (LPCVD) of a 10 nm thick layer of poly-silicon. The poly-silicon covers both sides of the wafer, and will be oxidized so a layer of 4-5 nm thick silicon oxide is grown on top of the SiRN. Again an Olin 907-17 positive photoresist layer is applied on the silicon oxide (from polysilicon) to pattern the topside of the membrane with 2µm circular features, which are evenly spaced by 5 µm. UV-exposure for 4 seconds with a dose of 12 mW/cm^2 and development in OPD4262 are performed, followed by a 2 minutes 1% HF etch step which patterns the silicon oxide (from poly-silicon) on top of the SiRN. The photoresist layer is stripped from the oxidized polysilicon by acetone and isopropanol, followed directly by a tetramethylammonium hydroxide (TMAH) etching step to etch through the remaining polysilicon onto the silicon nitride. The silicon nitride is etched using phosphoric acid (85% H_3PO_4, 180°C). The 85% H_3PO_4 etches the 200 nm silicon nitride isotropically and thus creates a shadow mask from the polysilicon layer. SiO_2 etches 10 times slower than SiRN in 85% H3PO4, 180°C. [13] This opens the

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option to stop the etching when the 40 nm thick SiO_2 sheet is reached during the etch process. This "internal" shadow mask is used for patterning of the gold which will be deposited both onto the newly exposed 40 nm thick SiO_2 sheet and on rest of the SiO_2/SiRN bilayer.

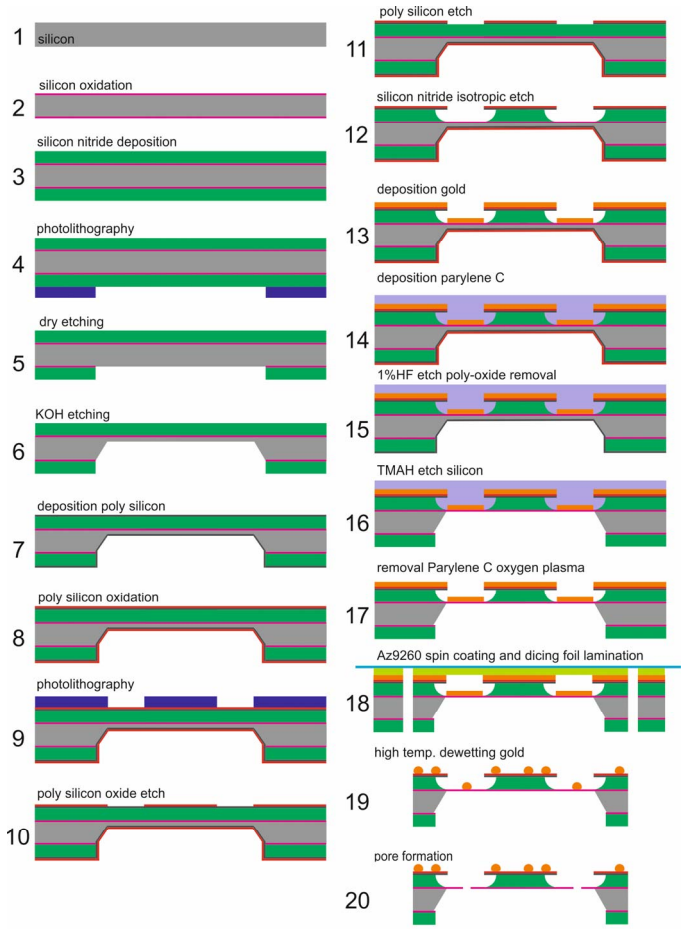

Figure 1 process flow of the manufacturing process.

In order to prevent damage to the SiO_2/SiRN bilayer with the patterned gold a layer of Parylene C with a thickness of 1 µm is applied to protect this side of the substrate. The parylene C is resistant to 1%HF and also to TMAH. This allows removal of the oxidized poly-silicon on the backside using 1%HF and removal of silicon by TMAH up to the 40 nm thick SiO_2 membrane. After removal of the Parylene C with oxygen plasma the substrate is diced into 12 mm square separate chips using a Disco Dicing DAD321. In this process the membranes could get damaged by the high pressure spray of the dicing blade cooling water, or during peel off from the dicing foil. Therefore, to protect the membranes from breaking during the dicing process, the gold patterned side of the wafer and membranes are spin coated with 10 µm thick AZ9260 photoresist, before being mounted on a dicing frame using foil. After dicing the chips are placed in acetone. The AZ9260 will dissolve and the dicing foil is lift-off from the chips. A high temperature treatment at 1064°C in ambient atmosphere (TOMA TSD 12, Volkel, the Netherlands) is performed to create the nanopores through the SiO_2. After the heat treatment a gold etch is performed (Gold etchant, standard, Sigma Aldrich) to avoid interference from the gold while measuring the ionic current through the nanopore (see later). After removal of the gold, a piranha (H_2SO_4:H_2O_2, 80°C) cleaning for 10 minutes is performed, followed by a 20 minutes O_2 plasma cleaning. Directly after the plasma cleaning the chip is put in a beaker with demineralized water to circumvent any filling issues of the nanopore in the conductance measurements.

Membrane

Thin films contain compressive or tensile stress due to the material properties and the method of how the film is applied. In the case of SiO_2 the residual stress is a compressive stress, for the case of SiRN this is a tensile stress. With these properties combined one could create a stable, non-buckled bilayer membrane of SiRN and SiO_2, where the SiRN forms a ridged support and the SiO_2 can be used for nanopore creation. Removal of the Si below a SiO_2/SiRN bilayer results in a freely suspended membrane mounted to the Si on the sides of the membrane. Following Popescu et al. [7] a value for the critical stress S_{cr}, in a SiRN monolayer membrane can be found using:

$$S_{cr} = \frac{h^2}{a^2}\frac{E}{1-v^2}$$

Here the membrane thickness is given as h, and the area of the membrane as a. E represents the Young's modulus, and v Poisson's ratio. For the calculation of the critical stress the values for the mechanically stable 200 nm thick SiRN layer are used, the values for the 40 nm thick SiO_2 layer are neglected. For the total stress, S_{tot}, the values of both the SiO_2 and SiRN layers are used. Buckling appears above the critical stress S_{cr}. To predict the total stress S_{tot}, the residual stresses of SiO_2 and SiRN should be known to calculate [7]:

$$S_{tot} = \frac{S_{SiO_2} * h_{SiO_2} - S_{SiRN} * h_{SiRN}}{h_{SiO_2} + h_{SiRN}}$$

The thicknesses of the layers are given as h_{SiO2} and h_{SiRN} in the membrane stack. Calculation of the stresses is given in the Results and Discussion section.

Characterization

Characterization of nanopores in the membrane is performed using high resolution scanning electron microscopy (HRSEM) to investigate morphology. To verify through-hole creation, transmission electron microscopy (TEM) was used. A second method used to verify whether through-hole nanopores were created was by measuring the ionic conductance of the membrane when suspended in solution. The setup for the conductance measurements is shown in Figure 2. The chip containing the nanopores was clamped by two O-rings. The reservoirs are filled with the 1M KCl solutions and the electrodes are placed in the trans- and cis-reservoirs.

For the transmembrane conductance measurements two reference electrodes were used (Calomel, XR110 13311-A03). Prior to each series of measurements an inspection of the electrodes was performed by submerging them both in a 1M KCl solution to verify if there is no voltage offset between the two electrodes and a low ohmic connection to the solution. Cyclic voltammetry was then used to apply a voltage profile to the electrodes and measure the current through the membrane.

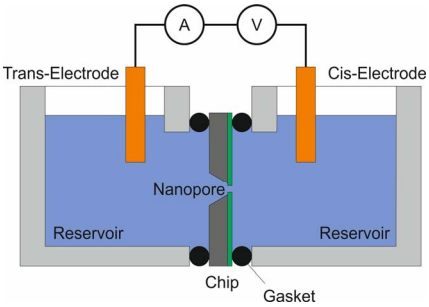

Figure 2 the ionic current measurement setup.

III. Results and Discussion

Manufacturing

Figure 3a and 3b show one of the twenty 25 x 25 µm SiO_2/SiRN bilayer membranes before and after heat treatment respectively.Each chip contains 20 membranes in total. The membrane is supporting 30 individual, Ø 2 µm, SiO_2 sheets. The entire surface of the SiO_2/SiRN bilayer membrane is covered with dewetted gold particles after heat treatment. We assume, based on previously published results that a thin layer of silicon oxynitride could has formed on the SiRN during the heating in ambient atmosphere. [5] The HRSEM image in figure 3c shows an individual SiO_2 membrane, after gold etching, where six nanopores can be observed.

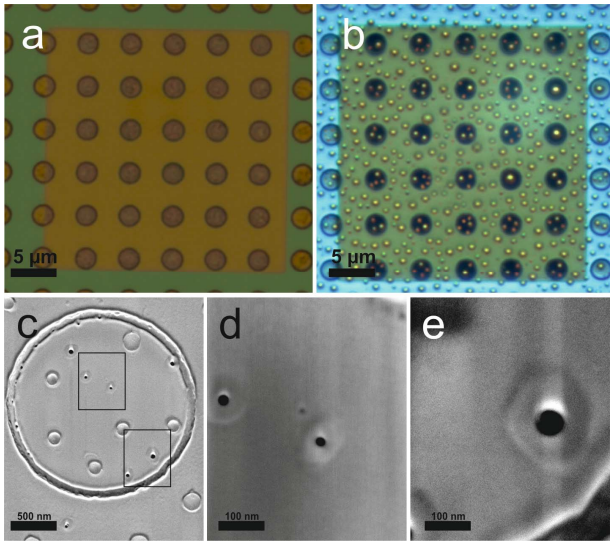

Figure 3a The SiO_2/SiRN bilayer membrane before heat treatment. 3b The surface covered with gold nanoparticles after annealing for 6 hours at 1064°C. The membrane contains 30 SiO_2 membranes with 2 µm diameter, 3c: a single SiO_2 membrane after gold etch showing 6 nanopores, 3d and 3e: close-ups of the nanopores in the square areas indicated in 3b.

The chips have been placed in gold etchant to remove all gold particles. The formation of multiple pores can be explained by the break-up from the originally continuous gold film on the SiO_2 due to pinch-off. [14] The separate gold nanoparticles will then each penetrate the SiO_2 membrane, forming nanopores. Figures 3d and 3e show a close-up of areas containing nanopore(s). Both the SiO_2 membrane and the SiRN surface show ridges as a result of ceramic migration under the gold nanoparticles, whereby a hexagonal shape represents the hexagonal crystalline gold nanoparticle. [5]

Membrane

Figure 3a and 3b show no buckling before and after heat treatment. This indicates that the total stress in the membrane is still below the critical stress value, above which buckling would occur. A 25 x 25 µm membrane, with a SiO_2 thickness of 40 nm and a SiRN thickness of 200 nm has a critical stress of 29,8 MPa, while a total stress of 16,7 MPa is calculated. The presence of the nanopores and the possible densification of the SiRN as a result of heat treatment has not been taken into account for these calculations.

Characterization

Evidence of nanopore through-hole formation is also given by TEM imaging, shown in figures 4a-d.

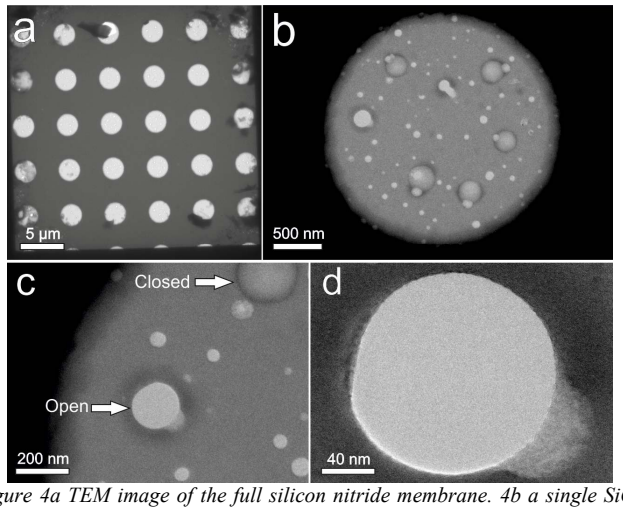

Figure 4a TEM image of the full silicon nitride membrane. 4b a single SiO2 membrane. 4c an open nanopore. 4d, close-up of the nanopore through hole shown in c.

The average size of the nanopores measured by TEM was 102 nm in diameter, with a standard deviation of 37 nm (n=26). The nanopore diameters were estimated from 14 of the 30 SiO_2 sheets in figure 4a. Extrapolation of the number of nanopores per SiO_2 patch would result in 56 nanopores per membrane and thus a total of 1120 nanopores per chip.

However, apart from by microscopic observations, the number of nanopores per chip was also determined via the trans-membrane conductivity measurements. Five different chips were measured in the trans-cis setup, whereby four chips

contained membranes with nanopores and one chip served as reference. Each chip has 20 membranes, each 25 by 25 µm squared, with 30 SiO_2 sheets with nanopores. A voltage sweep was applied from -5mV to +5mV at a rate of 1 mV/s and the resulting ionic current through the membrane was measured. Figure 5 shows the cyclic voltammetry curves of the closed membrane serving as reference (*Chip 1*) in green, and for the membranes with nanopores (*Chip 2-5*). The ionic current through the chips with membranes ranged from -0.8 µA to +0.8 µA as can be observed in Figure 5. The conductance of each chip was calculated as the average slope of the CV curves by a MATLAB script and was found to be ~0.15 mS.

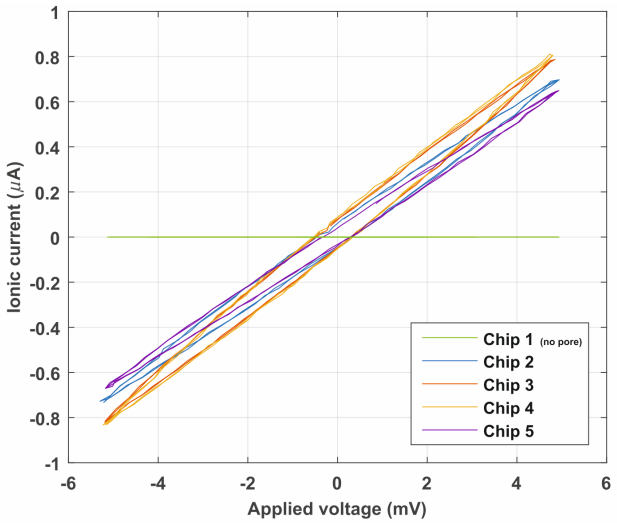

Figure 5. Cyclic voltammetry graph of 5 measured chips. Chip 1 contained no nanopores, chip 2-5 did contain nanopores.

For ease of calculation, each pore was assumed to be a cylindrical resistor and the membrane was assumed to be electrically equivalent to an array of pores in parallel not influencing each other. The total conductance of the chip is then equal to the sum of all pore conductances. The conductance for a single pore with diameter *d* was calculated using [15]:

$$G_{pore} = \sigma \left(\frac{4h}{\pi d^2} + \frac{1}{d} \right)^{-1}$$

The bulk solution conductivity σ was set to 10.8 S/m (for 1 M KCl at room temperature), and each pore was assumed to have a conductivity equal to this bulk conductivity. The 26 pore diameters which were observed in the TEM measurements served as an input for this calculation, which resulted in a mean pore conductivity of 0.78 µS with a standard deviation of 0.34 µS.

Using this calculated pore conductance and the measured membrane conductance, the total number of nanopores in the chips is estimated to be 235 with a standard deviation of 115 nanopores. The characterization using TEM mentioned above provided a measure for the average nanopore diameter of 102 nm and a nanopore count of 1120 nanopores per chip. The estimate from the ionic current measurements thus was almost 5 times less compared to the estimation based on the TEM results. The exact number of nanopores thus remains unclear.

IV. Conclusion

The internal shadow mask process presented here can be used to expose small features and as such is expected to be able to create even smaller nanopores in thinner membranes, since the process is easily downscalable. The process presented here relies on a single mask exposure step for each side of the wafer. A single alignment step is advantageous since it reduces alignment errors and thus increases yield. This approach could potentially, in combination with an established sub-micrometer lithography technique like laser interference lithography [16] or using Talbot lithography [17] and by simply varying the bilayer thicknesses and the gold layer thickness, create nanopores with low-nanometer dimensions. We further demonstrated that the combination of a SiO_2/SiRN bilayer membrane prevents buckling caused by heating, which is needed to create the nanopores in the SiO_2 membranes by gold penetration.

Acknowledgments

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