On the Modelling and Optimisation of a novel Schottky based Silicon Rectifier

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***Abstract*—The charge plasma (CP) diode is a novel silicon rectifier using Schottky barriers, to circumvent the requirement for doping and related problems when small device dimensions are used. We present a model for the DC current voltage characteristics and verify this using device simulations. The model revealed an exponential dependence of the current on the metal work functions. And approximate linear dependence on the device geometry. The model is used to optimise the device performance. We show a factor 30 improvement in on/off current ratio (and hence rectification) toward 10E7 by appropriate sizing of the lateral device dimensions at given specific metal work functions.**

I. Introduction

Rectifying pn-junctions are essential in nearly every electronic component. In recent years, these junctions have been downscaled to such dimensions that doping control has become a major issue. In particular, doping fluctuation [1] and [2], doping activation [3] and steep doping profiles that yield a low temperature budget have become difficult demands.

Alternatively, Schottky based devices in SOI are being investigated [4] in which abrupt source and drain contacts are formed between the metallic contact and the silicon body. An alternative to a Schottky based rectifier is the charged plasma (CP) diode [5] shown in Fig. 1 (a). Here two separate gates having different work functions are placed on top of a thin and lowly doped silicon body. The gates are isolated from the top of the body by a dielectric. Each of the metals forms a contact at the side of the silicon body. First realizations of this diode are presented in [6].

Recently this diode has been investigated using device simulations [7]. They concluded that the CP-diode shows good rectifying behavior depending on the dimensions and metal work functions. In this work we present a model and compare this with device simulations. Furthermore we optimise the rectifying behavior quantified by the on/off current ratio.

II. Theory

1) Thermal Equilibrium: For a well chosen cathode gate work function $\phi_{\rm mc}$ an elevated electron concentration (n) is induced in the underlying silicon body, here referred to as electron plasma. The hole barrier height at the cathode silicon interface is given by $\phi_{\rm bc} = \chi_{\rm Si} + E_{\rm g} - \phi_{\rm mc}$, where $\chi_{\rm Si}$ is the silicon electron affinity and $E_{\rm g}$ the silicon band gap. The anode work function $\phi_{\rm ma}$ on the other hand induces a hole plasma. The electron barrier height at the anode silicon interface is given by $\phi_{\rm ba} = \phi_{\rm ma} - \chi_{\rm Si}$. Fig. 1 (b) shows a schematic band

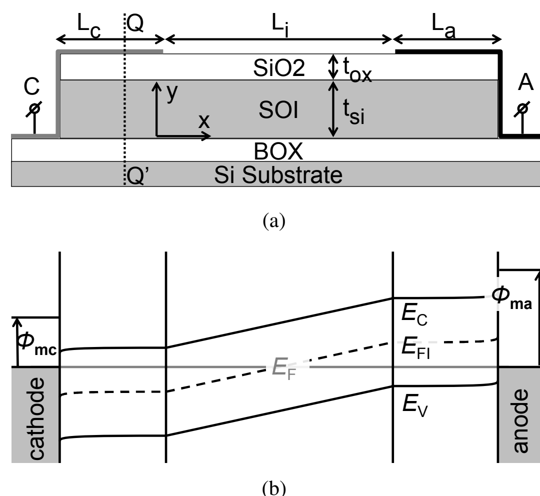

Fig. 1. (a) schematic cross section of the CP-diode, the cathode gate with length $L_{\rm c}$ induces an electron plasma due to $\phi_{\rm mc} < \chi_{\rm Si} + E_{\rm g}/2$. The anode gate with length $L_{\rm a}$ induces a hole plasma because $\phi_{\rm ma} > \chi_{\rm Si} + E_{\rm g}/2$. $L_{\rm i}$ is the length of the intrinsic region. (b) schematic band diagram of the CP-diode in horizontal direction just underneath the oxide.

diagram along a horizontal axis through the silicon. On the cathode side the Fermi level is close too the conduction band, indicating a high n. A high hole concentration (p) is formed at the anode side. The center region is not influenced by a gate and is lowly doped. Thus, there is hardly any charge present and the electric field is almost constant ($\frac{dE}{dx} = \rho/\epsilon$).

Fig. 2 shows a band diagram along the vertical dimension through the cathode of the CP-diode. The electron Schottky barrier between the SOI layer and cathode is relatively low because of the electrostatic effect. Let us neglect the influence of the buried oxide, silicon substrate (valid when $t_{\rm box} > t_{\rm ox}$), interface states and oxide charge. Also we neglect image force barrier lowering [8](important for high electric fields) and tunneling (important for very short regions). In the cathode region a positive charge is formed, the concentration of which varies along y.

To derive $n(y)$ it is necessary to have solution for the potential, for intrinsic silicon this is given by $q\Psi(y) = E_F - E_{Fi}(y)$. A similar problem shows up for the inversion charge in the subthreshold regime of a double gate MOSFET. This was presented earlier [9], [10] being,

$$\Psi(y) = \Psi(0) - 2u_{\rm T} \ln\cos(\beta y), \qquad (1)$$

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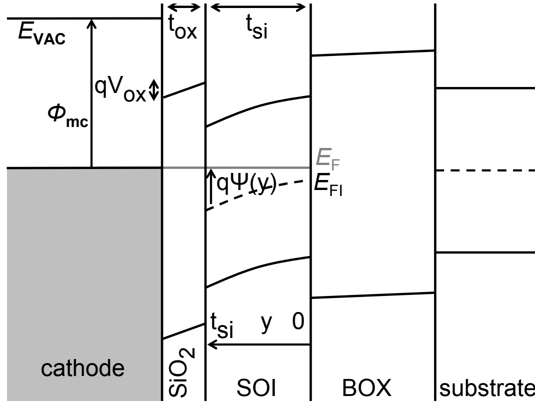

Fig. 2. Schematic band diagram taken along QQ' in Fig. 1 (a). The cathode work function $\phi_{\rm mc}$ pulls the silicon bands downward inducing an electron plasma. A low metal work function, thin oxide and silicon layers clearly result in an elevated electron concentration in the SOI.

here $u_{\rm T}$ is the thermal voltage, $\beta = \sqrt{exp(\Psi(0)/u_{\rm T})\delta/2}$, $\delta = n_{\rm i}/\epsilon_{Si}u_{\rm T}$ is a measure for influence of carriers on $\Psi(y)$ and ϵ_{Si} is the dielectric constant of silicon. The band diagram illustrates that the work function difference is equal to the potential drop across the oxide $V_{\rm ox}$ and the potential at the oxide silicon interface $\Psi(t_{\rm si})$. Furthermore the dielectric displacement at this interface is constant. Hence

$$\Psi(0) = \phi_{ms} - t_{\rm ox}\frac{\epsilon_{Si}}{\epsilon_{ox}}\frac{\delta\Psi}{\delta y} - 2u_t \ln\cos(\beta y)|_{y=t_{\rm si}}. \quad (2)$$

This equation can be solved numerically to find $\Psi(0)$. Note that we neglect the influence of the substrate. The highest minority concentration mainly determines the diffusion current density J, therefore, we use $y = 0$. The electron concentration under the cathode gate is given by $n_{\rm c} = n_{\rm i}\exp\frac{\Psi(y)}{u_{\rm T}}$ and the hole concentration by $p_{\rm c} = n_{\rm i}^2/n_{\rm c}$. Analogously the carrier concentrations under the anode gate ($p_{\rm a}$ and $n_{\rm a}$) can be found.

2) Reverse and small forward bias: Fig. 3 (a) shows the schematic band diagram along the silicon body for a small bias on the anode. Following the conventional p-n junction theory, [11] and [12], the majority quasi Fermi levels $E_{\rm Fn}$ and $E_{\rm Fp}$ are constant because the current is limited by minority carrier diffusion (constant J). Under the gates the majority quasi-Fermi levels are fixed by the gate-semiconductor work function difference. Hence an anode bias V results in a shift $qV = E_{\rm Fn} - E_{\rm Fp}$. This raises the minority carrier concentration under the gates by a factor $\exp V/u_{\rm T}$. Which results in a diffusion current of both carriers in the gate regions.

At the silicon cathode interface the hole concentration is governed by the effective surface recombination rate ($S_{\rm p,eff} = A_p^* T^2/qN_{\rm V}$) [13], here A_p^* is the Richardson constant and T the temperature. Near the intrinsic region the hole concentration is increased by the applied bias. For the diffusion and thermionic emission J in the cathode region we find

$$J_p^{\rm c} = q\frac{p_{\rm c}\left(\exp\frac{V}{u_{\rm T}} - 1\right)}{L_{\rm c}/D_{\rm p} + 1/S_{\rm p,eff}}, \quad (3)$$

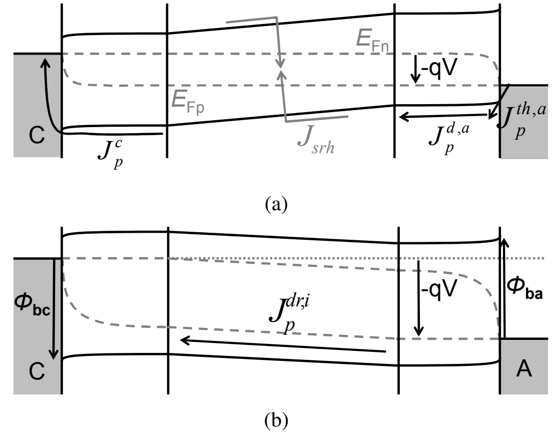

Fig. 3. Schematic band diagram of the CP-diode (Fig. 1) in horizontal direction of Fig. 1 just underneath the gates. (a) For small V the quasi Fermi levels $E_{\rm Fn}$ and $E_{\rm Fp}$ are splitted by a distance V. This results in thermionic emission and diffusion currents. Furthermore SRH generation/recombination could be taken into account. (b) For forward bias $V > V_{FB}$ drift through the intrinsic regions becomes important.

where $D_{\rm p}$ is the hole diffusion constant and k Boltzmann's constant. The hole concentration at the right hand side of the intrinsic region is high compared to the left hand side, see Fig. 3 (a). Hence we observe that holes can easily diffuse through this region and that this region doesn't affect the hole J.

3) Far Forward: When $V > V_{\rm FB} = \phi_{\rm ma} - \phi_{\rm mc}$, see Fig. 3 (b), the holes have to drift through the intrinsic region. The J is found by multiplying the hole concentration with the electric field,

$$J_p^{dr,\rm i} = \frac{n_{\rm i}\mu_{\rm p}q(V - V_{\rm FB})}{L_{\rm i}}e^{\frac{\phi_{\rm ba} - E_{\rm g}}{kT}}, \quad (4)$$

where $\mu_{\rm p}$ is the hole mobility and $L_{\rm i}$ the length of the intrinsic region. The potential is constant under the gate, hence holes diffuse through the anode region. The p at the anode metal interface is high compared to the anode intrinsic region interface hole concentration $p_{\rm a}$. As a result the diffusion component is given by,

$$J_p^{d,\rm a} = \frac{N_V q D_{\rm p}}{L_{\rm a}}e^{\frac{\phi_{\rm ba} - E_G}{kT}}, \quad (5)$$

where $N_V\exp(\phi_{\rm ba} - E_G)/kT$ gives the hole concentration (p) at the anode silicon interface. Holes travel by means of thermionic emission [14] from the metal anode into the silicon. The hole barrier at this interface is given by $E_{\rm g} - \phi_{\rm ba}$ resulting in a thermionic emission J,

$$J_p^{th,\rm a} = A_p^* T^2 e^{\frac{\phi_{\rm ba} - E_{\rm g}}{kT}}. \quad (6)$$

4) Current Model: The current components in Eqs. (3 - 6) are connected in series. Hence the smallest of them determines the total hole current density J_p^t. This can be modeled by

$$\frac{1}{J_p^t} \approx \frac{1}{J_p^{th,\rm a}} + \frac{1}{J_p^{d,\rm a}} + \frac{1}{J_p^{dr,\rm i}} + \frac{1}{J_p^{\rm c}}. \quad (7)$$

Analogously for the electrons J_n^t can be found. For negative or small positive biases the J may be far in excess from what is predicted by the diffusion and thermionic emission theory [15], [16]. This results from Shockley-Read-Hall generation/recombination which is modeled using theory from [17], [18]. We obtain

$$J_{\mathrm{SRH}} = \frac{q n_{\mathrm{i}} L_{\mathrm{i}}}{\tau_n + \tau_p}(e^{\frac{V}{2u_{\mathrm{T}}}} - 1), \tag{8}$$

where τ_n and τ_p are the electron and hole life time respectively. The total J can be found by summation of the electron, hole and SRH components.

III. Simulation

To evaluate our model we use the Synsopsys Sentaurus Device simulator [13]. The following models were used in the simulations: Schottky contact [19], electron effective density [20], hole effective density [21], carrier lifetimes [22], [23], enhanced Lombardi model for surface scattering and temperature dependent mobility [24] and Philips unified mobility model [25] for carrier concentration dependent mobilities.

Two different metal work function combinations were used in this work. Combination A ($\phi_{\mathrm{mc}} = 4.47$ eV, $\phi_{\mathrm{ma}} = 4.90$ eV) results from characterization of Schottky junctions fabricated in our cleanroom. Combination B ($\phi_{\mathrm{mc}} = 4.20$ eV, $\phi_{\mathrm{ma}} = 5.10$ eV) is chosen such that the metal work functions are very close to the silicon band edges, giving high carrier concentrations.

Fig. 4 shows the results. The theory predicts that for combination A the total off current is limited by the hole diffusion through the cathode region (J_p^{c}). The on current by diffusion through the anode region ($J_p^{d,\mathrm{a}}$). For A we also show a measurement result [6]. In general the characteristics are as expected, the differences can be attributed to differences in the metal work functions and the presence of interface states.

For combination B the currents are limited by both electron and hole diffusion. Due to the workfunctions being close to the band edges the diffusion current becomes rather small and the SRH current shows up for small or negative V.

In combination A the total current is determined by J_p^t, see Eq. (7). Current dependence on L_{a} and L_{c} is predicted by Eqs. (3) and (5). This dependence is shown in Fig. 5. Again the model is in good agreement with the simulation results. For long gate lengths the hole current is reduced so much that the electron current becomes important. This explains the reduced dependence on the gate lengths of the on and off currents for long gate lengths.

IV. Optimisation

The model can be used to optimise the rectifying performanceof the CP-diode. For a good rectifier we need at least: (1) a large maximum current through the device, (2) a high on/off current ratio. As shown in Fig. 5 scaling L_{c} and L_{a} helps to meet these requirements. In Figs. 6 and 7 the gate lengths have been scaled for combination A. The on current scales with L_{a}. When $L_{\mathrm{a}} < 10$ nm the on current

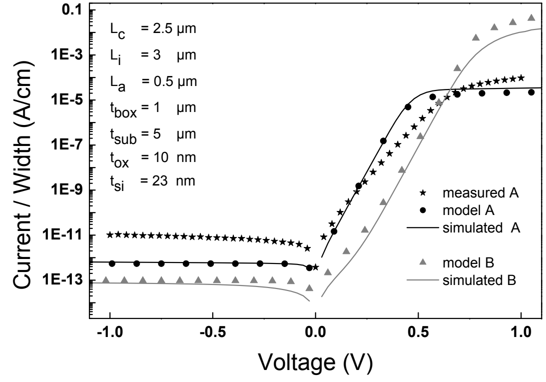

Fig. 4. Modeled and simulated IV characteristics for CP-diodes for work function combinations A and B. The dimensions are $L_{\mathrm{c}} = 2.5$ μm, $L_{\mathrm{i}} = 3$ μm, $L_{\mathrm{a}} = 0.5$ μm, $t_{\mathrm{box}} = 1$ μm, $t_{\mathrm{sub}} = 5$ μm, $t_{\mathrm{ox}} = 10$ nm and $t_{\mathrm{si}} = 23$ nm.

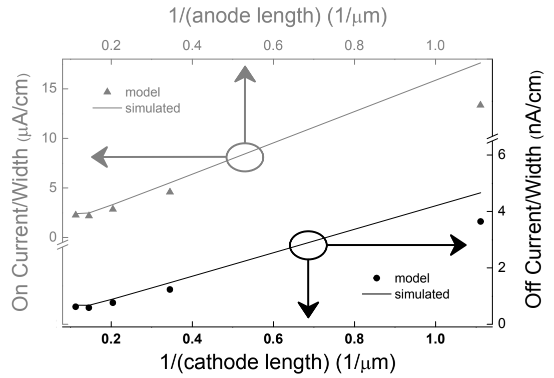

Fig. 5. The on and off current scaling with both gate lengths for combination A. The on current is extracted at $V = 1.5V_{\mathrm{FB}}$ and scales with $1/L_{\mathrm{a}}$. The off current is extracted at with $V_{\mathrm{FB}}/2$ and scales with $1/L_{\mathrm{c}}$. The device dimensions are $L_{\mathrm{i}} = 0.2$ μm, $t_{\mathrm{box}} = 1$ μm, $t_{\mathrm{sub}} = 5$ μm, $t_{\mathrm{ox}} = 15$ nm and $t_{\mathrm{si}} = 20$ nm.

is maximized and limited only by thermionic emission of holes from the anode, see Eq. (6). For very long L_{a} the electron current contribution becomes important and the L_{a} dependence becomes less.

The off current is determined by Eq. (3). Hence increasing L_{c} decreases the off current and results in an better on/off current ratio. For large L_{c} the electron off current becomes dominant and for small L_{a} the hole on current becomes limited by thermionic emission.

A short L_{i} is preferable because (1) the SRH current, Eq. (8), could enhance the off current, (2) the drift current, Eq. (4), could limit the on current. Regarding t_{si} and t_{ox}, good rectifying behavior is reached when both the cathode and anode region have a high carrier concentration, requiring a small t_{ox}. By tuning t_{si} a trade-off can be made between current level and reduced on/off current ratio.

For combination B the metal work functions are almost symmetric with respect to the silicon work function. Therefore, both the electron and hole current are equally important. Thus L_{c} and L_{a} cannot be used to optimise for either the hole or electron current. Here short gates results in a high on (and

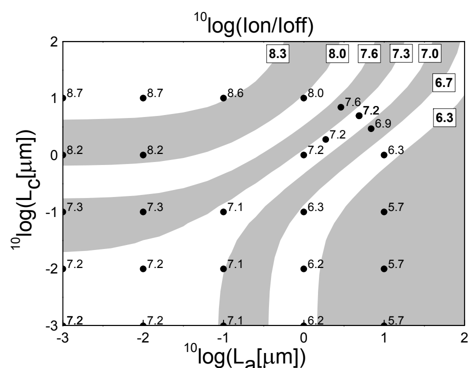

Fig. 6. Simulated (dots) and modeled (contours) on/off current ratio for combination A. Fixed parameters are $L_{\rm i} = 0.1, t_{\rm box} = 1, t_{\rm sub} = 5$ μm, $t_{\rm ox} = 15, t_{\rm si} = 20$ nm. Maximum on/off current ratio is obtained for short $L_{\rm a}$ and long $L_{\rm c}$.

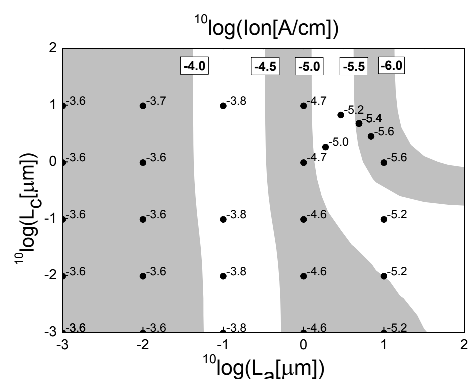

Fig. 7. Simulated (dots) and modeled (contours) on current for the same devices as in Fig. 6. Maximal on current is obtained for minimal $L_{\rm a}$ irrespective of $L_{\rm c}$.

off) current, but good on/off current ratio. Increasing both gate lengths result in a lower on and off current yielding a worse device performance.

However in a real CP-diode the metal work functions are unlikely to be symmetric with respect to the silicon work function and thus appropriate $L_{\rm c}$ and $L_{\rm a}$ sizing can improve the performance.

V. Conclusion

This work shows that the device dimensions of the CP-diode can be used to optimise the rectifying performance given the metal work functions. If the work functions are approximately equally distant from midgap, then a CP-diode without gates would give the best possible rectifier. However when the work functions are not equally distant from midgap finetuning the gate length gives an improved performance.

Our model can be used for optimizing the rectifying performance by adjusting the metal work functions, oxide and silicon thickness and lateral dimensions. For combination A (shown in Fig. 6) a maximum on/off current ratio of 5×10^8 was found, the on current is 1.2×10^{-4} A/cm and off current is 4×10^{-13} A/cm. Compared to the on/off current ratio of 1.5×10^7 for a device without gates this does yield an important improvement.

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