Trends and differences of the temperature effect on mismatch in different CMOS technology nodes

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Abstract

Statistical drain-current differences between pairs of supposedly identical transistors, usually known as matching, represent a crucial aspect of analog and mixed-signal circuits. Although matching has been a subject of study for more than two decades, how the temperature affects it is still scarcely discussed in the open literature [1,2]. In previous work, we discussed temperature effects on matching properties for a low-power CMOS 65-nm platform [1]. Measurements have been performed over a temperature range of 0 ◦C to 125 ◦C under several operating conditions. We discussed the temperature impact on relative current mismatch in the deep subthreshold region and the behavior of relative I_{ON} mismatch for individual pairs over temperature. Both subjects are important in modern circuit designs since the subthreshold region is often employed in ultra low-power circuits, while a drift in the individual pair mismatch can create problems in trimmed circuits.

In this paper we expand the original study by considering a wide span of technology nodes (140 nm to 45 nm). A broader range of device architectures and gate lengths is crucial for a better understanding of the physics behind the mismatch-temperature relation and propose consistent compact model solutions. The relative drain current mismatch is analyzed using fluctuation sweeps. In figures 1 and 2 an example of this comparison is shown. The device architecture has a big impact on the matching already at room temperature, for example in the case of NMOS for C45 (Fig. 1) the presence of the halos worsens the matching [3]. It is therefore interesting to see how such changes affect the temperature dependence. In this respect, trends of the threshold voltage mismatch and the relative current factor mismatch will be also shown.

In conclusion, this paper provides reliable information for circuit designers and system architects on the issue of the influence of temperature on mismatch based on a large set of measurements spanning different technology nodes.

Keywords: CMOS, fluctuation sweep, mismatch, temperature effect.

References:

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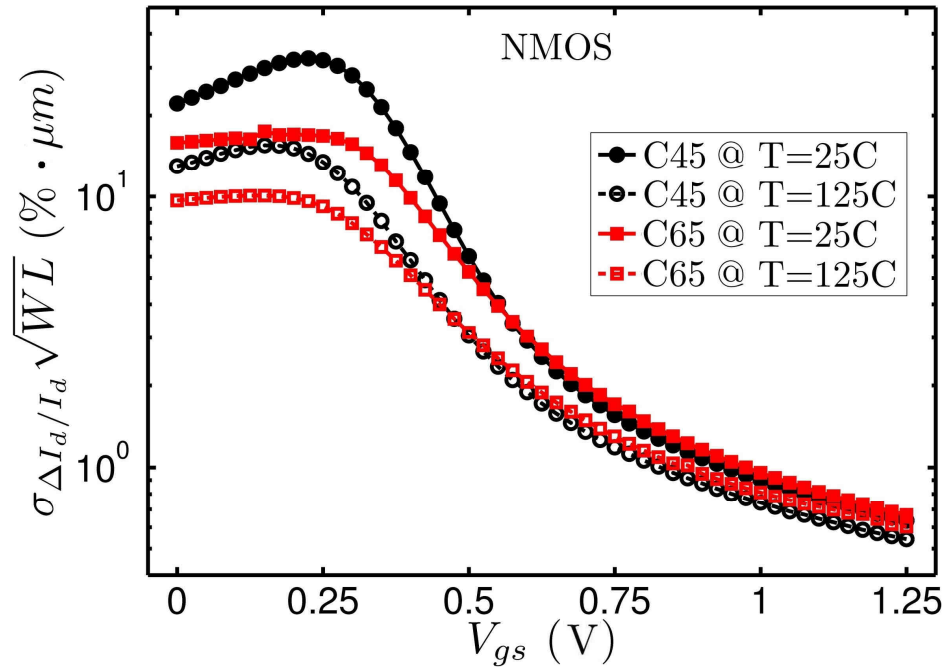

Figure 1. Relative drain current mismatch versus gate voltage (fluctuation sweeps) of NMOS devices for two temperatures and two different technology nodes. From this graph it is possible to notice that the temperature significantly affects the relative drain current mismatch in subthreshold and in minor quantity also in strong inversion region.

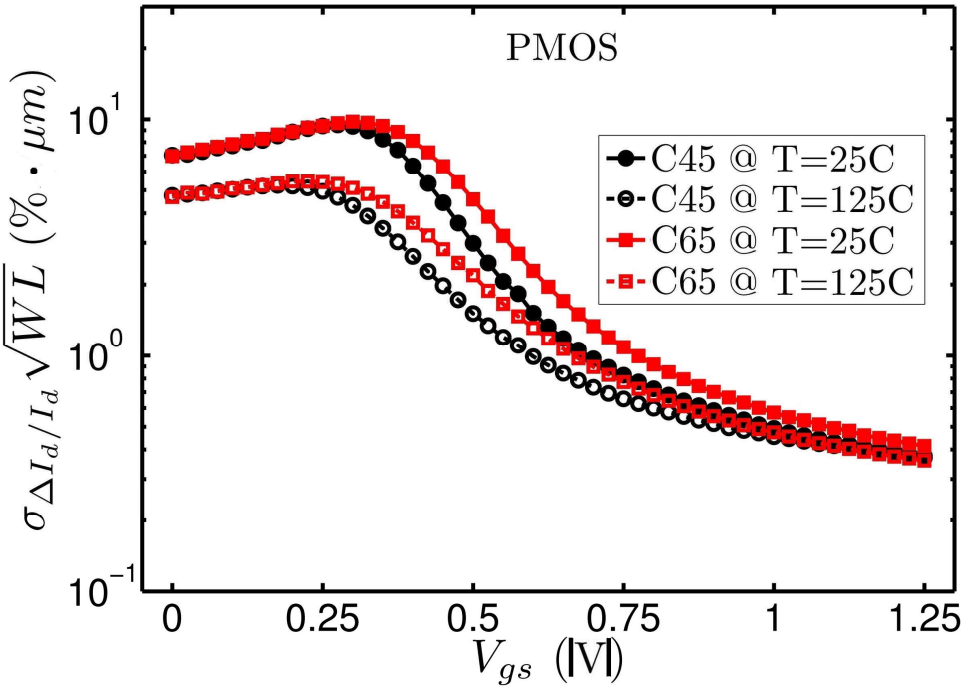

Figure 2. Relative drain current mismatch versus gate voltage (fluctuation sweeps) of PMOS devices for two temperatures and two different technology nodes. From this graph it is possible to notice that the temperature significantly affects the relative drain current mismatch in subthreshold and in minor quantity also in strong inversion region.