CHARACTERIZATION OF PIEZOELECTRICALLY ACTUATED PLD $Pb(Zr,Ti)O_3$ THIN FILM MEMBRANES

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***Abstract* — In our previous work, we presented a novel technique for fabricating Transmission Electron Microscopy (TEM) chips in order to investigate structural and piezoelectric properties of Pulsed Laser Deposited (PLD) Lead Zirconium Titanate ($Pb(Zr,Ti)O_3$) (PZT) thin films [1].**

We accomplished the fabrication of the devices we presented last year and obtained fully functional PLD PZT membranes. In this paper, we present the results of the fabrication process, which involves silicon-on-insulator (SOI) wafer technology together with deep reactive ion etching (DRIE) and highly selective etchants. In addition, we demonstrate the functionality of the membranes by piezoelectric actuation and characterized a selected membrane design through a set of experiments including X-ray diffraction (XRD), residual stress and frequency analyses.

***Keywords :* Lead Zirconium Titanate (PZT), Pulsed Laser Deposition (PLD), MEMS, Thin Film Membrane, Residual Stress, Frequency Response.**

I - Introduction

Piezoelectric materials are widely used in microelectromechanical systems (MEMS) applications including sensors [2] and actuators [3]. Among these, Lead Zirconium Titanate (PZT) is the most commonly used material due to its excellent ferroelectric and piezoelectric properties [4]. There exist a number of different methods for depositing PZT [5-8]. Here, we use Pulsed Laser Deposition (PLD), which enables deposition of large area PZT thin films, with excellent piezo- and ferroelectric properties [9, 10].

In this paper, the method for fabricating PLD PZT thin film membranes is revised with respect to our previous method [1]. Moreover, we present the results of the X-ray Diffraction (XRD), residual stress and frequency analyses on a selected membrane design, which has a 50 µm square shape. Finally, we conclude he article by mentioning about the future work on characterization of the membranes and the TEM experiments to be performed also in-situ.

The chips fabricated using this technique will enable investigation of the PZT membranes from the top, through their thickness. Top view TEM has many advantages over cross-sectional TEM, such as the possibility of determining the crystal size, revealing the diffraction patterns perpendicular to the plane and observing grain boundaries, crystal defects and such. Moreover, there is no need for modifying or damaging the structure to be investigated. Most importantly, the chips fabricated during this study will enable in-situ investigation of the membranes during actuation.

II – Design

A. Chip Design

The PLD PZT membrane chips are designed to fit into a standard TEM holder. This requires a diagonal length smaller than 3.05 mm. We selected a square shape with a side length of 2.1 mm for the chips, where the diagonal length is ~3 mm. The thickness of the chips is ~0.4 mm (Figure 1 (a)).

The chip boundaries are defined by 10 µm-wide, 7µm-deep v-grooves through the device layer on the top. Matching 20 µm-wide, 80-100 µm-deep grooves are also present at the backside, through the carrier wafer. These grooves enable easy breaking of the individual chips and eliminate dicing. A square PLD PZT membrane is located at the center of each chip. These membranes are composed of 20 nm Lanthanum Nickel Oxide ($LaNiO_3$) (LNO) as a seed layer and 100 nm-thick PZT thin film, with their side length varying in the range from 5 µm to 75 µm. This enables investigation of the effect of size on the properties of the membranes. In this work, we present the results of the experiments performed on a 50 µm square membrane.

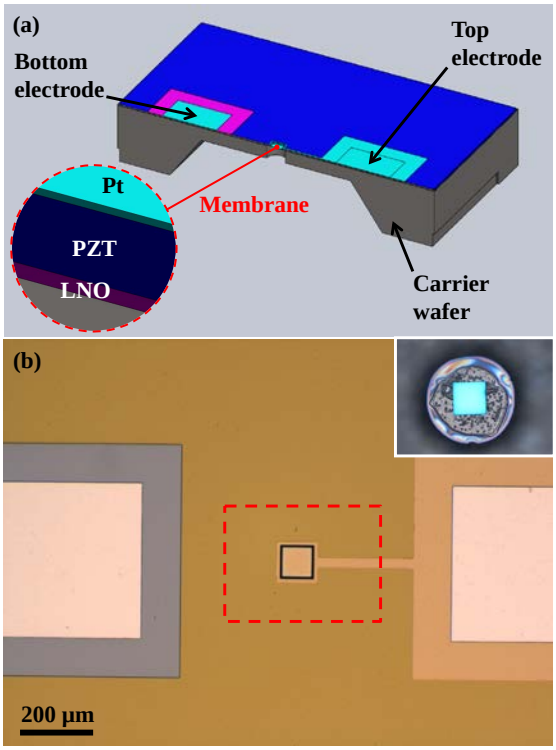

Figure 1*: (a) An illustration showing the cross-section of the PLD PZT membrane chip with the close up view of the membrane stack. (b) Optical micrograph of the fabricated membrane chip with the bottom view of the highlighted area in the inset.*

A two-step backside hole at the backside provides access to the PLD PZT membranes: A 300 µm-deep, 1 mm square groove and a ~85 µm–deep, 125 µm-diameter circular hole (Figure 1(b) inset). The two-step hole is preferable over a single high-aspect-ratio hole since the electrons do not travel through a confined region. Hence, the two-step hole will not result in a decrease in the quality of the TEM images.

The chip design includes top and bottom electrodes as well as corresponding contact pads (Figure 1 (b)), which enable actuation of the membranes, also during TEM investigation.

B. Process Design

Fabrication of the above mentioned chip design requires proper selection of the techniques and the process parameters to be used.

First step of the process design is the selection of the carrier wafer. We preferred to use a silicon-on-insulator (SOI) wafer in this work, in order to take advantage of the buried oxide (BOX) layer as an etch step during the backside deep reactive-ion etch (DRIE) and eliminate any non-uniformity during this step. In addition, both the BOX layer and the device layer provide strength to the PLD PZT membranes during this DRIE step and the breaking of the individual chips.

The usage of the SOI wafer technology also enables precise control of the size, shape and location of the membranes by etching rectangular grooves in the device layer. However, these grooves should not be etched through the device layer in order to grow better quality PLD PZT directly on the single crystalline silicon.

Another important step is the selection of the materials for the top and bottom electrodes. The LNO seed layer is conductive, and hence, it can also be used as the bottom electrode for the membranes. This requires selective etching of the PZT layer with respect to the LNO layer, which is possible with an a ammonium chloride-based etch solution.

Realization of metal top electrodes is rather straightforward through a lift-off process. Hence, a 5 nm-thick platinum layer is selected to serve as the top electrode.

As mentioned in the previous section, a two-step etch enables access to the PLD PZT membranes from the backside. The larger square groove is realized by anisotropic wet etching of the carrier wafer, whereas the smaller circular hole is realized by DRIE.

Most of the steps in the designed process are to be performed on a pre-patterned wafer. For this reason, the photolithography steps are performed using the spray coating technique with AZ4999 in order to achieve a uniform step coverage.

III – Fabrication

Fabrication of the PLD PZT membrane chips start with a 4-inch SOI wafer with <100> orientation (Figure 2(a)). The thicknesses of the device layer, the BOX and the carrier wafer are 10 µm, 0.5 µm and 385 µm, respectively.

Initially, the wafers are coated with a 300 nm-thick low-stress, low-pressure chemical vapor deposited (LPCVD) silicon-rich silicon nitride (SiRN) layer. The silicon nitride layer at the backside is then patterned by a reactive-ion etch (RIE) step to serve as a mask for the anisotropic wet etch of the 300 µm–deep square grooves in a 25 wt% KOH solution at 75 °C (Figure 2(b)). Then, the SiRN layer on the front side is patterned similarly by RIE and the 7-µm deep rectangular grooves, which define sizes and locations of the PLD PZT membrane, are realized within the device layer using a similar wet anisotropic etch step (Figure 2(b)).

Following the removal of the SiRN layer in a 85% phosphoric acid solution at 180°C, the 20 nm/100 nm-thick LNO/PZT layer is deposited by PLD at 600 °C on the front side of the wafer [9].

The LNO bottom electrode is patterned by etching the PZT layer in the area using the ammonium chloride –based etch solution. The etch is relatively fast, where the 100 nm-thick PZT layer is etched within 5 seconds. Following the realization of the bottom electrode, the top electrode is patterned by lift-off of a 5 nm-thick platinum layer. Both the 20 nm–thick LNO bottom

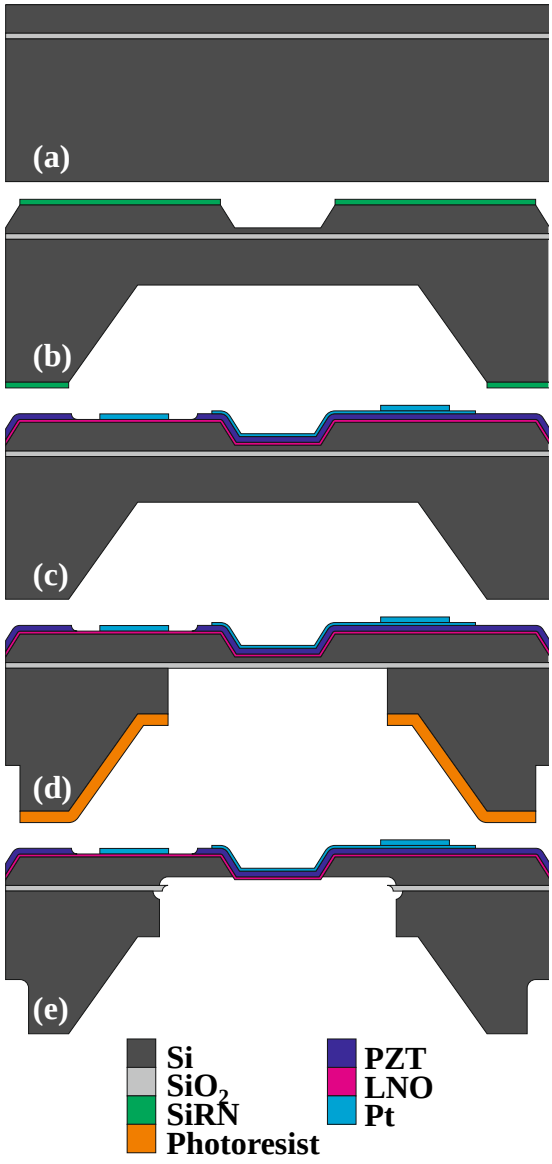

Figure 2*: Process flow for the PLD PZT membrane chip*

electrode and the 5 nm-thick platinum top electrode are relatively thin to establish electrical contact using needle probes. For this reason, 150 nm-thick platinum contact pads are realized again by lift-off, which concludes the front side processing (Figure 2(c)).

In order to access the PLD PZT membranes from the backside, 125 µm-diameter circular holes are defined through the carrier wafer by an SF_6-based DRIE etch step at -120 °C, where the spray coating photoresist is used as the mask (Figure 2(d)). During this step, the breaking grooves are also realized. Following the DRIE step, individual chips are broken and the process continues at the chip level by RIE etching of the BOX layer and the highly-selective gas phase XeF_2 etching of the remaining 3 µm-thick device layer.

Finally, stripping of the photoresist mask at the backside in oxygen plasma concludes the fabrication process (Figure 2(e)).

IV – Results & Discussion

A. *X-Ray Diffraction (XRD) Analysis*

A Bruker D8 Discover X-ray diffractometer with a Cu Kα cathode in the Bragg-Brentano geometry is used for analyzing the crystal orientation of the PLD PZT layer. The XRD scan reveals that the PLD thin film is a good quality PZT, where the dominant orientation is (100) (Figure 3).

B. *Membrane Deflection & Residual Stress*

Deflection of the PLD PZT membranes are measured by white light interferometry using MSA-400 micro system analyzer from Polytec. A majority of the membranes show an upwards deflection. The magnitude of the deflection varies in the range from 12 nm to 702 nm, depending on the size of the membrane. The deflection profile of the 50 µm square membrane is

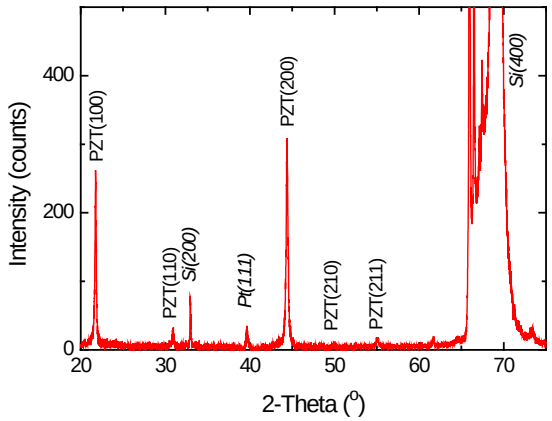

Figure 3*: XRD spectrum of the LNO/PZT thin film deposited on the (100) silicon surface.*

given in Figure 4.

The residual stress within this membrane is calculated to be 50 MPa using [10]:

$$C_1 \frac{t\sigma}{a^2} h + C_2(\upsilon) \frac{tE}{a^4} h^3 = 0 \qquad (1)$$

where, h is the center deflection, a is the half of the membrane's side length, t is the thickness, E is the Young's modulus (E=103 GPa [11]), σ is the residual stress, and υ the in-plane Poisson's ratio. C_1 and $C_2(\upsilon)$ are numerical constants.

C. *Frequency Analysis*

The piezoelectric frequency response of the 50 µm square PLD PZT membrane is obtained using scanning laser-Doppler vibrometry using MSA-400 micro system analyzer from Polytec (Figure 5). The resonance-frequency measurement is performed at the excitation voltage of 0.5 V_{ac} in the frequency range from 0 to 2 MHz. The first four resonances of the 50 µm membrane are obtained at 755 kHz, 1109 kHz, 1638 kHz and 1842 kHz, respectively. Corresponding mode shapes are obtained by exciting the 50 µm square membrane by applying a sinusoidal signal with a 0.5 V amplitude at each of these resonance modes (Figure 6). The resonance behavior of the measured device does not match with that of a perfect square membrane. This may be due to slight over-etch during the XeF_2 step, which can be solved by decreasing the etch time.

VI – Conclusions

In this work, we presented a novel method to fabricate PLD PZT thin film membranes with the ultimate aim to investigate the crystal structure of the material in-situ inside a TEM, under application of electric fields. The technique is based on utilizing SOI wafer technology and highly selective etchants. The proposed method can be adapted to many other thin film materials by proper selection of the etchants and the process parameters.

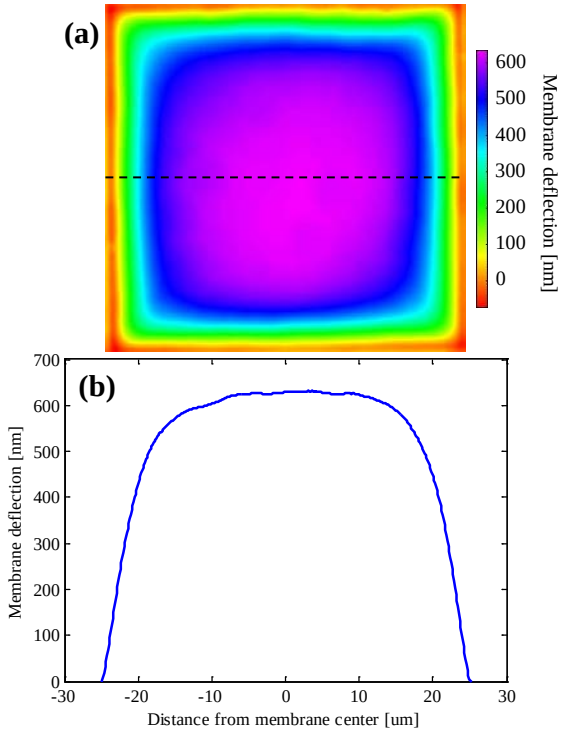

Figure 4*: (a) 2D plot showing the deflection of the 50 µm square membrane due to residual stress with (b) the deflection profile along the centerline.*

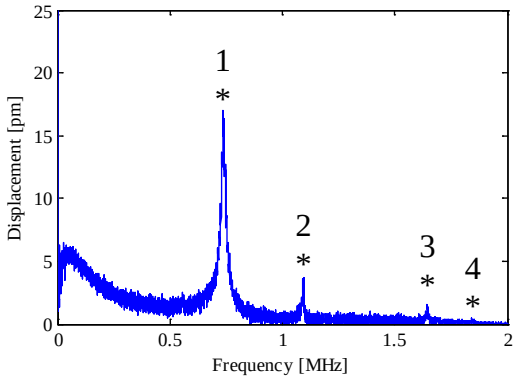

Figure 5*: Frequency response of a 50 µm square membrane using a periodic chirp signal.*

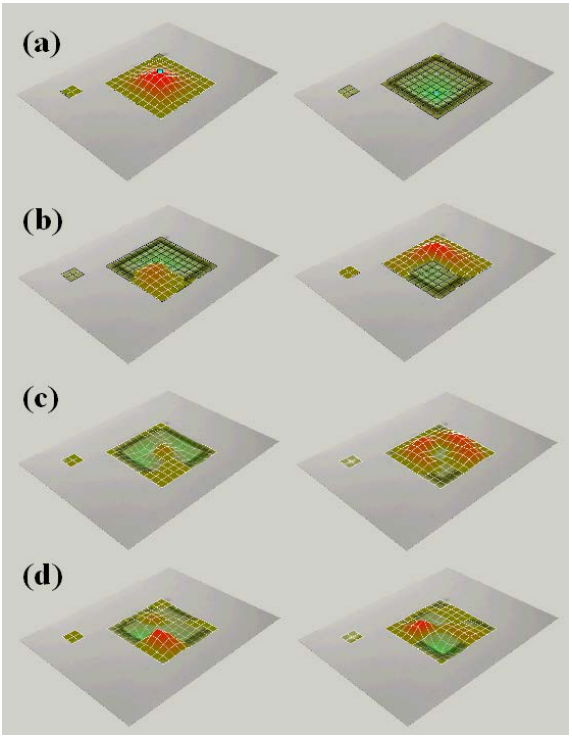

Figure 6*: Mode shapes of the 50 µm square membrane: (a) 1st mode at 755 kHz, (b) 2nd mode at 1109 kHz, (c) 3rd mode at 1638 kHz and (d) 4th mode at 1842 kHz.*

XRD spectrum reveals that the PLD PZT is a good quality film with (100) orientation. We observed that most of the membranes bend upwards when released. We also characterized the initial deformation and calculated the corresponding residual stress of a selected membrane with a side length of 50 µm. The deflection and the residual stress values for this membrane are 628 nm and 50 MPa, respectively.

We characterized the dynamic resonance frequency behavior of the selected 50 µm membrane by applying a periodic chirp signal. First four resonance peaks of the membrane appeared at 755 kHz, 1109 kHz, 1638 kHz and 1842 kHz, respectively. We determined the mode shapes of the 50 µm square membrane by applying a sinusoidal signal at each of these resonant frequencies, and hence, proven the functionality of the fabricated devices. The frequency spectrum of the measured device does not agree with that of a perfect square membrane. This problem may be eliminated by decreasing the etch time of the XeF_2 process.

The characterization work will be extended to the remaining membranes with different sizes as well as different thicknesses. At the same time with this characterization, the crystal structure of the membranes will be investigated inside a TEM and the optimum thickness for high-quality TEM imaging will be determined. Ultimately, the membranes will be actuated inside the TEM using a special holder with electrical connections and the change in the crystal structure will be investigated in-situ.

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