Stray-Insensitive Sample-Delay-Hold Buffers For High-Frequency Switched-Capacitor Filters

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I. Abstract.

Two high-frequency switched-capacitor sample-delay-hold (SDH) buffers are presented. The circuits provide a correct transition from the continuous-time to the discrete-time domain or vice versa.
Experimental results show an excellent frequency behavior for clock frequencies up to 25 MHz.

II. Introduction.

Switched-capacitor (SC) circuits are analog discrete-time signal processing circuits. At the front-end of these circuits, the continuous-time input signal has to be transformed into a discrete-time version. In order to optimize the settling speed of the SC circuit by creating step-input settling responses, the input interface circuit has to transform the continuous-time input signal into a uniform-sampled full period sample-and-hold (SH) signal. At the back-end of the SC circuit, the transition from the discrete-time to the continuous-time domain has to be made. Due to the finite circuit time constants of the SC circuit, the output signals will contain continuous-time transients, even for true full period SH input signals. An output interface circuit is required to sample the correct output signal values of the SC circuit at the ends of the settling periods and to transform the obtained signal sample sequence into a full period SH signal. Therefore, the use of these interface circuits is especially of advantage in high-frequency SC circuits.
The commonly applied interface circuit is the delay-free sample-and-hold buffer of figure 1a.

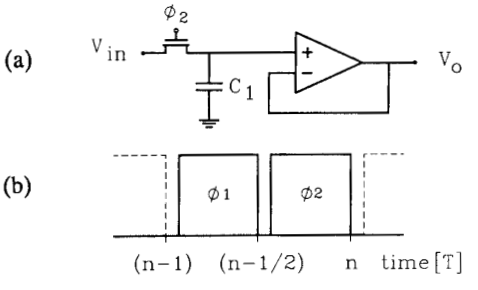

Figure 1. (a) Standard delay-free SH buffer.
(b) Timing diagram.

This and all other circuits described in this paper are controlled by a bi-phase 50% duty cycle clock pattern as shown in figure 1b. The tracking phase ϕ_2 causes a continuous-time input settling response of the amplifier during this phase. The realization of a full period SH signal requires a cascade of two delay-free SH buffers, driven by opposite clock phases. As shown in figure 2, requires the extension of this approach to obtain a SH signal during both phases (double-sampling) [1]-[3] three amplifiers.

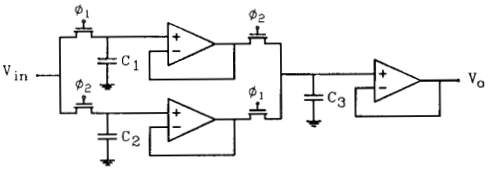

Figure 2. Standard double-sampling SH buffer.

This paper presents two novel input/output interface circuits, providing a full period SH output signal with the use of only one amplifier [3]. The introduction of a half period delay between the input and output signal samples guarantees an optimal step-input settling response of the amplifier.

III. Stray-insensitive sample-delay-hold buffers.

Figure 3 shows a stray-insensitive full period sample-delay-hold (SDH) buffer suitable for bi-phase single-sampling SC filters.

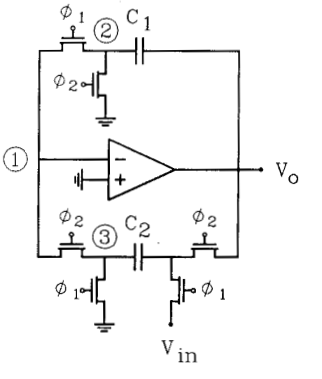

Figure 3. Single-sampling SDH buffer.

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The transfer function of this circuit can be found from the difference equations (1) and (2)

$$V_o(n)=\frac{C_2V_{in}(n-1/2)+Cp_1V_o(n-1/2)/A_o+V_{os}(C_2+Cp_3)}{C_2+[C_2+Cp_1+Cp_3]/A_o} \quad (1)$$

$$V_o(n-1/2)=\frac{[C_1+Cp_1/A_o]V_o(n-1)+V_{os}(C_1+Cp_2)}{C_1+[C_1+Cp_1+Cp_2]/A_o} \quad . \quad (2)$$

These equations include the effects caused by a finite open-loop gain A_O and the offset voltage V_{OS} of the amplifier and by the stray-capacitances at the circuit nodes 1, 2 and 3. Ideally, for $A_O \gg 1$, the output signal of the SDH buffer only changes value at the beginning of clock phase ϕ_2 and holds this value over a full clock period. Including the amplifier offset voltage V_{OS}, the SDH buffer output signal will contain an offset component equal to V_{OS} during clock phase ϕ_2 and two times V_{OS} during ϕ_1. Standard Fourier analysis shows that the output spectrum contains frequency components at DC (1.5 V_{OS}) and at all odd multiples n of the clock frequency ($2V_{OS}/n\pi$). For applications of the SDH buffer as output buffer, the latter are suppressed by a continuous-time smoothing filter. A double-sampling implementation of the SDH buffer is shown in figure 4.

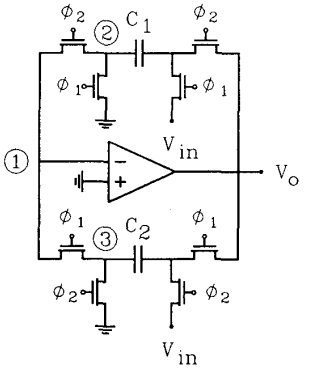

Figure 4. Double-sampling SDH buffer.

This circuit realizes the sample-delay-hold function during both clock phases. Assuming identical parasitic capacitances at the nodes 1, 2 and 3 in figures 3 and 4 and $C_1=C_2$, equation (1) is valid during both clock phases. Note that in the double-sampling implementation the sample frequency is twice the clock frequency. The amplifier offset voltage V_{OS} only causes a frequency component at DC in the output spectrum of the double-sampling SDH buffer with an amplitude V_{OS}. For $A_O \gg 1$, the periodic output spectrum of the ideal SDH buffers is

$$V_{OUT}(\omega) = \sum_{n=-\infty}^{n=+\infty} V_{IN}(\omega-n\omega_T)\,\frac{[1-e^{-j\omega T}]}{j\omega T}\,e^{-j(\omega-n\omega_T)T/2}$$

$$= \sum_{n=-\infty}^{n=+\infty} V_{IN}(\omega-n\omega_T)\,\frac{\sin(\omega T/2)}{\omega T/2}\,e^{jn\pi}\,e^{-j\omega T} \quad (3)$$

with a sample period T and $\omega_T=2\pi/T$.

For applications of the SDH buffers in the video frequency range, high-performance amplifiers with a transconductance in the order of several mA/V and a slew-rate in the order of hundreds of mV/ns have to be used. In order to prevent saturation of the amplifiers during the required non-overlapping time slots of the bi-phase clock pattern, the continuous feedback technique [4], shown in figure 5, will be added to both single- and double-sampling SDH buffers. During one of the on-periods of the clock phases ϕ_1 and ϕ_2, capacitor C_X degrades the performance in the same way as the parasitic capacitor at the negative input terminal of the amplifier. The capacitor C_Y just forms a small load capacitor for the amplifier. If both clock phases are off, the amplifier is switched as unity-gain buffer and the output signal will remain unchanged.

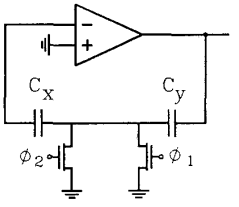

Figure 5. Continuous-time feedback circuit.

The clock feedthrough of both SDH implementations is primarily determined by the switches in this feedback circuit. The symmetry of the switch configuration at the amplifier inverting input terminal results in a first-order canceling of the output signal related clock feedthrough components as in double-sampling SC circuits. Assuming that the amplifier operates in its linear region, the clock feedthrough effects of the switches in the feedback loop can be described using the small-signal model shown in figure 6.

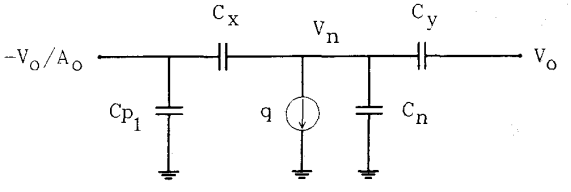

Figure 6. Small-signal model of the feedback circuit during the switch-off transients.

The charge source q models the total switch charge subtracted from the signal path during the time slot, starting at the beginning of the negative clock transition of either of the clock phases and ending as soon as the opposite clock signal reaches the threshold voltage. The capacitance Cp_1 models the input capacitance of the amplifier, C_n consists of the junction capacitances of the two switches and the total overlap capacitance of either of the switches that is in the off-state. The open-loop gain of the amplifier is again indicated by A_O.

The Kirchhoff current law gives the next equations

$$q = Cp_1V_o/A_o + C_y(V_o-V_n) - C_nV_n,$$
$$V_n = -(1+Cp_1/C_x)V_0/A_0. \quad (4)$$

From (4), the circuit node V_n is found to be a virtual ground for $A_O \gg 1$ and the total switch charge q will flow through C_Y. For fast switch-off transients, the switch channel charge will be distributed approximately equal to drain and source [5], resulting in

$$q \simeq (C_{ox}/2+C_{o1})(V_G-V_S-V_T) \quad (5)$$

for a single NMOS switch transistor with a total gate capacitance C_{OX}, a gate-drain and gate-source overlap capacitance C_{OL}. As the gate potential has reached the threshold voltage of the switch, an additional charge $C_{OL}(V_S+V_T)$ is subtracted from the signal path. The sample-delay-hold buffer becomes active again, as the opposite clock signal reaches the threshold voltage.
In most applications, the sample capacitor C_Y is much larger than the parasitic capacitors C_{OX} and C_{OL} and the clock feedthrough will not cause saturation of the amplifier. Due to the very small widths of the clock feedthrough pulses, the output spectrum components can usually be neglected. The assumption that the switch channel charges split equally to drain and source during the turn-off transient of the switch reduces the clock feedthrough mechanism into a linear function of the switch signal V_S. Any deviation from this 50% charge splitting will result in harmonic distortion. An accurate prediction of the clock feedthrough requires an accurate knowledge of all parasitic capacitances, the speed of the clock transients and the clock skew.

IV. Experimental results.

The single- and double-sampling SDH buffers have been realized using unit capacitances C_1, C_2, C_X and C_Y of 0.28 pF. The switches are realized with transmission gates consisting of 60/2.5 μm NMOS and 60/3 μm PMOS transistors. The widths of the switch transistors in the feedback loops are 30 μm. The amplifiers are BiCMOS folded-cascode transconductance amplifiers with an experimental DC-gain of 69 dB and a unity-gain frequency of 98 MHz. All circuits operate at a power supply of ± 2.5 V.
The gain responses of the SDH buffers have been measured for clock frequencies of 1, 5 and 25 MHz. Figure 7a shows the experimental gain response of the single-sampling SDH buffer for which the sample and clock frequency are equal. The experimental results of the double-sampling SDH buffer are shown in figure 7b for the same clock frequencies. The doubling of the sample rate is demonstrated clearly.

Figure 8 shows the phase response of the single- and double-sampling SDH buffer for a 25 MHz clock frequency. The ideal phase response $-2\pi f_{IN}/f_{SAMPLE}$, see (3), is met very closely.

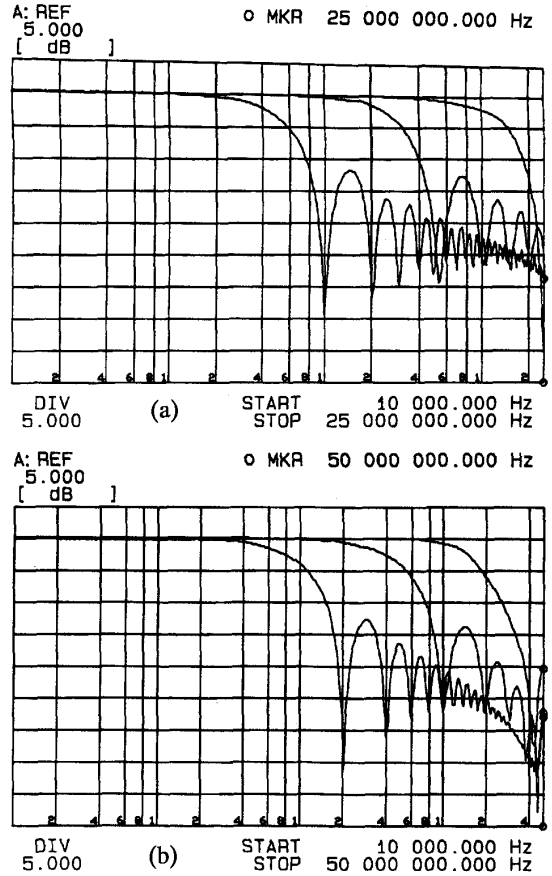

Figure 7. Experimental gain response of the SDH buffers (vert. 5 dB/div) for a clock frequency of 1, 5 and 25 MHz,
(a) single-sampling, (b) double-sampling.

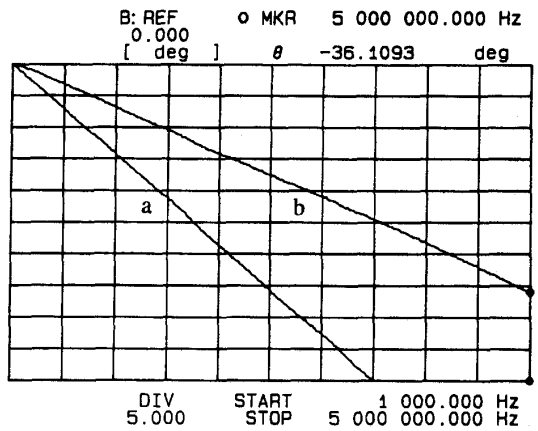

Figure 8. Experimental phase response of the SDH buffers (vert. 5 deg/div) for a clock frequency of 25 MHz,
(a) single-sampling, (b) double-sampling.

A typical experimental harmonic distortion curve HD_2 of both single- and double-sampling SDH buffer is shown in figure 9.

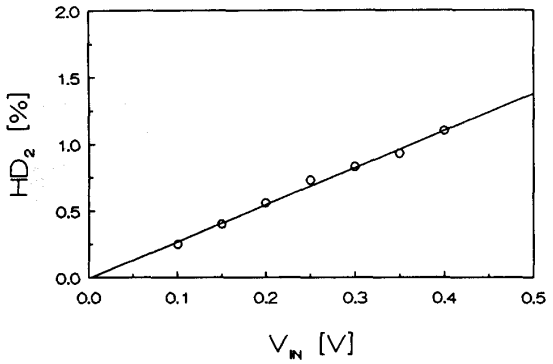

Figure 9. Experimental second harmonic distortion curve of the SDH buffers.

The total harmonic distortion consists primarily of second harmonics caused by non-linear clock feedthrough. The experimental third harmonics are typically 25 dB lower and originate from an on-chip continuous-time output buffer.
The experimental noise level including the noise of the output buffer is 0.3 $\mu V/\sqrt{Hz}$ for the double-sampling SDH buffer and 0.6 $\mu V/\sqrt{Hz}$ for the single-sampling SDH buffer. Using the data of figure 9, the dynamic range for 1% distortion is 52.5 dB for the double-sampling SDH buffer (bandwidth= 5 MHz) and 49.5 dB for the single-sampling SDH buffer (bandwidth= 2.5 MHz).
The experimental DC offset voltage is typically 70 mV for both single- and double-sampling SDH buffers. For a 25 MHz clock frequency, the spectral components at 25 and 50 MHz are respectively 12 mV and 60 mV for the double-sampling SDH buffer and 15 mV and 63 mV for the single-sampling SDH buffer. Referring section III, the symmetry of the switch configuration at the inverting amplifier input terminal of both SDH buffers makes the output referred clock feedthrough components mainly determined by the switch-off behavior of the switches in the feedback loops. These switches cause frequency components at the multiples of twice the clock frequency for both SDH buffers. A non-ideal cancellation of the switch charge injection of the switches connected to the amplifier input terminal results in frequency components at the odd multiples of the clock frequency. The difference between the 25 MHz clock frequency components of the single- and double-sampling SDH buffer, respectively 15 mV and 12 mV, originates from the amplifier offset voltage (typically 2.8 mV) as explained in section III.

Figure 10 illustrates the effects of the SDH output buffer on the frequency response of a video frequency SC filter operating at a 10 MHz clock frequency. The single-sampling SC filter has an ideal passband ripple of 0.5 dB and a ratio of the sample frequency to the filter cutoff frequency of 10 [3]. The reduction of the continuous-time output signal components caused by the settling behavior of the filter stages is shown clearly.

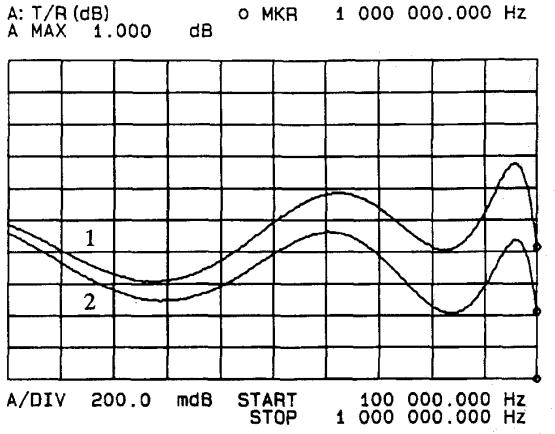

Figure 10. Experimental SC filter passband ripple (vert. 0.2 dB/div) for a 10 MHz clock frequency,
1: continuous-time output, 2: SDH output.

V. Conclusions.

Two stray-insensitive switched-capacitor sample-delay-hold buffers for video frequency applications are presented. Both buffers use only one amplifier and can be used as input or output stage for SC video frequency filters. The circuits can also be used as delay-cells for applications in discrete-time adaptive filter designs.

VI. Acknowledgements.

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VII. References.

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