A combined analogue+digital software defined radio receiver front-end for Bluetooth and Hiperlan/2

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Abstract— **The number of wireless communication links is witnessing tremendous growth and new standards are being introduced at high pace. However, circuit development is costly and time consuming due to mask costs and design iterations. Moreover, with ever-increasing radio standard complexity, these costs are increasing. This pleads for a Software Defined Radio approach, in which one piece of flexible radio hardware is re-used for different applications and standards, downloadable and under software control.**

A software defined radio receiver can -at different times- receive signals of a multitude of standards, obliviating the need to design, manufacture, stock and carry around separate receivers for all contemporary radio standards. The presented design includes both the analogue and the digital front-end. A CMOS integrated analogue downconverter containing a low-noise amplifier, downconversion mixers and filters performs all analogue processing required between RF pre-filters and the analogue-to-digital converter. The real-time baseband processing is partly implemented on an ASIC (channel selection) and partly on a standard PC (demodulation). Using a standard PC further enhances the flexibility of the design. The combined set-up is capable of receiving both Bluetooth and Hiperlan/2 signals.

We conclude that an analog wide-band front-end with a flexible Sample-Rate Converter (SRC) combined with appropriate software on an inherently flexible PC forms a feasible architecture for Software Defined Radio.

keywords: Software Defined Radio, HiperLAN/2, Bluetooth, Physical Layer, Radio Frequency, Wide-band front-end, MAP receiver, Demonstrator.

I. INTRODUCTION

In our SDR project we aim at combining two different types of standards –Bluetooth and HiperLAN/2– on one common hardware platform. HiperLAN/2 is a high-speed Wireless LAN (WLAN) standard [1], whereas Bluetooth is a low-cost and low-speed Personal Area Network (PAN) standard [2]. As is illustrated in table I the standards differ in several aspects and pose an interesting challenge for an SDR platform.

TABLE I
BLUETOOTH & HIPERLAN/2 PARAMETERS.

	Bluetooth	HiperLAN/2
System	PAN	WLAN
Frequency Band	2.4-2.4835 GHz	5.150-5.300 GHz, 5.470-5.725 GHz
Access Method	CDMA	TDMA
Duplex Method	TDD	TDD
Modulation Type	GFSK	OFDM
Max. Data Rate	1 Mbps	54 Mbps
Channel Spacing	1 MHz	20 MHz
Max Power Peak	100 mW	200 mW - 1 W

We focus on the radio front-end of a receiver, so from antenna (Radio Frequency (RF) signal) till and including demodulator (raw bits).

Our vehicle is a notebook to which we add SDR functionality. The analog front-end is made to be flexible and reconfigurable, see section II in which we present the wide band integrated front-end. The digital baseband part consists of a channel selection and sample-rate conversion part in flexible and reconfigurable hardware and a demodulator part with algorithms using GPP hardware, see section IV. We think the latter is feasible as current processors, such as the Pentium IV have huge processing capabilities. This capability is even increased due to special (signal processing) instructions such as SSE [3].

Most of the system-level design decisions were presented two years ago [4]. Last year we presented the designed demonstrator and discussed implementation choices [5]. In this paper, we present the results of experiments performed with this platform.

II. ANALOGUE FRONT-END

This section discusses the analogue part of our SDR front-end. A block schematic can be seen in figure 1.

As discussed in [4], the front-end uses separate anten-

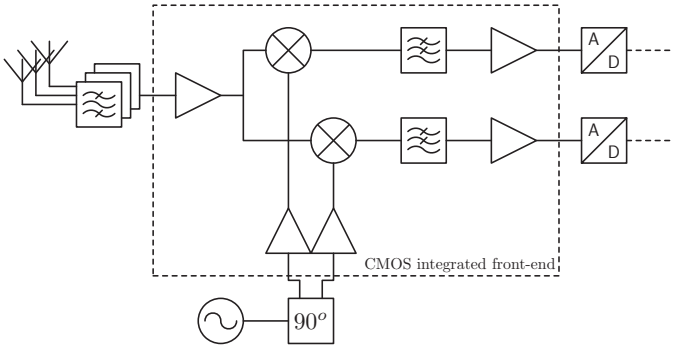


Fig. 1
ANALOGUE FRONT-END.

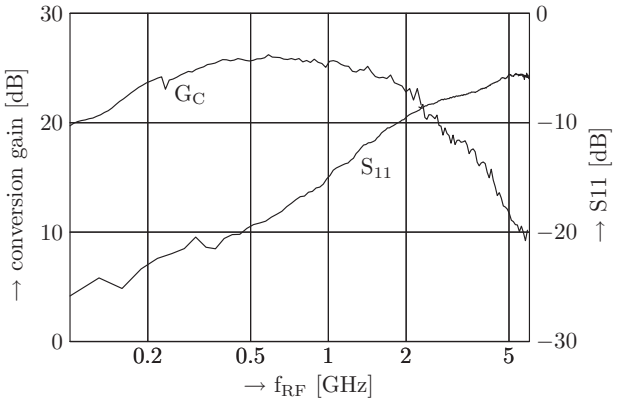


Fig. 2
VOLTAGE CONVERSION GAIN VS. INPUT FREQUENCY (OUTPUT FREQUENCY=5 MHz) AND S_{11} (V_{DD}=1.8 V)

nas and RF filters for the various bands. The rest of the receiver however, which should have a large bandwidth, is integrated. This way, the integrated circuit can still be used for a large number of applications, and only a new PCB with filters and possibly the antenna has to be designed when a receiver for a new frequency band is required.

The rest of the discussion in this section will focus on the part in figure 1 inside the dashed rectangle. For this part, an integrated circuit has been designed using a standard 0.18μm CMOS process. This front-end poses a strong technical challenge, as it has to work over a wide bandwidth of a few GHz, while satisfying high linearity and noise demands. We show that this is feasible in currently available CMOS IC-processes.

The circuit starts with a wideband low noise amplifier (LNA). This LNA employs noise cancelling, a recently published technique which is useful for obtaining a low noise figure over a wide bandwidth [6].

The LNA is followed by two mixers. Two local oscillator (LO) signals with a phase difference of 90 degrees are present. These implement quadrature down-conversion, enabling both zero-IF and low-IF architectures.

The two mixers are both followed by a low-pass filter with a cut-off frequency of around 10 MHz. This is more than enough for a single channel Bluetooth signal and sufficient for HiperLAN/2 signals.

Finally, the circuit contains two baseband amplifiers.

More information on the design can be found in [7].

III. EXPERIMENTAL RESULTS

The front-end was realised in a 0.18 μm standard CMOS process (figure 6). The active chip area is 800$\times$ 650 μm, most of which is taken by filter capacitors.

Measurements were done on a packaged chip (HVQFN24 package). It was mounted on a PCB made of Rogers RO4003 substrate with a thickness of 0.8 mm.

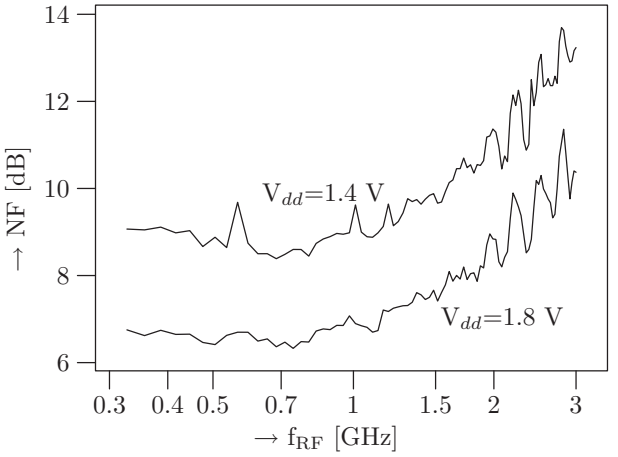


Fig. 3
NOISE FIGURE (TAKING IMAGE REJECTION INTO ACCOUNT) VERSUS INPUT FREQU ENCY (OUTPUT FREQUENCY=10 MHz)

Figure 2 shows the measured voltage conversion gain as a function of input frequency, showing 200 MHz–2.2 GHz −3 dB bandwidth. The lower cut-off frequency is determined by the coupling capacitors in the LNA. At higher frequencies the conversion gain is still considerable, albeit at increased noise figure. The same figure also shows S_{11}. This is lower than -10 dB up to 1.9 GHz.

Figure 3 shows the noise figure, at two different supply voltages. This is the noise figure when taking image rejection into account.

Figure 4 shows the output noise of the downconverter. This was measured using a differential probe. Note the 1/f noise corner frequency of <50 kHz.

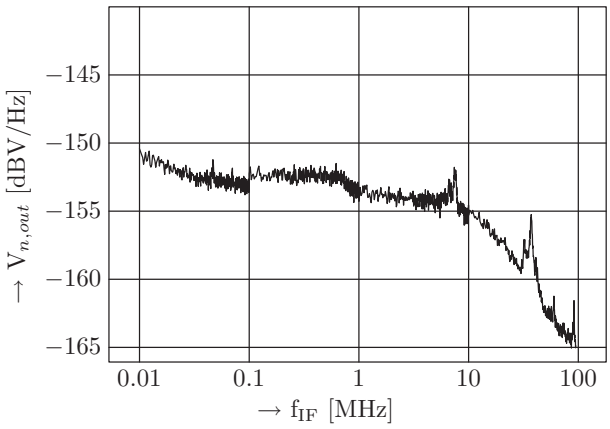


Fig. 4
OUTPUT NOISE VS. FREQUENCY. LO=1 GHz, V_{DD}=1.8 V

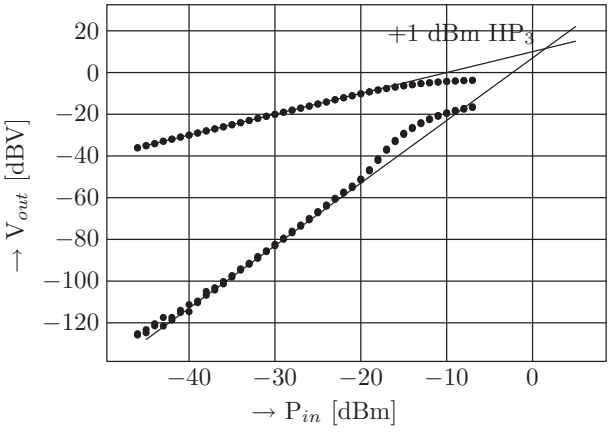


Fig. 5
TWO-TONE 3RD ORDER INTERMODULATION DISTORTION. INPUT AT 1005 AND 1006 MHz, V_{DD}=1.8 V.

	Vdd = 1.4 V[a]	Vdd=1.8 V
−3 dB BW	0.2 – 2.2 GHz	0.2 – 2.2 GHz
G_C	21 dB	25 dB
NF_{min}	8.5 dB	6.5 dB
IIP_3	+1 dBm	+1 dBm
IIP_2	+31 dBm	+35 dBm
−1 dB CP	-14.5 dBm	-16 dBm
LO radiation @1 GHz	-47 dBm	-47 dBm
P	130 mW	200 mW

[a] supply of LO buffers at 1.8 V

TABLE II
KEY PERFORMANCE MEASUREMENTS

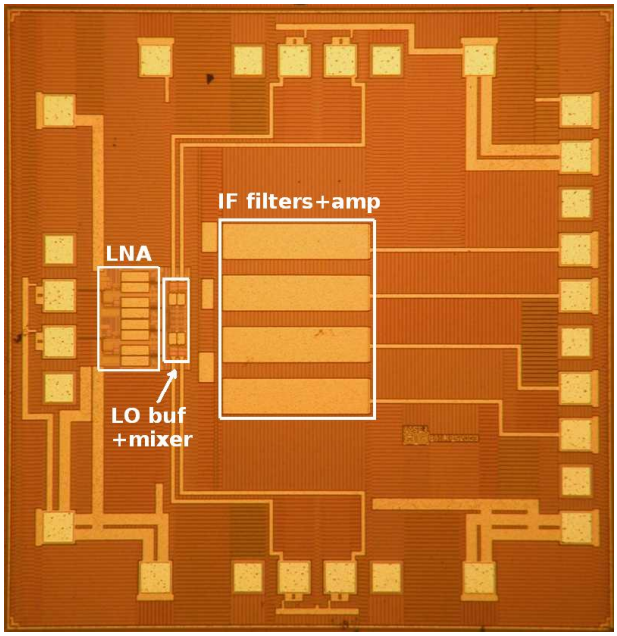


Fig. 6
CHIP MICROGRAPH

Figure 5 shows an IIP_3 plot, measured with an LO frequency of 1 GHz and two input signals at 1005 and 1006 MHz. The IIP_3 is +1 dBm (OIP_3: 13 dBV), which is considerably better than typically found for narrowband receivers. IIP_2 is +35 dBm and the -1 dB compression point is -16 dBm. A summary of the measurement results can be found in table II .

IV. DIGITAL PART

This section first presents the functional architecture of a Bluetooth-enabled HiperLAN/2 receiver [8]. Subsequently the real-time demonstrator for the digital part of the project is described.

A. Functional architecture

The Bluetooth standard is designed for low power and low cost receivers. Therefore a large part of the receiver is implemented in the analogue domain which does not map on a digital OFDM receiver. In our project we used a Maximum A posteriori Probability (MAP) receiver for Bluetooth. This receiver has better and even optimal performance compared with commonly used Bluetooth receivers [9]. Moreover this receiver can be mapped on the HiperLAN/2 receiver.

In our proposed SDR receiver (see figure 7), channel selection of the Bluetooth receiver has been integrated with the frequency offset correction and FFT of the Hiper-

LAN/2 receiver. Also, the HiperLAN/2 QAM demodulator (and FEC decoder) can be combined with the Bluetooth MAP receiver. More information can be found in [9] and [10]. This integration can also be seen in a wider scope. In fact, every phase-modulation standard can be integrated into an OFDM receiver. So, we expect that this SDR functional architecture can be used for other wireless LAN standards as well.

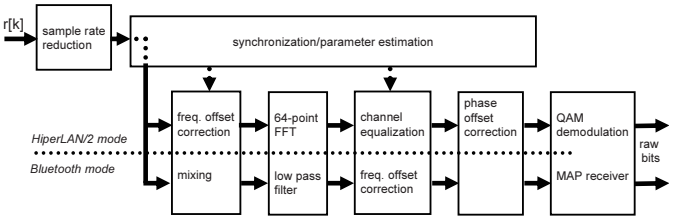


Fig. 7
DIGITAL PART OF A BLUETOOTH-ENABLED HIPERLAN/2 RECEIVER.

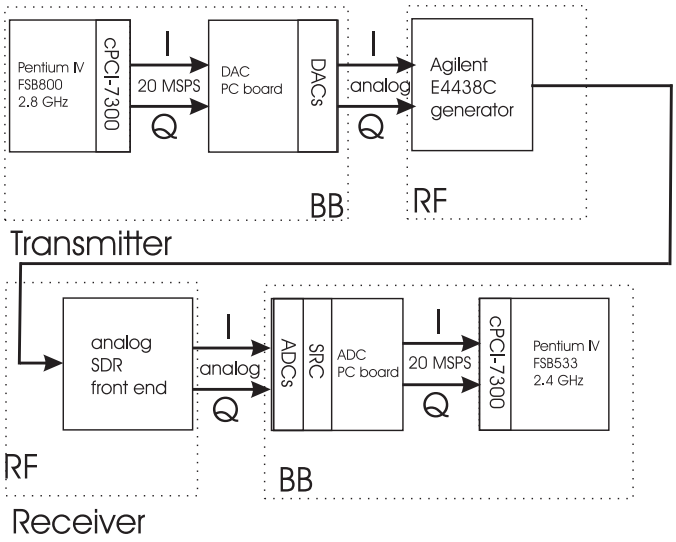


Fig. 8
SETUP OF THE REAL-TIME DEMONSTRATOR (SCENARIO FOR BANDPASS EXPERIMENTS).

B. Real-time demonstrator

The real-time demonstrator consists of two computers (transmitter PC and receiver PC) and two PC boards. This setup is depicted in figure 8. These two PC boards communicate with the computer through a digital I/O ↔ PCI interface (NuDAQ cPCI-7300A).

All baseband processing in the transmitter is performed by the computer and the baseband output is connected to the DAC PC board. This board contains an FPGA for communication with the computer, two DACs (20 MSPS) and analogue reconstruction filters.

The output of this board can be connected to a signal generator and our analogue front-end for bandpass-signal experiments, see figure 8.

The ADC/SRC PC board contains two ADCs (80 MSPS), a Sample-Rate Converter (SRC), Intersil ISL5416, that decimates the incoming (complex) 80 MSPS to a 20 MSPS signal and an FPGA for communication with the computer. Further signal processing is performed by the CPU of the computer.

C. Experiments

RF experiments have been performed with the setup of figure 8 and a picture of the testbed is shown in Figure 9. Because the used LO are very accurate, the frequency offset can be neglected. Therefore we have disabled the frequency-offset detection and correction algorithms in both receivers to achieve optimal results. Furthermore, the setup of figure 8 is not complete because

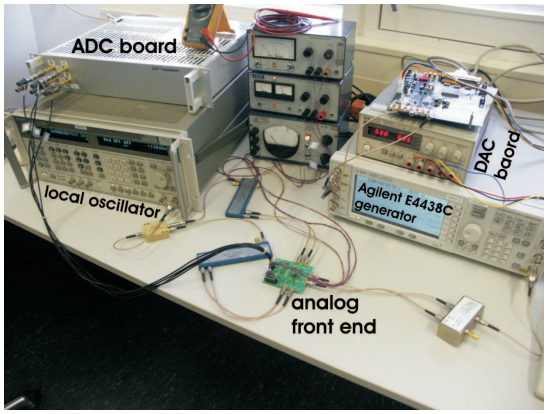
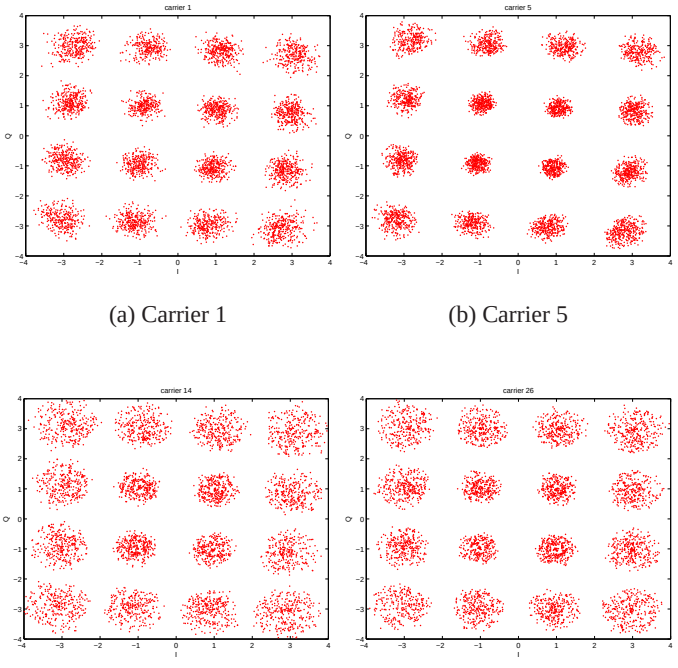


Fig. 9
PHOTOGRAPH FROM THE SETUP USED IN RF EXPERIMENTS (BOTH COMPUTERS ARE NOT SHOWN).

fully functional receivers also contain an analog AGC. In our setup, only the AGC of the Sample-Rate Convertor (SRC) in the digital domain is enabled, so weak signals will not use the full scale of the ADC. For this reason, the sensitivity requirements of both standards are not yet met. More research is required to implement this feature because it needs to know for example, the signal strength at the input of the ADC.

In Bluetooth mode, the receiver operates from -20.0 to -69.4 dBm signal strength[1] within the specifications of the standards i.e. the BER is below 0.1%. Figure 11

[1]We have calibrated the output of the Agilent generator by manually measuring the RMS value of the generator output.



(a) Carrier 1 (b) Carrier 5

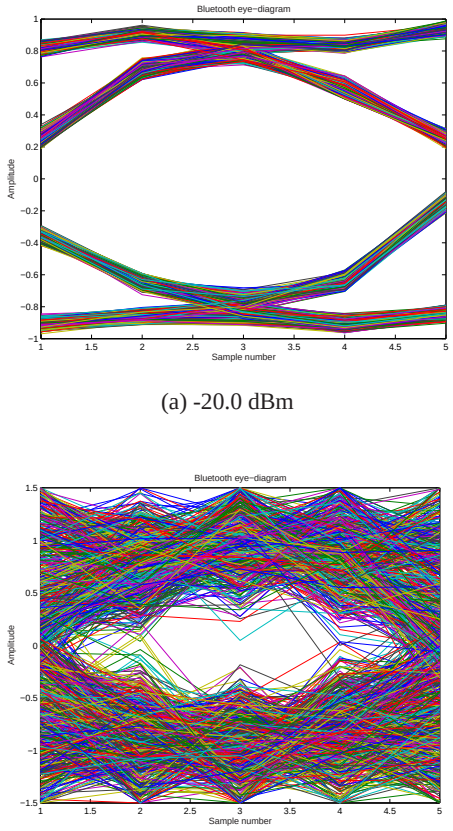
(c) Carrier 14 (d) Carrier 26

Fig. 10
RF EXPERIMENTS: 16-QAM CONSTELLATION DIAGRAMS FOR SEVERAL CARRIERS AT -40 DBM SIGNAL STRENGTH.

depicts the eye-diagram for both -20.0 and -69.4 dBm Bluetooth signal. The first eye-diagram is very open. With the weak signal at -69.4 dBm (sensitivity level: -70 dBm), the eye-diagram appears almost closed, but it still meets the Bluetooth 10^{-3} BER requirement.

In HiperLAN/2 mode, the receiver works for BPSK, QPSK and 16-QAM mode. In 64-QAM mode, the PER is larger than 10%. Figure 10 depicts the constellations of several carriers in 16-QAM mode just before demapping. It seems that for all carriers, the constellation points at the border of the constellation diagrams are more noisy than the inner points. Additional testing is needed, to find the cause of this distortion, but experiments indicate that this distortion is introduced in the ADC/SRC PC board. Furthermore, the analog circuit before the ADCs has a high-pass filter characteristic and its cut-off frequency is 400 kHz [11] whereas the carrier frequency of carrier 1 is 312.5 kHz. However, measurements in the analog circuit showed only a 0.1 dB attenuation at 312.5 kHz. Probably there are other reasons for this cut-off frequency and replacing the analog circuit may solve the problem.

Moreover, we have also conducted sensitivity tests for both standards, see Table III. In Bluetooth mode, the specification of the standard are almost met and in HiperLAN/2



(a) -20.0 dBm

(b) -69.4 dBm

Fig. 11
RF EXPERIMENTS: EYE-DIAGRAM OF RECEIVED BLUETOOTH SIGNAL.

Mode	**Required sensitivity**	**Measured sensitivity**
Bluetooth	-70 dBm	-69.4 dBm
HiperLAN/2 BPSK	-83 dBm	-71.0 dBm
HiperLAN/2 QPSK	-79 dBm	-66.0 dBm
HiperLAN/2 16-QAM	-73 dBm	-53.8 dBm
HiperLAN/2 64-QAM	-68 dBm	NA

TABLE III
SENSITIVITY TESTS

mode there is a large gap between requirements[2] and the performance of our SDR receiver. It is expected that implementation of an analog AGC in the testbed setup will improve these results dramatically. However, the design of an AGC is not easy, because it is a feedback system in both the analog and digital domain.

V. CONCLUSIONS

In this paper we outlined our SDR demonstrator. For this demonstrator we design and implement a wide-band analog front-end, a PCB with SRC/ADC and GPP software.

The combination of a wide-band analog front-end and GPP hardware is capable of receiving Bluetooth and HiperLAN/2 signals.

The testbed can be extended to other standards, because the only limitations in our testbed are the maximal channel bandwidth of 20 MHz, the dynamic range of the wideband SDR analog front-end and the processing capabilities of the used PC.

ACKNOWLEDGMENT

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[2] The maximum PER is 10% in HiperLAN/2 which equals a raw BER of about 10^{-3}. This value is an approximation because it depends strongly on the nature of the raw bit-errors and the used error-correction code.