A 7-8 GHz serrodyne modulator in SiGe for MIMO signal generation

Johan C. J. G. Withagen*, A. J. Annema*, B. Nauta*, F. E. van Vliet* †

*University of Twente, Enschede, 7500 AE, Netherlands, +31 53 486 2644, j.c.j.g.withagen@utwente.nl

†TNO, The Hague, 2509 JG, The Netherlands, +31 88 86 61 058, frank.vanvliet@tno.nl

Abstract—**An 8-bit 360° sawtooth modulated phase shifter is used to apply very small frequency offsets to RF signals between 7 and 8 GHz. Offsets between 6 Hz and ~10MHz can be obtained. Such frequency offsets can be used to generate orthogonal signals, which are required in e.g. MIMO applications. Each undesired frequency component is suppressed to below -30 dBc. The phase modulator is realized in a 250 nm SiGe BICMOS technology.**

Index Terms—**Phase Modulation, Radar, BICMOS intgrated ciruits, MIMO**

I. INTRODUCTION

Multiple Input Multiple Output (MIMO) radar transceivers [1], [2] require the generation of orthogonal signals. Orthogonality can be achieved by generating unique small frequency offsets at every array element. The simplified radar concept in Fig. 1 contains element-level waveform control, in this case a time-dependent frequency translation $\Delta f_N(t)$ in the RF domain. Mixers can perform this function, but would generate many harmonics and inter-modulation products near the carrier, since $\Delta f_N \lll f_{LO}$. Another issue of mixers is LO leakage to the output signal. In contrast, using a linear phase shift to change the frequency does not produce images and harmonics in band. It also minimizes LO leakage. In this paper a circuit is presented that can accomplish frequency shifts, based on linear phase shifting [3] which is suitable for this task.

II. CONCEPT

Modulating the phase $\phi(t)$ of a sinusoid linearly in time (i.e. $\phi(t) = k \cdot t$), translates the angular frequency of this sinusoid by k:

$$v_{out}(t) = V \cdot \sin(\omega_{in} t + \phi(t)) = V \cdot \sin((\omega_{in} + k)t). \quad (1)$$

The resulting angular frequency ω_{out} of the output signal is then a shifted version of the input frequency, $\omega_{out} = \omega_{in} + k$. As phase is periodic in 360°, a linearly increasing phase is equivalent to a sawtooth-shaped phase with a 360° amplitude; this latter is used in this paper. By replacing $\phi(t) = k \cdot t$ by any continuous function, any frequency translation or chirp, linear and non linear, can be generated. To obtain the phase shift, 1st order All Pass Filters (APFs) are used, each with the following transfer function [4]:

$$H(j\omega) = 2\frac{1}{1 + j\frac{\omega}{\omega_0}} - 1 = \frac{1 - j\frac{\omega}{\omega_0}}{1 + j\frac{\omega}{\omega_0}} \quad (2)$$

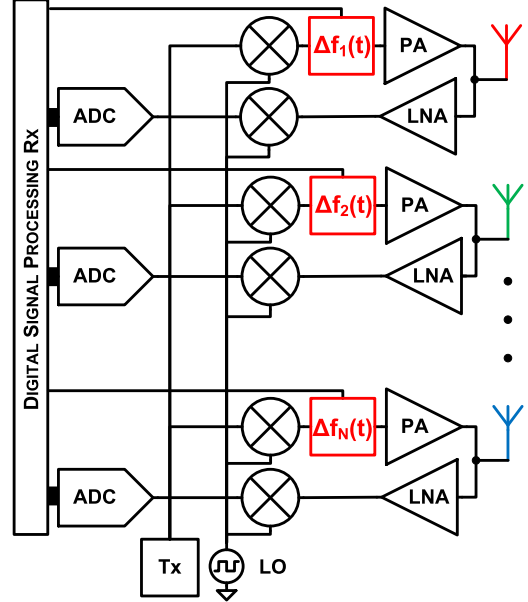The amplitude and phase transfer of these APFs are given by:

Fig. 1: Simplified time-multiplexed N-element MIMO pulsed radar array, with per-element waveform control, $\Delta f_N(t)$.

$$|H(j\omega)| = 1 \quad , \quad \angle H(j\omega) = \pi - 2\arctan\frac{\omega}{\omega_0} \quad (3)$$

The phase shift range of such APFs is theoretically 180°; in practical designs less than 180°. To shift 360° at least 3 APFs are needed. For symmetry purposes an interleaved combination of 4 APFs is used to achieve 360°, requiring 90° tuning range per APF. By adding two cross-bar switches, the differential structure of the phase shifter can be exploited to reduce the number of APFs to 2. Together with a polyphase filter and an output switch, a 360° phase shifter is obtained. The phase shifter structure is given in Fig. 2. "Path A" shifts phase from 0° to 90° and 180° to 270° and "Path B" shifts phase from 90° to 180° and 270° to 360°. In Fig. 3 phase sweeps to get a static frequency translation are plotted versus time. The output switch switches when the phase of signals from both APFs are equal, in order to prevent spurs by phase jumps. This is ensured by a period of time in which both tune sweeps overlap. The switches are implemented as soft switches. Combined with summing in the current domain, this results in the interpolation of phase errors. The cross-bar switches switch while the other APF is connected to the output, thus minimizing its influence on the output.
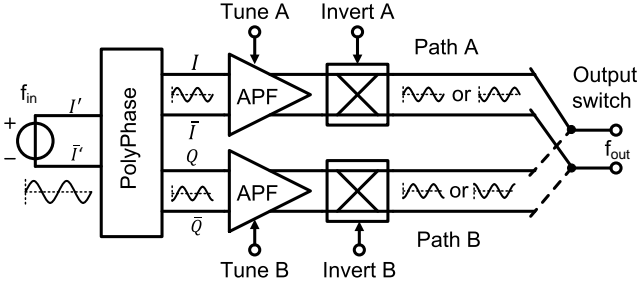
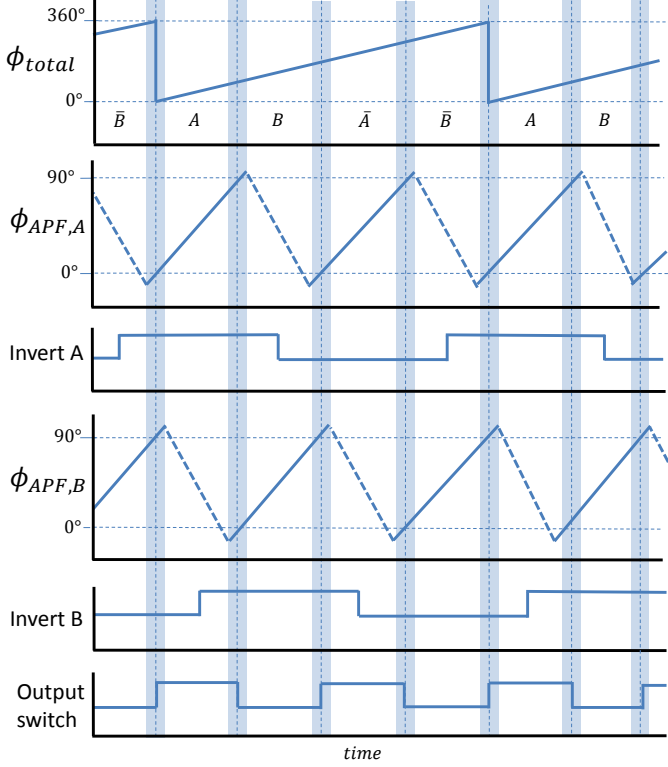Fig. 2: Structure of the 360 ° interleaved phase shifter.

Fig. 3: Phase shifter A and B are tuned and used interleaved in time to create a 360° phase shifter. The blue areas indicate where phase shifter A and B have the same output phase. The switches "Invert A" and "Invert B" switch when they are not connected to the output via "Output switch".
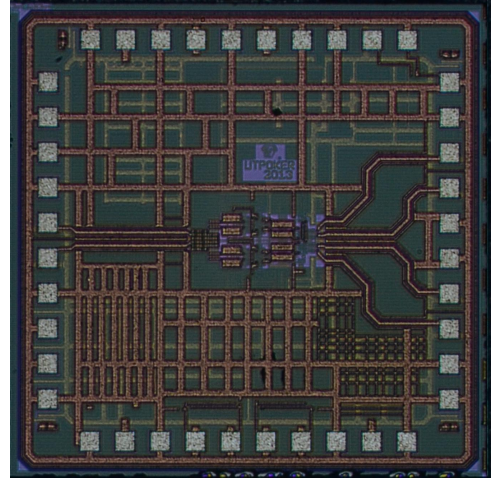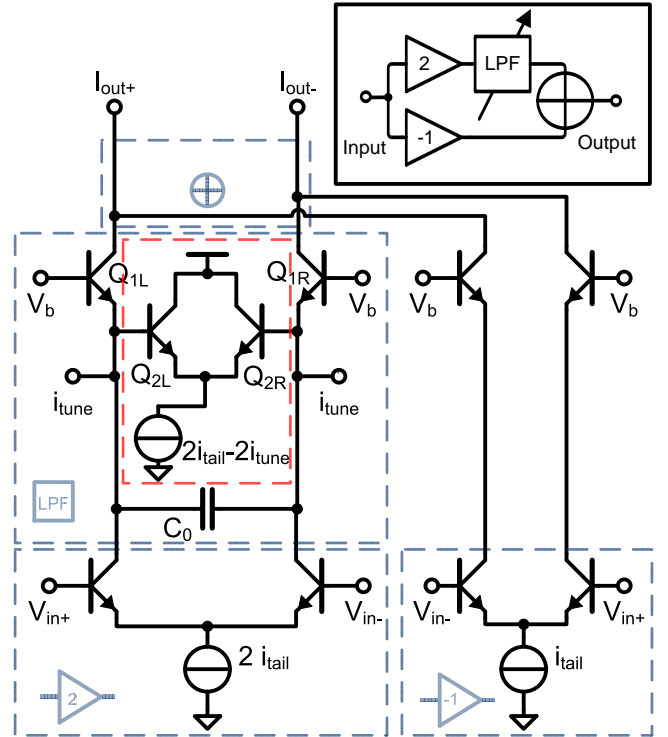

Fig. 4: Die photo. Chip measures 1.6mm x 1.6mm.

Fig. 5: Circuit implementation of the APF; blue insets represent the parts described in (2) and shown in the top level overview of the APF in the top right corner. The red box indicates the capacitance compensation circuit.

III. CIRCUIT IMPLEMENTATION

The circuit is implemented in a $0.25~\mu m$ BICMOS technology with Si-Ge bipolar hetero junction transistors (HBTs) with a f_t of 180 GHz; a die photograph of the chip is shown in Fig. 4. At the input a wide band 7-12 GHz polyphase filter is used to create a differential quadrature signal from the differential input signal. The four quadrature signals are fed to the two APFs, see Fig. 2; the architecture of an APF is shown in Fig. 5. The input signal of the APF drives both its differential pairs. The leftmost differential pair is biased at twice the bias current of the rightmost differential pair to achieve a gain ratio of 2:1. The negative gain in the right hand side part is implemented by swapping the input signal compared to the left-hand side.

The Low Pass Filter (LPF) is implemented by a gm-C filter created by the cascode transistors transconductance g_m and by a capacitance C between the cascode transistors emitters. Tuning the collector current $i_{tune} + i_{C,diffpair}$ of the cascode transistors, their transconductance is changed and therefore the cutoff frequency of the LPF, $\omega_0 = \frac{g_m(t)}{C(t)}$, is tuned. With (3) this yields

$$\phi(t) = \pi - 2\arctan\frac{\omega C(t)}{g_m(t)}. \tag{4}$$

HBTs are used in the APF, whose transconductance g_m is ideally given as

$$g_m(i) = \frac{i(t)}{V_t}. \qquad (5)$$

Here $i(t)$ represents the time dependent collector current through the device and V_t is the thermal voltage $\frac{q}{k_b T}$. The capacitance in (4) is mainly composed of capacitor C_0 and of the base-emitter junction capacitances of the cascode transistors; the latter are by good approximation linearly dependent on the collector current: $C_{be}(i_C) \approx i_C \cdot \chi$. The circuit can be operated both linearly for small input signals and can use large signals which essentially utilizes the differential pairs as current commuting switches. The resulting behavior and equations are similar. For simplicity reasons, the analyses in this paper assume linear operation. Then (4) can be rewritten as:

$$\phi(t) = \pi - 2 \arctan \frac{V_t \omega \left(2 \cdot C_0 + \chi(i_{tune}(t) + i_{tail})\right)}{i_{tune}(t) + i_{tail}} \qquad (6)$$

which can be rewritten into an equation that describes the heavily non-linear relation between $i_{tune}(t)$ and $\phi(t)$:

$$i_{tune}(t) = \frac{V_t \omega 2 C_0 \tan\left(\frac{\phi(t)}{2}\right)}{1 - V_t \omega \chi \tan\left(\frac{\phi(t)}{2}\right)} - i_{tail} \qquad (7)$$

Equation (7) shows that the current dependency of the base-emitter capacitance of Q_1, $C_{be,Q1}$, results in relatively large required $i_{tune}(t)$ ranges, which is to a large extent due to the current dependency of the C_{be} of the cascode transistors. In our design this dependency is compensated by the circuitry within the red box in Fig. 5. Here, an extra transistor, Q_2, is added and connected via its base to the emitter node of the corresponding cascode transistor. Operating this Q_2 at $I_{C,Q2} = I_{constant} - I_{C,Q1}$ with for example $I_{constant} = i_{tail}$, the capacitance $C(t)$ in (4) becomes:

$$C_1(t) = 2C_0 + \chi(i_{tail} + i_{tune}(t) + i_{tail} - i_{tune}(t)) \\ = 2C_0 + 2\chi i_{tail} \qquad (8)$$

Using this, (7) reduces to

$$i_{tune}(t) = V_t \omega C_1 \tan\left(\frac{\phi(t)}{2}\right) - i_{tail} \qquad (9)$$

Many $\phi(t)$ shapes can be constructed, all requiring a different $i_{tune}(t)$. To get a constant frequency shift, linear phase modulation $\phi(t) = kt$ is required resulting in

$$i_{tune}(t) = V_t \omega C_1 \tan\left(\frac{kt}{2}\right) - i_{tail} \qquad (10)$$

In the actual circuit design, the cascode stage in Fig. 5 is implemented twice in parallel and is operated as a Gilbert Cell. This effectively implements the crossbar switches A and B that provide the 180° phase shift as required for the system in
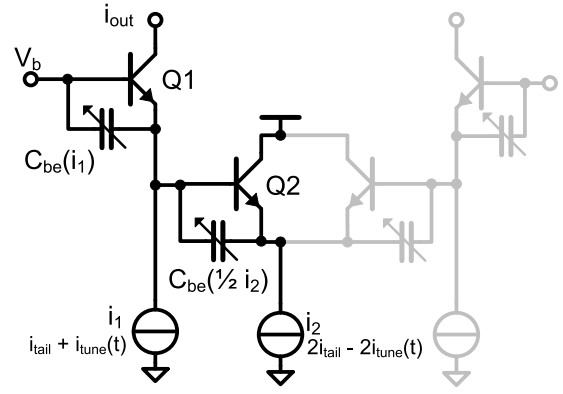

Fig. 6: Half of the left hand side part of the LPF in Fig. 5: the impedance seen at the emitter of Q_1 is composed of the $1/g_m$ of $Q1$ together with the reactance due to $C_{be,Q1}$, $C_{be,Q2}$ and $2C_0$ which is i_{tune}-independent if $i_1 + \frac{1}{2}i_2 = $ constant.

Fig. 2. Relatively slow switching is used to suppress switching spurs. The output switch in Fig. 2 is also implemented as a slow switching Gilbert Cell. Degenerated bipolar differential pairs are used to create the $\pm i_{tune}$ currents required for both the cascode circuitry and for the C_{be}-compensation circuitry from externally applied differential v_{tune} voltages.

IV. MEASUREMENTS

The measured $\phi(v_{tune})$ behavior of the two APFs in the inverting and non-inverting state at a signal frequency of 7 GHz is shown in shown in Fig. 7. For this measurement, the phase shift of the chip was measured using a vector network analyzer and the tune signals were provided by a 14-bit Digital Analog Converter (DAC) of which 8 bits are effectively used to drive the IC. Figure Fig. 7 shows that at 7 GHz the system can shift a full 360° which allows frequency translation. To create a fixed frequency translation, Δf, the $\phi(v_{tune})$ characteristic in Fig. 7 is inverted to get $v_{tune}(\phi) = v_{tune}(\Delta f \cdot t)$ which voltage was generated by the DAC. For an input signal at 7 GHz and a $\Delta f = 5.5kHz$ the resulting phase error across one sawtooth period is shown in the "before calibration" curve in Fig. 8. The phase error, $\Delta\phi$, is used to calibrate the phase shifter by adapting the v_{tune} as:

$$\Delta_{vtune} = \Delta\phi \left(\frac{\delta\phi}{\delta t}\right)^{-1} \left(\frac{\delta_{vtune}}{\delta t}\right) \qquad (11)$$

The resulting one-pass calibrated phase error is depicted by the "after calibration" curve in Fig. 8. The measured spectrum of the output signal for the calibrated phase shifter, shifting the 7 GHz input signal by 5.5 kHz, is shown in Fig. 9. A number of unwanted spurs is visible near the carrier; the strongest of these is the third harmonic spur at -30.8 dBc. Three effects are identified as most dominant in spurious creation: 1) phase-dependent gain of the APF causes amplitude modulation (AM); 2) switching causes phase jumps as shown in Fig. 7 and 3) a small second harmonic oscillation remains in the phase error after calibration. The first mechanism is due to an inexact gain ratio between the leftmost and the rightmost

differential pair in the APF; this gain ratio ideally is 2:1. In the current setup this mechanism results in the -30.8 dBc third harmonic spurs. The phase jumps are mainly due to insufficient isolation in the circuit and bond wire inductances which result in -68 dBc third harmonic spurs according to measurement and simulation. And finally the second order oscillation in the phase error produces -76 dBc third harmonic spurs.
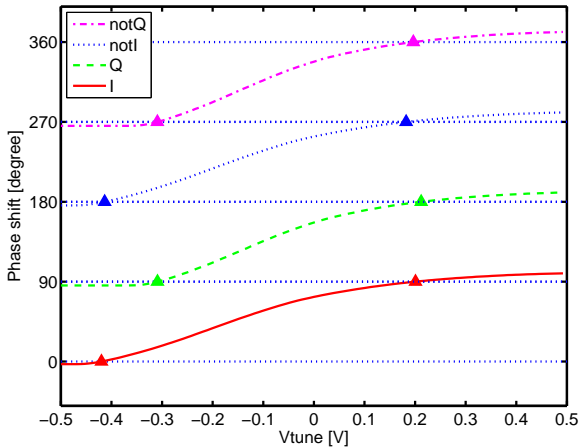

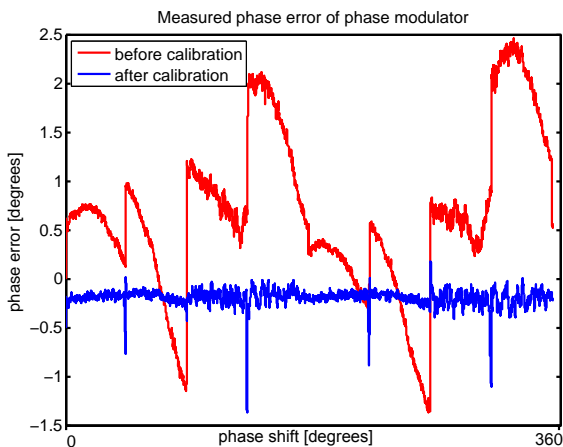Fig. 7: All four states of the 360° phase shifter characterized by a quasi DC sweep.

Fig. 8: The phase error before and after calibration of one sawtooth period stretching 360° averaged 30 times measured with a vector network analyzer.

V. Comparison with other work

As the authors are not aware of previous publications of these type of circuits for MIMO applications and a focus to translate a small frequency with low spurs, a comparison is made with phase modulators in Table I.

VI. Conclusions

A system that uses linear phase modulation to create a relatively small continuous frequency translation of an RF carriers was presented. The frequency shift can accurately be
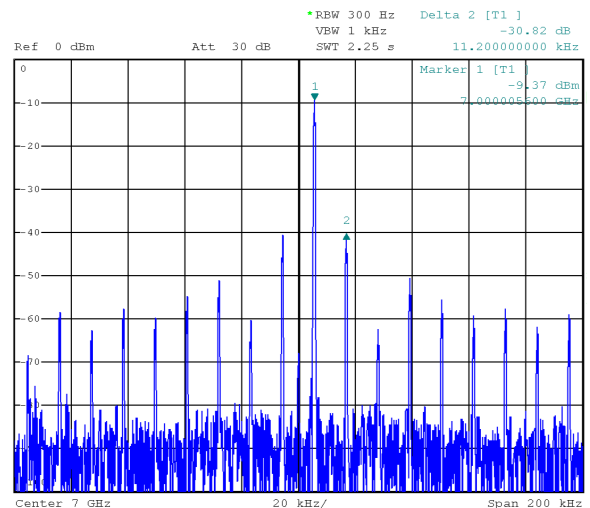

Fig. 9: Measured output spectrum for an input signal of 7 GHz, translated by 5.5 kHz.

TABLE I
COMPARION TABLE

	[5]	[6]	This work	
Technology	wavetubes	MMIC FET	SiGe	
Bandwidth	8.5-9.5	6-18	7-8	GHz
phase shifter bits	4	5	8	
highest spurious	-23.7	-22	-30.8	dBc

determined by either the control signal programmed in a DAC or by its sampling frequency. By changing the linear slope of the phase modulation into e.g. a quadratic one a linear chirp could be generated. The systems' operating frequency of the current design is lower limited by the polyphase filter and upper limited by the cutoff frequency of the APFs. The Spurious Free Dynamic Range (SFDR) is limited by amplitude modulation. Simulations, using phase measurement data as shown in Fig. 8, show that suppressing this AM could result in a 30 dB SFDR improvement.

VII. Acknowledgements

References

[1] E. Fishler, A. Haimovich, R. Blum, D. Chizhik, L. Cimini, and R. Valenzuela, "Mimo radar: an idea whose time has come," in *Radar Conference, 2004. Proceedings of the IEEE*, 2004, pp. 71–78.

[2] D. Rabideau, "Doppler-offset waveforms for mimo radar," in *Radar Conference (RADAR), 2011 IEEE*, May 2011, pp. 965–970.

[3] E. Rutz and J. Dye, "Frequency translation by phase modulation," in *WESCON/57 Conference Record*, vol. 1, 1957, pp. 201–207.

[4] K. Bult and H. Wallinga, "A cmos analog continuous-time delay line with adaptive delay-time control," *Solid-State Circuits, IEEE Journal of*, vol. 23, no. 3, pp. 759–766, June 1988.

[5] G. Klein and L. Dubrowsky, "The digilator, a new broadband microwave frequency translator," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 15, no. 3, pp. 172–179, Mar 1967.

[6] S. Mitchell, J. Wachsman, G. Lizama, F. Ali, and A. Adar, "A wideband serrodyne frequency translator," *Appl. Microwave*, pp. 325–330, 1990.