Functional layers for CIGS Solar Cell on-chip fabrication during post-processing

Jiwu Lu, Alexey Y. Kovalgin, Jurriaan Schmitz

Abstract - The ubiquitous deploying of wireless electronic devices due to pervasive computing results in the idea of Energy Scavenging, i.e., harvesting ambient energy from surroundings of the electronic devices [1]. As an approach to the most practical realization of such an energy scavenger, copper indium gallium selenium (CIGS) thin-film solar cells have attracted much attention due to the possibility to combine their reasonably high efficiency and low-temperature fabrication technology. The CIGS solar cells can be realized using CMOS compatible technology and are therefore suitable for CMOS post-processing and for their integration on a silicon chip as the energy scavenger.

In this work, we designed an integrable CIGS solar cell and developed a process flow entirely based on low temperature (<450 ^{o}C) post-processing technology[9]. Our CIGS solar cells are to be composed of a stack of the functional layers including plasma deposited silicon nitride barrier layer, DC-sputtered metal (Mo) back contact layer, RF-sputtered CIGS layer (intrinsically p-type) providing high light absorption, RF-sputtered n-type CdS buffer layer, and RF-sputtered tin-doped indium oxide (ITO) layer as a top transparent conductive layer to realize the second electric contact. The functional layers are characterized in terms of their physical properties.

Keywords: **CMOS post-processing, energy scavenging, low temperature CIGS Solar Cell deposition, micromachining**

I. Introduction

In the realization of pervasive computing [1], powering a huge number of the small electronic devices by wires or replacing the low capacity batteries routinely is an impossible mission. In the past decade, the advances in VLSI fabrication, such as the reduction of the transistor power consumption and the low duty cycles of the wireless electronic devices, reduced the power requirement to the sub-miliwatt range [2]. The low-power dissipation provides the opportunity for energy harvesting from the ambient environment, which surrounds the electronic devices. There are various energy sources for energy harvesting, and each source has certain advantages and disadvantages [3]. In spite of a number of limitations, solar cells are still the most practical and realistic energy scavenger in the near future due to their high power output ($100\times\eta$ mW/cm^2 under air mass 1.5 (AM1.5) spectrum, where η is the efficiency of the solar cells).

With the threat of the global warming, solar cells receive significant attention from both industry and academic research. Among all existing solar cell types, CIGS solar cells are chosen as the first choice of the energy scavenger because of their high efficiency [2], small required thickness of the functional layer stack (<5 μms) and possibility for fabrication under 425^{o}C. The latter is crucial for CMOS post-processing technology [9].

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II. 2. Fabrication of CIGS Solar Cells on a Chip

The starting material for the fabrication is silicon substrate with standard CMOS-fabricated test structures such as MOSFET transistors, diodes, and MOS capacitors.

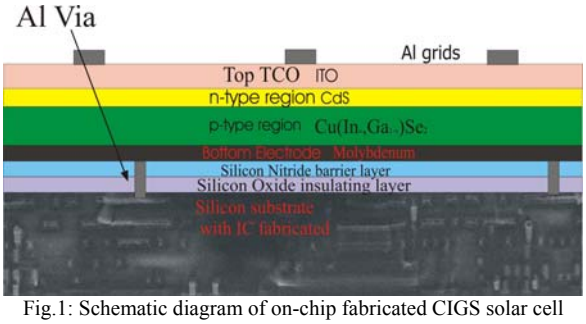

Fig.1: Schematic diagram of on-chip fabricated CIGS solar cell

Prior to the deposition of the functional layers, a silicon oxide layer and a silicon nitride layer are to be deposited by PECVD at 300^{o}C. These two layers act as the insulating and barrier layer, respectively [9].
A 600 nm thick molybdenum layer is further sputtered as the bottom contact. The CIGS

(intrinsically p-type) absorption layer is co-sputtered by the 3-stage process [10]. The n-type CdS buffer layer is sputtered in the same reactor without vacuum break. The top transparent conductive oxide (TCO, which is tin-doped indium oxide or ITO) is deposited by sputtering followed by post-deposition annealing at 300°C in N_2 ambient for 60 minutes. The latter is performed for electrical activation. The Al/Mo front contact grids are deposited in order to facilitate the current collection.

III. 3. Characterization of the Functional Layers

We used X-ray diffraction (XRD) method to determine the crystal structure and high resolution SEM (HRSEM) to obtain the surface morphology. Energy dispersive x-ray analysis (EDX) and X-ray photo spectroscopy (XPS) were employed to determine the chemical composition. A four-probe station was used to measure resistivity of the electrodes.

A. ITO characterization

The ITO layers, if used as transparent electrodes, are expected to have both high electrical conductivity and high optical transparency. Conventional layers (e.g. used for liquid crystal and flat panel displays, organic light-emitting diodes, etc.) are normally characterized by a high carrier concentration of 10^{20}–10^{21} cm^{-3} and a large band gap of 3.5– 4.3 eV.

A Philips XRD model Expert system II was used to measure the crystal structure of ITO. In Fig. 2, the green-line spectra belongs to the as-deposited ITO sample, whereas the red-line spectra shows a result of post-deposition annealing of the same sample at 300°C in N_2 for 60 min. One can see that, after the annealing, the peak corresponding to (222) crystal orientation increases.

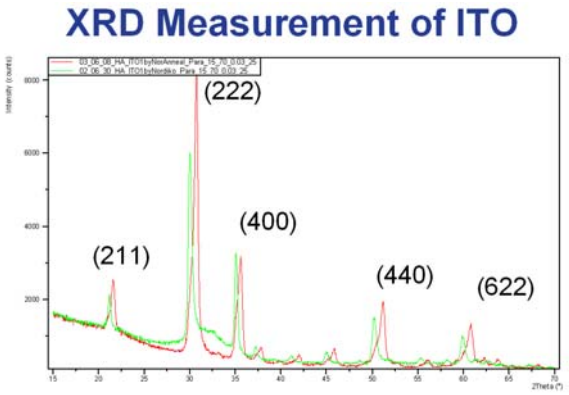

Fig.2: XRD Measurements of ITO

A four-probe station was used to measure the ITO sheet resistance; the layer thickness was measured by a Dektak surface profiler. For a commercially available ITO, the resistivity is normally in the range $(1 \sim 4) \times 10^{-4}$ ohm*cm [5]. The resistivity of our samples was measured to be 3×10^{-4} ohm*cm, which is comparable to that of the commercial samples.

Table 1: Resistivity of ITO

Resistivity of the ITO

	Sheet Resis (Ohm)	Thickness (nm)	Resistivity ($\times 10^{-4} \Omega \bullet cm$)
As-deposited	90.6	~100	9
Anneal at 300 °C for 1 hour in N_2	30.1	~100	3

The optical transmittance of ITO in the wavelength range between 300 nm and 2500 nm was measured. The yellow and blue curves correspond to the transmittances of as-deposited and annealed samples, respectively. The average transmittance in the visible region is clearly above 80% for the annealed sample.

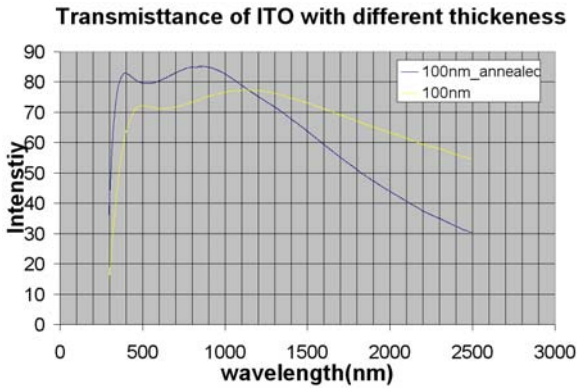

Fig.3 Transmittance of ITO

The XPS method was used to measure chemical composition of the ITO. In Fig.4, the blue, green and purple curves express the concentration of O, In, and Sn in atomic percents, respectively. The XPS data reveal that the chemical composition is not changing over the layer thickness. The Sn concentration is about 2.7 atomic %.

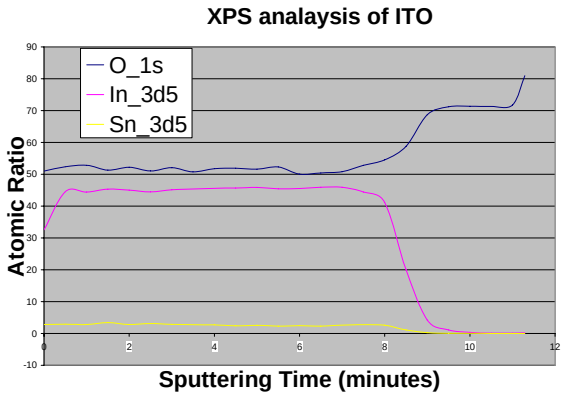

Fig.4. XPS analysis of ITO

B. Characterization of CdS

CdS is an n-type direct-bandgap semiconductor with $Eg \approx 2.4$eV and a typical resistivity in the range between 0.15 ohm·cm and 11.4 ohm·cm [11]-[12]. The resistivity of our samples was 0.615 ohm*cm, which is in the specified resistivity range.

A four-probe station was used to measure the sheet resistance of CdS. The thickness was measured by means of the Dektak surface profiler.

Table 2: Resistivity of CdS

Sheet Resistance	Thickness	Resistivity
57 k ohm	125 nm	0.615 ohm*cm

In Figure 5, the XRD measurement results indicate a polycrystalline and predominantly cubic structure of the CdS films, which is expected.

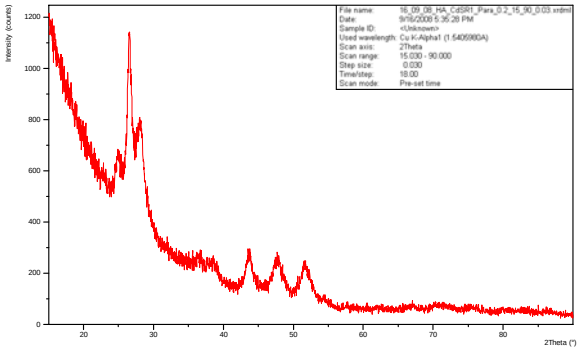

Fig.5. XRD spectrum of CdS

C. Characterization of CIGS

A CIGS alloy is a p-type material which has a strong absorption in the visible spectral range. In Fig. 6 one can see HRSEM images of the sputtered CIGS layers. One can notice a smaller grain size for the layers deposited on Pyrex substrate.

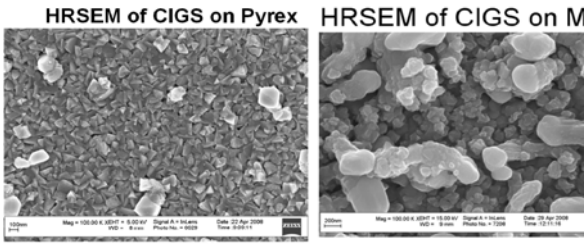

Fig. 6: HRSEM of CIGS on different substrates: Pyrex wafers (left) and Mo layer (right).

The XRD spectrum of CIGS on Mo (Fig. 7) clearly indicates the desired polycrystalline structure with a preferred (112) orientation.

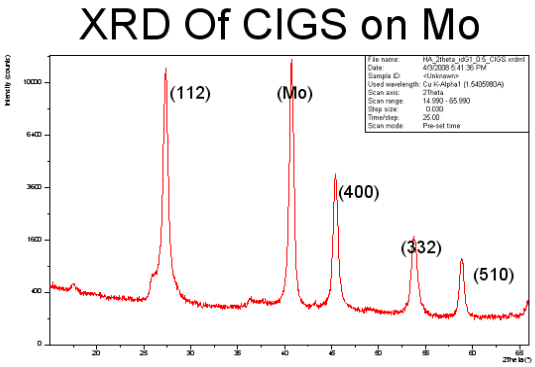

Fig.7. XRD spectrum of CIGS

To analyze the chemical composition, the EDX measurements were performed (see Fig.8. and Table 3). One can notice that the layer composition is quite deviating from the optimal composition needed to provide high-efficiency solar cells. Based of these results, increased indium and Se fractions combined with a decreased Cu fraction are still required.

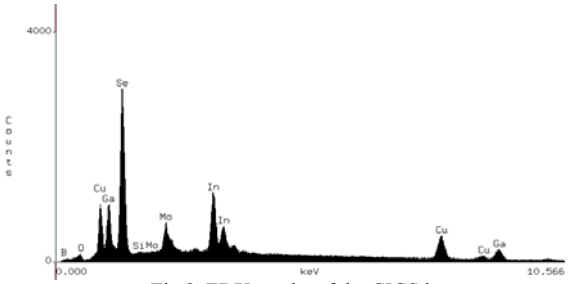

Fig.8. EDX results of the CIGS layer

Table 3. Atomic Ratios (i.e., concentration of certain atoms in atomic percents) in deposited CIGS layers

	Cu	In	Ga	Se
Atomic ratio	28.51	13	23	35
Optimal composition	25	17~20	5~8	50

IV. 5. Conclusions

In this paper, the CIGS solar-cell based energy scavenger has been proposed and designed. The function layers, needed to realize such a device, were deposited and characterized in terms of their physical properties. The ITO and CdS layers exhibited the required properties. However, the chemical composition and morphology of the CIGS absorption layers would require further improvements.

V. 6. Acknowledgements

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References

[1] Joseph A. Paradiso, Thad Starner, Energy Scavenging for Mobile and Wireless Electronics, (2005) *IEEE Pervasive Computing*, 4 (1), pp. 18-27.
[2] Contreras, M.A., Egaas, et.al. Progress toward 20% efficiency in Cu(In,Ga)Se polycrystalline thin-film solar cells, (1999) *Progress in Photovoltaics: Research and Applications*, 7 (4), pp. 311-316.
[3] Friedrich Kessler, Dominik Rudmann, Technological aspects of flexible CIGS solar cells and modules, (2004), *Solar Energy*, 77 (6), pp. 685-695.
[4] Friedrich Kessler, Konrad Herz, Flexible and monolithically integrated CIGS-modules, (2001) *Materials Research Society Symposium - Proceedings*, 668
[5] C. G. Granqvist, A. Hultåker, Transparent and conducting ITO films: new developments and applications, (2002) *Thin Solid Films*, 411 (1), pp. 1-5.
[6] R. Amirtharajah, A. P.Chandrakasan, Self-Powered Signal Processing Using Vibration-Based Power Generation, 1998, IEEE Journal of Solid-State CircuitsPage(s):687 - 695.
[7] Roundy, S., Energy Scavenging for Wireless Sensor Networks, 2003, Kluwer Academic Publishers, Boston MA.
[8] Martin A.Green, et.al., "Solar Cell Efficiency Tables (Version 31)", Prog. Photovolt: Res. Appl. 2008; 16: 61-67
[9] Jurriaan Schmitz, Adding functionality to microchips by wafer post-processing, 2007, Nuclear Instruments and Methods in Physics Research A 576, 142-149
[10] Gabor, A.M., Tuttle, J.R., Albin, D.S., Contreras, M.A., Noufi, R., Hermann, A.M., High-efficiency $CuIn_xGa_{1-x}Se_2$ solar cells made from $(In_x,Ga_{1-x})_2Se_3$ precursor films, 1994, *Applied Physics Letters* 65 (2), pp. 198-200
[11] A.L. Dawar, P.K. Shishodia, G. Chauhan and A. Kumar, Fabrication of low resistive CdS thin films, Thin Solid Films ***201*** (1991) (1), p. L1
[12] S. Ray, R. Benerjee and A.K. Barua, Properties of Vacuum-Evaporated CdS Thin Films, Jpn J Appl Phys ***19*** (1980), p. 1889