19.2 A Self-Interference-Cancelling Receiver for In-Band Full-Duplex Wireless with Low Distortion Under Cancellation of Strong TX Leakage

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In-band full-duplex (FD) wireless communication, i.e. *simultaneous* transmission and reception *at the same frequency, in the same channel*, promises up to 2x spectral efficiency, along with advantages in higher network layers [1]. The main challenge is dealing with strong in-band leakage from the transmitter to the receiver (i.e. self-interference (SI)), as TX powers are typically >100dB stronger than the weakest signal to be received, necessitating TX-RX isolation and SI cancellation. Performing this SI-cancellation solely in the digital domain, if at all possible, would require extremely clean (low-EVM) transmission and a huge dynamic range in the RX and ADC, which is currently not feasible [2]. Cancelling SI entirely in analog is not feasible either, since the SI contains delayed TX components reflected by the environment. Cancelling these requires impractically large amounts of tunable analog delay. Hence, FD-solutions proposed thus far combine SI-rejection at RF, analog BB, digital BB and cross-domain.

Figure 19.2.1 shows three current approaches to in-band FD: 1) use a well-isolating antenna solution, and cancel remaining SI in the digital domain; 2) cancel direct crosstalk as well as part of the reflected SI using an analog multi-tap filter at RF, combined with digital cancellation [3]; 3) exploit the digital BB and use a replica TX chain for cancellation at RF, combined with digital cancellation. Of these approaches, 2) yields the highest FD link performance reported so far, competing with 802.11 links [3]. However, all 3 approaches have their drawbacks: 1) requires very high isolation from the antenna, which generally results in a bulky, environment-sensitive or narrow-band solution; 2) requires nanosecond-scale analog delays in its multi-tap filter, which are incompatible with IC integration; 3) is limited in its ultimate cancellation performance by uncorrelated (phase) noise sources between the two TX chains.

This paper presents a zero-IF CMOS transceiver for small-form-factor FD systems, assuming a compact FD-antenna can only provide roughly 20dB worst-case isolation. Previously, the authors in [6] demonstrated an FD transceiver achieving -18dBm TX-power. In this work, we target +10dBm. Figure 19.2.1 shows the proposed architecture. To reduce the SI before amplification and ADC, a *second downconverter* is used to subtract a phase-shifted, amplitude-scaled TX replica in the analog BB. Adaptive phase-shift and amplitude-scaling are necessary to obtain robust cancellation of direct crosstalk for a varying antenna near-field. This is achieved by a vector modulator (VM) downmixer. A fixed attenuation is added externally to match the maximum range of the VM to the worst-case antenna-dependent isolation. This topology enables tapping the TX signal as close as possible to the antenna, thus including transmitter imperfections in the cancellation path.

To allow further cancellation of SI, including delayed SI-components, in digital and uncover the desired signal, the RX should have very high linearity under cancellation of strong SI, so as not to introduce distortion that raises the RX noise floor and masks the desired RX signals. In other words, a high self-interference-to-noise-and-distortion-ratio ("SINDR") is required. This puts very strict in-band linearity requirements on both downmixers, as they both have to process the maximum TX leakage. Furthermore, to prevent RX clipping under strong SI, cancellation has to take place before amplification. Hence, both the main RX and the VM are based on a highly linear passive mixer with series resistors [4].

Figure 19.2.2 shows the structure of the proposed RX + VM front-end. The VM can be considered a sliced version of the main mixer, which is essentially a switched resistor. Each slice is followed by static multiplexer switches that can rotate the 4-phase output currents through the four virtual ground nodes, resulting in VM functionality. This way, the 31-slice VM covers a square constellation of 32-by-32 phase/amplitude points, similar to [5]. This resolution allows for up to 28.5 dB of SI cancellation, in case the incoming SI is equal to the maximum range of the VM as set by the external attenuator (Fig. 19.2.1). Note that SI currents are absorbed by the VM before amplification (gray SI-current arrow in Fig. 19.2.2).

Figure 19.2.3 shows implementation details of a VM slice and the BB amplifiers. In contrast to [5], for better linearity no transconductors are used in the RF path up to the cancellation point, just resistors and switches. In the 65nm prototype, linearity is further increased by using low-ohmic mixer switches, in series with poly resistors to realize 50Ω input matching. The implementation is differential to lower even-order distortion. The BB amplifiers are two-stage opamps with a telescopic input stage and a push-pull output. Their linearity for desired signals and remaining SI is boosted by means of a tunable negative conductance at the inputs [4]. Although this work focusses on the RX, a low-power TX is co-integrated. Figure 19.2.7 shows the die micrograph of the CMOS transceiver.

Although measured gain, noise and linearity closely matched simulation results, two mistakenly-interchanged LO phases caused the RX to receive mirrored frequencies compared to the VM. This was corrected with a focussed ion beam repair to allow cancellation measurements.

The cancellation of the RX was tested using an 802.11g-style signal consisting of 52 tones with randomized phases in 16.25MHz BW centered at 2.5GHz. Measurements were first performed in a controlled case, with an external VM between TX and main RX, emulating the SI-channel. Figure 19.2.4 shows that the transceiver can suppress residual SI to 27dB below the power set by its fixed attenuator for a wide range of SI-channel phases and amplitudes. Next, cancellation was tested with the same signal under realistic conditions using two crossed WLAN dipole antennas as a simple FD antenna providing ~20dB worst-case (cross-polarization) isolation. Using these antennas, it was confirmed (not shown) that 27dB SI-cancellation can be achieved for a wide range of practical near-field scenarios.

Figure 19.2.5 shows the linearity performance of the RX at maximum gain, without SI-cancellation and under 28dB cancellation, versus SI-power. The derived SINDR plot shows that in a 16.25MHz BW, when the external attenuator is chosen for -18dBm maximum SI, the RX achieves its peak 69dB SINDR. When set for -10dBm, it achieves 60dB SINDR, whereas the RX without cancellation would clip under such SI. For this -10dBm case, with 20dB worst-case antenna isolation, FD links with +10dBm TX power and -70dBm distortion-limited noise floor should be achievable, sufficient for line-of-sight link ranges of ~100 meters at 2.5GHz.

Although most experiments were performed at 2.5GHz, the cancellation technique is essentially broadband: Figure 19.2.5 shows performance figures of the front-end over LO frequency.

Figure 19.2.6 compares the performance with the FD transceiver presented in [6], where TX-RX isolation is achieved by injecting the TX signal into the common-gate node of a noise-cancelling BB LNA. Note that the designs are not fully comparable, since [6] uses a single-port antenna (no isolation), with duplexing completely achieved in the BB. Assuming no antenna isolation, our design has increased peak SINDR, peaks at 20dB higher SI powers, and has >19dB higher RX compression under strong SI. Combined with some antenna isolation, this now enables FD links at practical TX powers in excess of 0dBm with sufficient DR for reception, compared to the compressed -17.3dBm of [6]. This comes at the expense of 3-to-5dB NF, but in FD the SI-induced distortion and residual SI will dominate RX sensitivity in practice. The chip has comparable power consumption.

Summarizing, an integrated RX for compact FD-nodes was proposed, featuring a highly linear passive VM for SI cancellation. Up to 69dB SINDR in 16.25MHz is demonstrated, enabling short-range FD communication.

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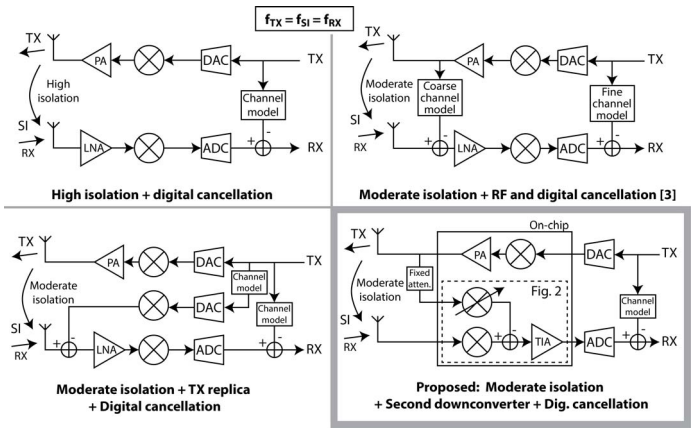

Figure 19.2.1: Full-duplex transceivers: 3 reported implementations and the proposed architecture. TX, SI and RX occur simultaneously at equal frequencies.

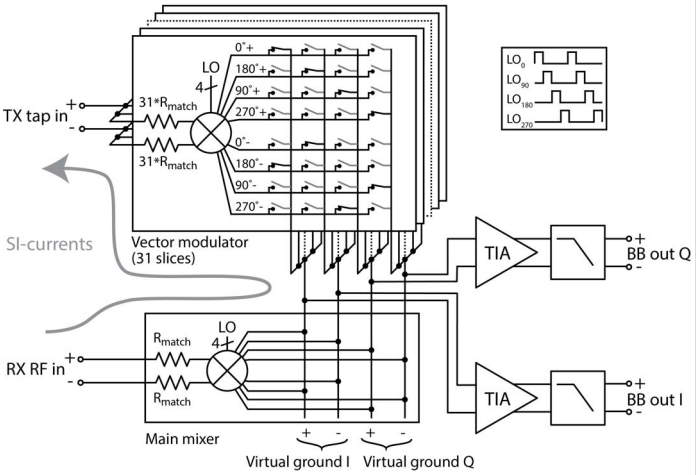

Figure 19.2.2: The proposed FD receiver: VM downmixer, main RX mixer and baseband amplifiers.

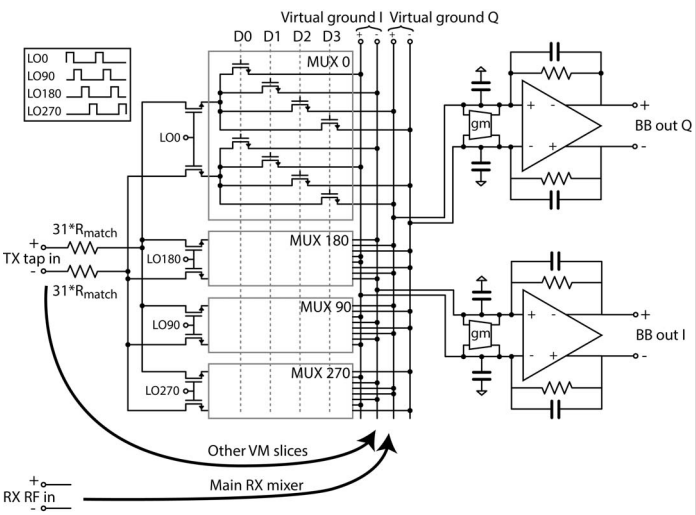

Figure 19.2.3: Implementation of one of the 31 VM slices and negative-conductance-compensated baseband TIA's.

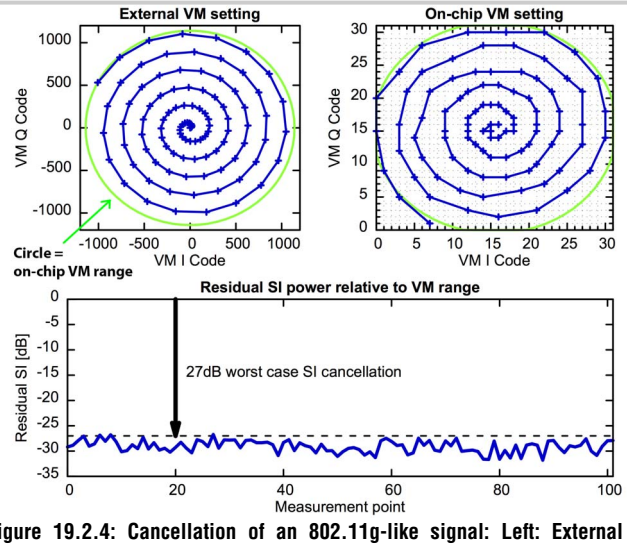

Figure 19.2.4: Cancellation of an 802.11g-like signal: Left: External VM emulates the SI-channel. Right: On-chip VM finds the points of best cancellation. Bottom: residual SI.

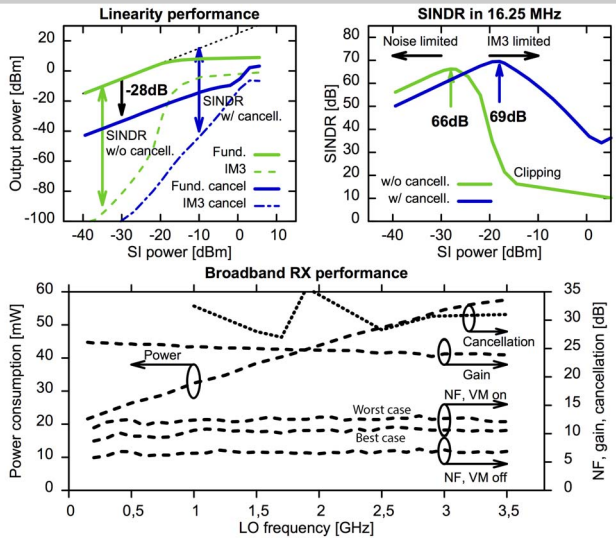

Figure 19.2.5: Top: Linearity and SINDR without and with cancellation of various SI powers. Bottom: Performance over LO frequency.

	[6]	This work
Topology	Noise-cancelling duplexer LNA's + complex feedforward network	Mixer-first receiver + SI-cancelling VM-downmixer
Technology	65 nm CMOS	65 nm CMOS
Supply	1.2V (LO) / 2.5V (BB)	1.2V
Operating freq.	0.1-1.5 GHz	0.15 – 3.5 GHz
Max. gain	51-55 dB	24 dB
NF	5-8 dB	10.3 – 12.3 dB (6.3 in half-duplex)
Power consumption	43-56 mW	23 – 56 mW (RX incl. LO tree)
Baseband BW	N/A	24 MHz (-12 MHz to +12 MHz)
In-band IIP3	-32.7 dBm	+8 / +16.2 dBm (Neg. conductance off / on)[1]
Effective in-band IIP3 with respect to SI	-7.2 dBm [2]	+19 dBm
SINDR in 16.25 MHz BW	57.0 dB peak @ -38 dBm SI [3] 21.6 dB @ -18 dBm SI	69.5 dB peak @ -18 dBm SI
Out-of-band IIP3	22.5 dBm	22.0 dBm
TX/RX isolation	33 dB	27 dB
TX power @ 1.3 dB RX compression	-17.3 dBm	> +1.5 dBm [4]
1/f Noise corner	N/A	2 MHz
Area	1.5 mm^2	2 mm^2

1) Neg. cond. gives a slight NF penalty [4] , 2) from -32.7 IIP3 and 60 dB better IM3 @33 dB isolation, 3) from 5 dB NF, 16.25 MHz BW, -7.2 dBm eff. IIP3, 4) 135 kHz spacing [6], under 28 dB cancellation.

Figure 19.2.6: Comparison to [6], assuming no antenna isolation for fair comparison.

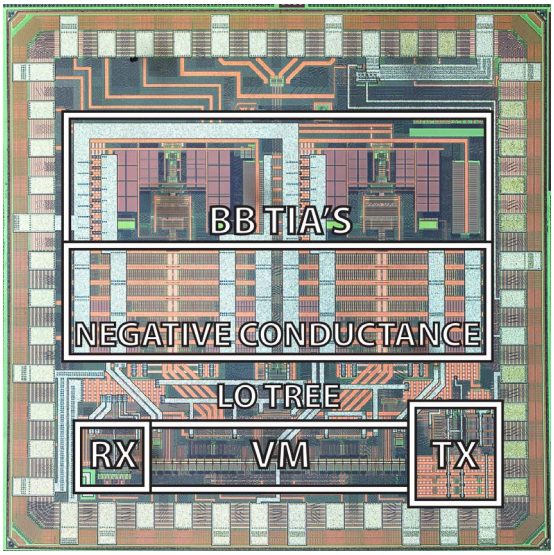

Figure 19.2.7: Micrograph of the 1.4×1.4mm prototype in 65nm CMOS.

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