Using the Oscillation Test Method to test for Delay Faults in Embedded Cores

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Abstract - **Continual advances in the manufacturing processes of integrated circuits provide designers the ability to create more complex and denser architectures and increased functionality on a single chip. The increased usage of embedded cores necessitates a core-based test strategy in which cores are also tested separately. The IEEE P1500 proposed standard for Embedded Core Test (SECT) is a standard under development which aim is to improve the testing of core-based system chips. This paper deals with the enhancement of the Test Wrapper and Wrapper Cells to provide a structure to be able to test embedded cores for delay faults. This approach allows delay fault testing of cores by using the digital oscillation test method and the help of the enhanced elements while staying compliant to the P1500 standard.**

Keywords - **P1500 SECT, Delay Fault Testing, Oscillation Test Method, Test Wrapper, Wrapper Cells**

I. INTRODUCTION

Design methodologies for VLSI system-on-a-chip (SOC) circuits based on reusable predesigned circuits, which are variously called intellectual property (IP) circuits or cores are becoming very popular. Verifying that such designs meet their performance objectives is difficult due to the hidden implementation details of the IP circuits. Delay fault testing of these cores is therefore difficult as access to these cores is not always available. The testing of cores is receiving a lot of interest nowadays due to the popularity of SOCs. The IC design community is divided into two groups: the core providers and the core users. The providers supply these cores as fault-free blocks to the user who is only concerned with the design, manufacturing and testing of his system. The cores are provided as soft, firm or hard-core, not manufactured and therefore not tested [1]. This leaves the testing of the core to the user after manufacturing the system. The user would therefore require assistance from the provider by delivering pre-defined tests with the core.

In this environment the IEEE P1500 SECT was developed. It intends to facilitate the testing of embedded cores as separate entities [2]. The IEEE P1500 does not cover the core's internal test methods or SOC test integration and optimisation. The IEEE P1500 is targeted at testing "black-box" third party cores. The implementation details of the cores are hidden from the core user and it is mandatory that the core providers deliver tests with these cores to ensure that testing of these cores can be carried out.

The paper is organized as follows. Section 2 gives a brief review on delay faults and the oscillation test method and section 3 covers the standard wrapper. In section 4 and 5 the proposed enhanced wrapper will be discussed. Section 6 will provide the conclusions.

II. DELAY FAULT TESTING

The increasing performance requirements of VLSI circuits make it difficult to design with large timing margins. Due to imprecise delay modelling, the statistical variations of the parameters during the manufacturing process as well as physical defects in the integrated circuits, the circuit performance can be degraded without altering its logic functionality. These faults are called delay faults. Most of the techniques used for detection of delay faults is time consuming and occupy a lot of silicon area. It also needs a two-vector test pattern to propagate the delay fault. One way to overcome this is to make use of the digital oscillation test method. In our experiment we will make use of the oscillation test method to detect delay faults within an embedded core with the help of our proposed enhanced IEEE P1500 compliant wrapper.

A. Oscillation Test Method

The oscillation test method for delays is concerned with sensitising a critical path and then test for delay faults. Critical paths are those paths that have the longest propagation delay from primary input to primary output. Therefore, the critical path is the most likely path for a delay fault to cause the circuit to malfunction. To sensitise a path, all off-path logic values inputs must be set to non-controlling values [4]. In the oscillation test method for digital circuits one considers the well-known digital ring oscillator in which an oscillation occurs when there is an odd number of inverting elements in the ring. The earlier mentioned sensitised path in the CUT is then incorporated into a ring oscillator to test for delay faults. The oscillation frequency is determined by the propagation delay through

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the sensitised path. Any delay-fault or stuck-at-fault that may alter or stop the oscillations can be detected by observing the oscillating frequency [5]. Therefore, a given delay increase in a critical path may result in a malfunction in the circuit but the same delay increase in another path may not effect the circuit functionality and performance. The oscillating frequency (fosc) is a function of the propagation delay in the critical path. Therefore, the loss or the deviation of the oscillating frequency from its nominal value can be employed to detect delay faults in the circuit.

III. STANDARD WRAPPER

The Standard P1500 wrapper acts as a shell around a core that allows that core to be tested as a stand-alone entity by shielding it off from its environment. The wrapper also allows the external circuitry to be tested independent from the state of the core. The wrapper must be able to function in three different modes. The first mode is the functional mode, in which the wrapper is transparent and operates as if not existing. Then, one has an inward-facing test mode, in which test access is provided to the core itself. Finally, there is an outward-facing test mode, in which test access is provided to the external circuitry outside the wrapper.

A. Wrapper Architecture

Within the P1500 standard there are optional and mandatory components [6]. Some of the mandatory elements are: a one-bit input/output port pair, WSI ('Wrapper Serial Input') and WSO ('Wrapper Serial Output'), and optionally one or more multi-bit input/output port pairs, named WPI ('Wrapper Parallel Input') and WPO ('Wrapper Parallel Output'). The complete wrapper is controlled via the Wrapper Interface Port (WIP) and an internal Wrapper Instruction Register (WIR). The WIP consists of six control signals. These control signals will be explained at the end of this section. The WIP controls the WIR. The WIP allows the WIR to be loaded with an instruction via the WSI. The operation of the remainder of the wrapper is controlled by both the WIP signals, as well as the instruction loaded into the WIR. Once an instruction is loaded into the WIR, the corresponding test mode becomes active. The P1500 wrapper also contains a Wrapper Bypass Register (WBY), which serves as a bypass for the serial test data mechanism through WSI and WSO.

The architecture of the standard P1500 wrapper will be shown in the next section together with the enhanced wrapper. The control signals are used as mentioned earlier to control the overall operation of the wrapper together with the instructions that are loaded into the WIR.

B. Wrapper Boundary Cells

The Wrapper Boundary Register (WBR) provides test access to the core. The WBR exists of Wrapper Boundary Input/Output Cells. There is a single cell for each functional digital core terminal. The cell must be able to provide the following features:

- Functional pass-through
- Controllability from the test data ports using the WSI and WPI.
- Observability to the test data ports using the WSO and WPO.

The implementations of a standard core input and core output wrapper boundary cells will be shown in the next section together with the enhanced wrapper cells. These simple cells provide all the functionality that is required from these wrapper boundary cells. Note that IEEE P1500 does only define the behaviour of such cells, and not the implementation. P1500 allows for extension of the functionality of the wrapper cells.

C. Wrapper Instructions

Instructions loaded into the WIR determine, together with the WIP signals, the mode of operation of the wrapper and possibly the core itself. There is a minimum set of instructions and corresponding operations that have to be provided. Optional instructions and their corresponding behaviour are also defined, together with the requirements for extension of the instruction set. All instructions that establish test modes that utilize the parallel ports WPI and WPO are optional, as the presence of these ports is optional. A minimal implementation of an IEEE P1500 compliant wrapper has no parallel test data ports. This wrapper provides limited test access bandwidth through WSI and WSO only.

IV. ENHANCED WRAPPER FOR DELAY FAULT TESTING

To be able to use the oscillation test method to test for delay faults in embedded IP cores with our proposed method, we require the IP core providers to supply delay data and partially specified test vectors for a set of representative paths in each IP core. For each path selected for testing in an IP core, we require the following information: (1) the input and output terminals of the path, (2) the delay value of the path, and (3) the test set for all inputs of the IP core to sensitise the selected path. The paths that will be tested for delay faults are a set of paths that are within a certain delay range and a set of longest paths through the core. Thus, an IP core specification should define IP core paths in a way that enables all such paths to be derived. The IEEE P1500 standard only defines the behaviour of cells and not the implementation. It therefore allows for extension of the functionality of the wrappers cells.

A. Enhanced Wrapper Input Cell

The enhanced input cell has the added functionality that makes it possible to select the cell for delay fault testing. Each input cell will be assigned a unique address. This address can be loaded into the added cell address register (CAR) in the cell by using the normal scan-in path and the DC control signal [7]. When the unique address is loaded into the CAR it must be updated in the address register. The *UpdateWR* signal with corresponding instruction in the WIR to enable the address register will be used to update the CAR. This loading and updating of the unique cell addresses can be executed while the wrapper is in normal mode. When the cell address that is necessary to be used for delay testing is scanned into all address registers

(AD) of the cells, the value will be compared to the unique address of the cell and only one cell will have a match and will therefore be selected. This match will produce a signal from the address register and together with the existing signal "*wci*" is used to select the multiplexer to allow the output signal from the selected output cell to be connected to the input of the core [7].

B. Enhanced Wrapper Output Cell

The same method as applied to the input cells has been used in the output cells regarding the use and loading of the unique cell address. The difference is that the signal produced from the address register if there is a match between the unique cell address and select cell address, is used to enable a tristate buffer to be able to link the output of core to the specified input of the core via the wrapper input cell [7].

C. Enhanced Wrapper

The enhancements to the wrapper are limited to the addition of two multiplexers, one demultiplexer and an XOR gate. The XOR gate, in figure 1 number 4, is employed to establish either an inverting or non-inverting feedback loop.

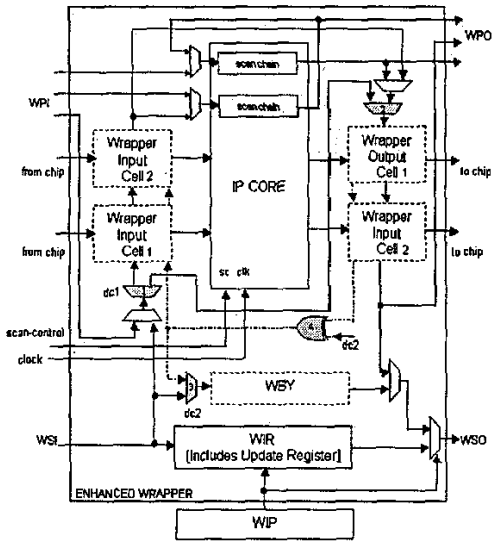

Figure 1. Enhanced Wrapper

To be able to have a different select address for the wrapper input and wrapper output cells we need a separate path for the wrapper output cells to be able to load a different select address than that as for the wrapper input cells. This can be accomplished by using a demultiplexer (1), multiplexer (2) and the use of control signal "*dc1*". The function of multiplexer (3) will be explained in another section. The modified wrapper architecture is shown in figure 1. The shaded elements are new to the wrapper and the elements depicted with a dotted line have been modified in figure 1. The testing for delay faults in the wrapped core can be done by sensitising the critical path that is required to be tested and selecting the appropriate wrapper input cell and the wrapper output cell. The test procedure together with the extra instructions that are needed will be explained in the following sections. It must be noted that it is assumed that the unique cell addresses are already loaded in the cells address registers. The wrapper is therefore in the normal mode and has no effect on the inputs and output to and from the chip to the core.

The delay testing process makes use of four control signals: *dc*, *dc0*, *dc1* and *dc2*. The specific use of the signals is as follows:

- *dc* - Allow loading of data into the CAR
- *dc0* - Select input signal for the WBY
- *dc1* - Load address data into the output cells
- *dc2* - Used to establish either an inverting or non-inverting feedback loop and enabling WBY for counting

A dedicated delay test IP core or control unit on the chip can generate these control signals. To control the CAR we define the following instructions to be written in the WIR Register:

- LOADIN_UNIQ: it loads the unique addresses from WSI into the CAR of all wrapper input cells
- LOADOUT_UNIQ: it loads the unique addresses from WSI into the CAR of all wrapper output cells

V. RESULTS WITH VHDL MODEL OF ENHANCHED WRAPPER

To be able to verify the operation of the wrapper it is necessary to manually apply the setup signals and observe the relevant signals of the wrapper. All wrapper elements were clocked by a single clock (*WCLK*) signal. All of the instructions were loaded serially. In the following sections the setup procedures and result of VHDL simulations on the operation of the enhanced wrapper will be shown.

A. Wrapper Cells Selection

The input cell is primary required for the transport of data from the chip to the core. The cells also provide access for the scan-in or scan through of data. As explained earlier, the enhanced cell also has the ability that a unique address can be stored in the CAR and then be compared with the selection address in the AD for delay fault testing. In figure 4, the timing and signal set- up for first loadings of unique address are shown.

The results show that the unique address only gets updated into the CAR from the AD once the *UpdateWR: CAR* signal becomes active. The two input cells now have two unique addresses. The same sequence is shown for the output cells and signal *dc1* is used to scan in data to the output cells so that the unique address can be loaded faster. Note that an instruction must first be loaded into the WIR and be updated in the WIR to allow the loading of the

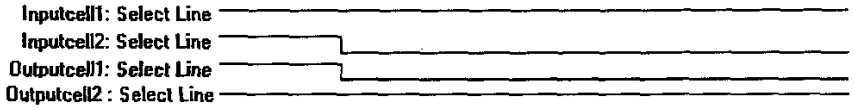

Figure 2. Input and Output Cell Select Lines

unique address for the input and output cells. As mentioned earlier, this all can be done while the wrapper is in normal mode. Once the unique addresses are loaded into the CAR of each cell, the cells are ready to be selected for the delay fault test. Only one input and one output cell must be selected. The output of the cell will be connected to the delay line (see figure 1) and the delay line to the input of the input cell. This then provides the feedback loop that is required for the oscillation test method. If an inverting feedback is needed then signal *dc2* will provide it via the added XOR gate in the delay line.

The first step in the delay fault-testing procedure is to load the selection addresses into the AD of the cells. There will be one address for the input cells and a different address that will be loaded into the output cells. It is critical that only one input and one output cell is selected for the test. When the selection addresses are loaded into the ADs of the cells, the address will be compared with the unique address of the cell once the *dc2* signal gets active.

This will result in only one input and one output cell select lines to be active. In figure 2, only input cell number 2 and output cell number 1 are selected and therefore their select lines are active. In our example we are using input cell number 2 as the start and output cell number 1 as the end of our selected critical path through the core. As can be seen in figure 3, once the cells are selected and they are linked from the output cell to the input cell we are able to perform the oscillation test to detect delay faults. The only element in the feedback path that adds to the delay time of the critical path is the XOR gate and the multiplexer on the input cell side (see figure 1) and the buffer on the output cell side.

The next stage in the delay-testing process is the evaluation of the oscillating frequency. This will be discussed in the next section. For testing purposes the core is represented by a simple combinational circuit.

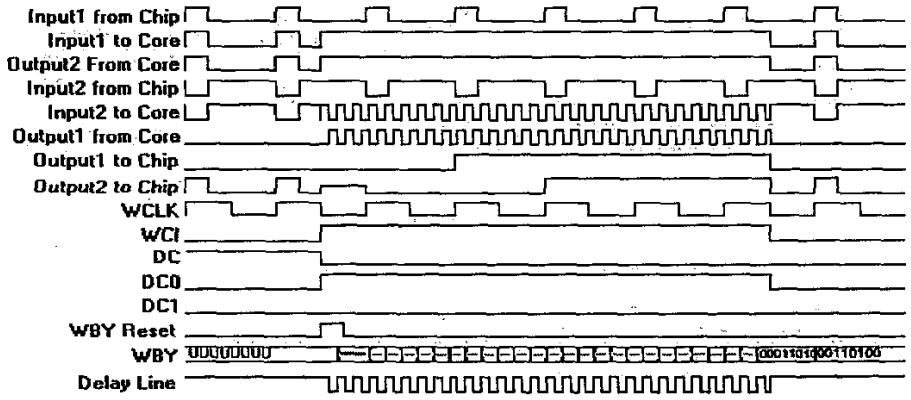

Figure 3. Delay Fault Testing Timing Diagram

B. Delay Fault Detection

The essential part of this testing method is the evaluation of the oscillation frequency. In the oscillation test method, the oscillating frequency must be observed to compare it with the oscillation frequency of a good device to be able to detect any extra delay in the selected critical path. Any extra delay will alter the oscillating frequency and can therefore be detected.

The WBY has been used for the evaluation of the oscillation frequency. This is favourable in order to reduce the amount of extra elements needed for this proposed testing technique. To be able to use the WBY for the measuring of the oscillation frequency it is necessary that the WBY must be able to count this frequency. It therefore requires a register and also a counter. As registers are constructed by using flip-flops, it will be possible for the WBY to be configured as a counter. The input to the bypass register will therefore be normally shifting data or the oscillation frequency will trigger it as a counter. Therefore if the WBY is enabled for a certain time period while being triggered by the oscillation frequency a certain counting word will be stored in the WBY after this time period. This

word will then be relative to the oscillation frequencies. Any extra delay in the selected critical path will alter the oscillating frequency and therefore also the value of the counted word in the WBY.

The simulation results are shown in figure 3. The results show how the WBY acts as a counter to measure the oscillating frequency. The selection of the input and output cells are similar to that previously explained. In figure 3, input cell number 2 and output cell number 1 are selected and the figure clearly shows that the oscillation occurs between these two cells and through the core. Before the oscillation test starts, the WBY is being reset. Signal *dc0* together with *dc2* enables the WBY for a certain time period and it counts the number of pulses from the oscillating frequency in that time frame. The value in the WBY can be serially shifted out and evaluated on chip or with a slow-speed tester. The WBY can then be used as a bypass register or oscillation counter depending on the instruction in the WIR together with the WIP signals for bypassing data through the wrapper. This proves therefore that delay faults, that are a combination of path and gate delays, can be detected with this technique.

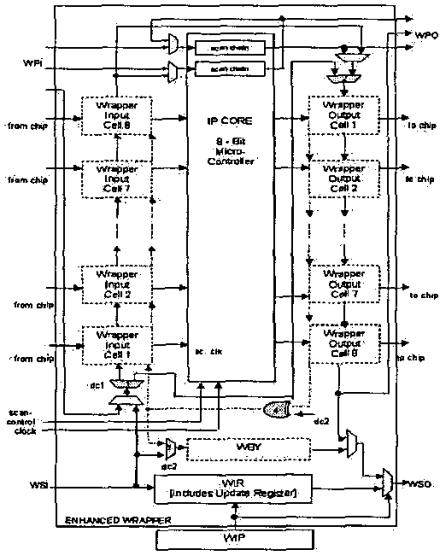

Figure 4. Enhanced Wrapper for IP Core

The proposed enhancements were simulated in ModelSim using an 8-bit microcontroller core. The enhanced wrapper for the 8-bit microcontroller core is shown in figure 4. The core was synthesized and the longest delay through the core was measured to be 7.17ns. This delay originates from input data line number 7 through to the address output-line number 15. This shows that for some instances it will be necessary to make use of wrapper output cells for internal signals that are part of the set of critical paths in the core. This was done in the same way that the wrapper output cells were designed for the primary outputs of the core. We added an extra delay of 400ps to the path through the core and the value of the count in the WBY has changed from 31 to 35. This indicates that the added delay fault of 400ps has been detected. One problem that had to be overcome was that the microprocessor output lines only get updated on the rising edge of the clock pulse. Therefore a test routine was developed to ensure that the output lines were updated constantly to ensure that the oscillation test method could be used. This test routine will be activated with the "*dc1*" control signal

C. *Implementing Test Technique on Sequential Logic*

In a sequential circuit, the system is free of timing failures if every combinational path between two memory elements propagates its signal in less time than the interval of the operating system clock. In other words, the input signal of every memory element in the system should have a stable signal before the arrival of the active clock edge.

A simplified example of a sequential circuit is shown in figure 5. To ensure that the system is fault-free, the clock period should be larger than the sum of the propagation delay of the input flip-flop FFi (t_{PDFFi}), the propagation delay of the combinational circuit (t_{PDCC}), and the setup time of the output flip-flop FFo (t_{SUFFo}) [5].

$$T_{CK} \geq (t_{PDFFi} + t_{PDCC} + t_{SUFFo}) \qquad \textbf{Equation 1}$$

The above relationship can be rewritten as follows.

$$t_{PDCC} \leq (T_{CK} - t_{PDFFi} - t_{SUFFo}) \qquad \textbf{Equation 2}$$

Therefore a given delay increase in a path may result in a malfunction in the circuit, but the same delay increase in another path may not affect the circuit functionality and performance.

Figure 5. Simple sequential circuit

Figure 6 shows a simple sequential circuit containing feedback. The output waveform for this specific circuit under specific input conditions is shown in figure 7. This simulation results indicates the sequential behaviour of the circuit. Figure 8 shows the oscillating output waveform when a critical path in the circuit is sensitized. Dedicated test inputs are used at the circuit's primary input to be able to sensitize the critical path. This verifies that the oscillation test method can be applied to sequential circuits with feedback.

It is clear from the results that the application of the oscillation test technique to a sequential circuit is viable. Automatic test pattern generators for test sequence

generation in sequential circuits are available and can be use to eliminate the time consuming process of finding correct test patterns for sensitizing the critical paths.

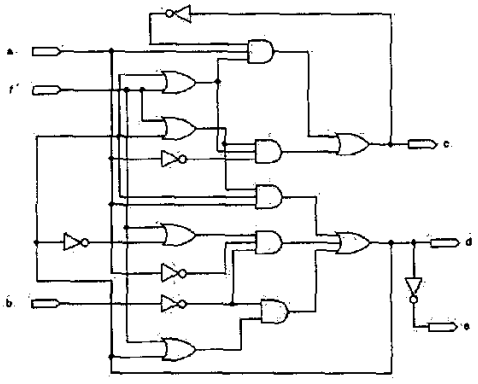

Figure 6. Sequential Circuit used for simulations

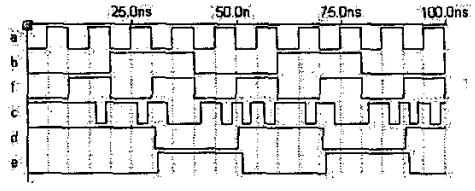

Figure 7. Output waveform of sequential circuit during normal operation

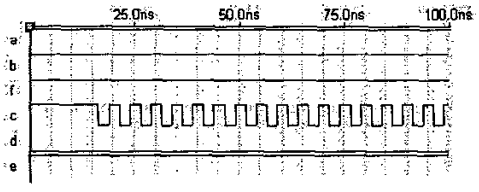

Figure 8. Output waveform of sequential circuit when using the oscillation test method

VI. CONCLUSIONS

The quest for the detection of delay faults is driven by the increased performance requirements of VLSI circuits. Our proposed architecture is primarily aimed at the detection of delay faults in embedded cores. Simulation results prove that the proposed enhanced wrapper will be able to test embedded cores for delay faults.

The enhancements were done to allow delay fault testing of embedded cores without needing much extra chip area. The input cells and output cells were enhanced to allow the cells to be individually selected which is a major advantage to the cells and wrapper. Another advantage is the use of the WBY for measuring the oscillation frequency. The proposed enhancements to the P1500 wrapper will make it possible that delay fault testing of various cores can be done in parallel thereby reducing the test time.

The complete enhanced wrapper that includes the input cells and output cells were verified by simulations to ensure correct operation within the P1500 guidelines. An extra delay was added in the critical path and the results show that our enhanced wrapper was able to detect this added delay fault. This proposed technique does not require many extra elements in the wrapper and it still remains P1500 compliant. The possibility to test the external circuitry and interfacing circuitry for delay faults with the use of this architecture will be investigated.

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