Electrically Active Interface Defects in the (100)Si/SiO_x/HfO_2/TiN System: Origin, Instabilities and Passivation

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An analysis of the origin and passivation of interface states in (100)Si/SiO_x/HfO_2/TiN capacitor structures is presented. For high-*k* gate/metal gate capacitors which exhibit relatively high interface state densities (> $1\text{x}10^{11}\text{cm}^{-2}$) the dominant interfacial defects are silicon dangling bond (P_{bo}) centres. For (100)Si/SiO_x/HfO_2/TiN capacitors which experience no high temperature thermal budget following HfO_2/TiN gate formation (T<600°C), the devices exhibit instabilities, where the interface state densities are modified during electrical measurements. The origin of this instability is studied. The response of the interface state density to rapid thermal annealing (30s) in N_2 over the temperature range 600-900°C is presented. In addition, results are presented for interface state passivation in forming gas ($0.5H_2/0.95N_2$) from 350-550°C for (100)Si/SiO_x/HfO_2/TiN gate stacks with no post deposition annealing following TiN gate formation and for devices following a 900°C, 30s N_2 RTA.

Introduction

The scaling of silicon based metal-oxide-semiconductor field effect transistors (MOSFET's) to minimum dimensions less than 45nm presents major technological challenges in terms of lithography and in terms of the basic materials which constitute the device. Since the first practical realization of a silicon MOSFET over 40 years ago the Si/SiO_2 system has remained at the heart of silicon based integrated circuit technology. The MOSFET device concept and the materials which constitute the device (Si, SiO_2) have remained essentially unchanged since the introduction of the polysilicon gate process. In current state-of-the-art microprocessors, which in 2006 represents minimum MOSFET feature sizes of 65nm, the gate oxide layers are based on a nitrided SiO_2 with a physical thickness around 1.2 nm. Further reductions of the gate oxide thickness are limited by gate oxide leakage currents densities and oxide reliability. From a fundamental perspective further scaling of the gate oxide is also limited simply by the number of Si and O atoms which constitute the thickness of the gate oxide layer.

These limitations have prompted a concerted research effort into finding materials of a higher dielectric constant (high-*k*) than nitrided SiO_2 to act as the gate layer in future processes. The use of high-*k* materials allows reduced leakage current densities for physically thicker films while maintaining the same capacitance per unit area of the gate oxide. A wide range of high-*k* materials have been suggested as candidates to replace nitrided SiO_2 including: HfO_2, ZrO_2, TiO_2, Ta_2O_5, Al_2O_3, La_2O_3 and Y_2O_3, silicated or

pseudobinary alloys like $(ZrO_2)_x(SiO_2)_{1-x}$ and $(HfO_2)_x(SiO_2)_{1-x}$, nitrided silicates HfSiO(N) ($HfO_2Si_xO_yN_z$) and epitaxial high-*k* such as $SrTiO_3$ (MBE) (1). A concentration of research effort into HfO_2 and nitrided $(HfO_2)_x(SiO_2)_{1-x}$, is evident over the last 5 years.

The use of high dielectric constant (high-*k*) thin films to replace nitrided SiO_2 in the gate stack of MOSFET's introduces many new technological issues, such as: mobility reduction in *n* channel MOSFET's (1,2), transient instability (3), fixed charges in the high-*k* layer (4), interface layer formation and control (5), control of the gate work function (6) and the understanding and passivation of electrically active interface states (7-12). This paper will provide an overview of recent work on the characterisation and passivation of interface states in the $(100)Si/SiO_x/HfO_2$ system. The results presented are primarily for high-*k* (HfO_2) metal-insulator-semiconductor (MIS) samples which exhibit relatively high interface state densities (> $1x10^{11}cm^{-2}$), where the interface states result in measurable distortion in the capacitance-voltage (CV) response of metal gate $(100)Si/SiO_x/HfO_2$ structures.

Following the experimental section, which provides details of the samples used in the work, the paper is divided into four main results sections. The first section considers the origin of the interface states responsible for the frequency dependent distortion commonly observed in the capacitance-voltage (CV) response of high-*k* MIS structures. The second results section presents measurements and analysis of instabilities in the CV and conductance-voltage (GV) response which occur for $(100)Si/SiO_x/HfO_2/TiN$ capacitors which experience no high temperature thermal budget following HfO_2/TiN gate formation (T<600°C). The third experimental results section covers the effect of rapid thermal annealing in N_2 (600-900°C) on the interface state density and device instabilities. Finally, the effect of forming gas annealing (350-550ºC) is presented for $(100)Si/SiO_x/HfO_2/TiN$ capacitors with no high temperature thermal budget following HfO_2/TiN gate formation (T<600°C), and for capacitors following a 900°C, 30s RTA in N_2.

Experimental

The starting substrates were *p* and *n* type Si(100) wafers with dopant concentrations of ~$3.5x10^{15}$ cm^{-3}. Following a 150s 2%HF sacrificial oxide removal and an IMEC clean, 4nm HfO_2 films were deposited by atomic layer deposition from $HfCl_4$ and H_2O at 300°C (80 cycles). The interface SiO_2 layer is approximately 1nm chemical oxide. The gate electrodes were 50 nm PVD TiN . The capacitors have no polysilicon capping layer over the TiN. Fully overlapped capacitor structures of 65μm × 65μm defined by local oxidation were used for the electrical measurements. It is emphasized that this work was limited to fully overlapped 65μm × 65μm capacitor structures. MOSFETs and gate-comb capacitors were not studied in this work.

Selected samples experienced rapid thermal annealing (RTA) in a Jipelec Jetfirst 150 RTP system for 30s at 600/700/800/900 ºC in a N_2 ambient with a graphite susceptor and passive cooling down. Prior to the maximum anneal temperature the wafers experienced a 300 ºC pre-anneal for 3 minutes to evaporate any volatile species. Forming gas annealing (FGA) was performed at 350/400/450/500/550 ºC for 30 minutes in a 5 % H_2 / 95 % N_2 ambient. The forming gas was flowing during the whole process, including the

cooling phase, and samples were unloaded from the furnace at 350°C. The cooling time for the 400, 450, 500 and 550°C was 50, 80, 102 and 123 minutes respectively. Cooling in forming gas or nitrogen did not result in any significant differences in the effect of the FGA annealing on the interface state densities (13). The interface state density [D_{it} (cm^{-2})] and the energy distribution of interface states across the energy gap, or at a specific energy level, [$D_{it}(E_g)$ ($cm^{-2}eV^{-1}$)] were determined from frequency dependent capacitance-voltage (CV) and conductance–voltage (GV) analysis. The CV and GV measurements were recorded using a HP4284A LCR meter following open calibration and bond pad correction. The measurements were performed on wafer in a microchamber probe station (Cascade Microtech, model Summit 12971B) with a humidity level < 0.5%. All measurements were recorded at room temperature. Unless otherwise stated the capacitors experience no FGA or RTA processes following HfO_2/TiN gate formation. Such low thermal budget capacitors are subsequently referred to as "no PDA".

Origin of Interface States in (100)Si/SiO_x/HfO_2/TiN Structures

Figure 1 shows example CV and GV responses over *n* and *p* type silicon for the 65μm x 65μm (100)Si/SiO_x/HfO_2/TiN capacitor structures (no PDA). The CV response exhibits a frequency dependent distortion in the region between accumulation and inversion for both the *n* and *p* type substrates. The frequency dependent distortion (subsequently referred to as a peak), increases with reducing the ac signal test frequency from 1 MHz to 100 Hz. Figure 1 shows only 400 KHz ad 10 KHz for clarity. The CV and GV data in Figure 1 have been corrected for parasitic capacitance and resistance using the model proposed by K. Kwa et. al. (14). The frequency dependence of the capacitance and conductance response are indicative of interface defects located as specific levels in the energy gap (13). Similar observations have been reported for a wide range of high-*k* MIS structures, including: ZrO_2, HfO_2, La_2O_3, Lu_2O_3, Dy_2O_3 and other high-*k* MOS structures (7, 15-19).

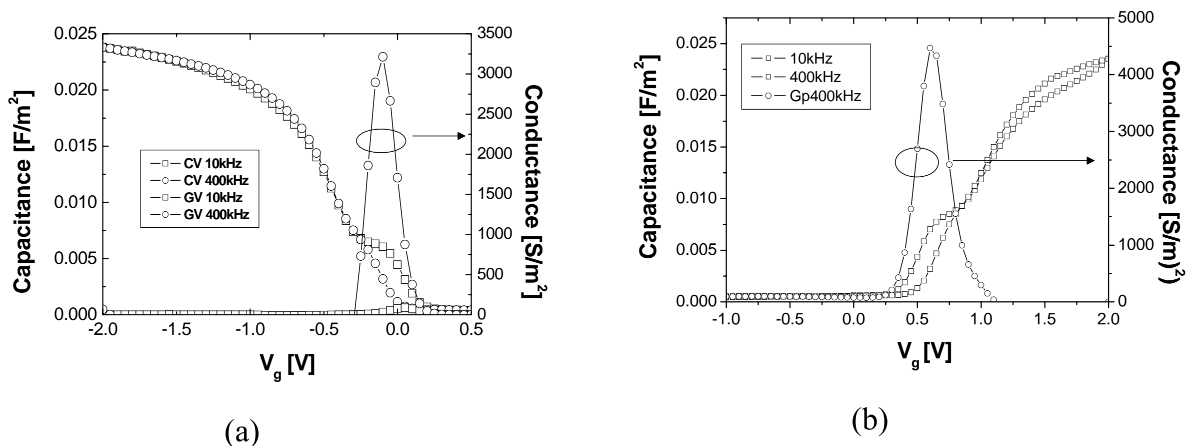


Figure 1. Corrected CV and GV characteristics at 10kHz and 400kHz for a (100)Si/SiO_2/HfO_2/TiN gate stacks over (a) *p* type silicon and (b) *n* type silicon. Equivalent oxide thicknesses (E_{ot}) in the range 1.4 to 1.6 nm.

This type of CV/GV behaviour is generally observed in high-*k* MIS capacitors which exhibit no high temperature post deposition annealing (T>600°C) and no forming gas annealing after gate oxide formation. High-*k* MIS capacitors where the final process step is an RTA in N_2 (700-900°C) can also exhibit similar CV/GV responses (12), where the RTA step results in hydrogen detachment from the interface states and cooling is sufficiently rapid to avoid passivation in the cooling process (20).

The interface state densities across the energy gap $D_{it}(E_g)$ were extracted from the corrected CV characteristics using the Berglund integral method. The energy gap regions of E_v to E_i and E_i to E_c were determined from the *p* and *n* substrate samples respectively. The full interface state distribution across the energy gap is then obtained based on concatenation of these results. The $D_{it}(E_g)$ plots for the Si(100)/SiO_2/HfO_2/TiN gate stacks prior to FGA or RTA are shown in Figure 2 (open squares), extracted at an ac signal frequency of 10 kHz[1]. The peak densities in the interface state density profile are directly related to the peak values in the capacitance voltage responses shown in Figures 1a and 1b. Figure 2 also shows (open circles) the interface state density obtained for the (100)Si/SiO_2 interface following hydrogen detachment by a 1050°C rapid thermal anneal (RTA) in N_2 (20). For the (100)Si/SiO_2 system RTA in N_2 is an alternative method to vacuum annealing or rapid pull from a furnace oxidation to achieve hydrogen detachment from P_{bo} and P_{b1} centers. The Figure also illustrates (dotted line) the energy distribution of the combined density of P_{bo} and P_{b1} centers as determined by Gerardi (21).

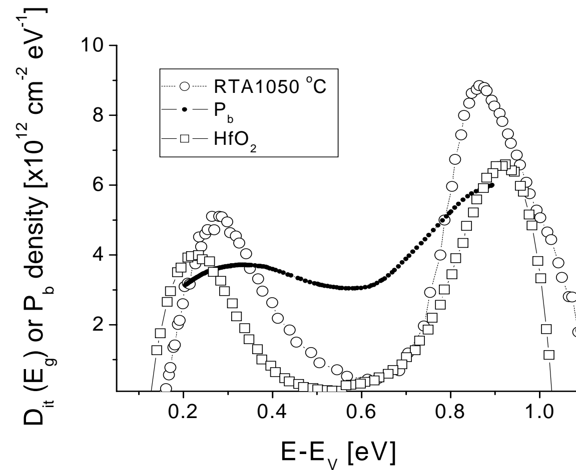


Figure 2. $D_{it}(E_g)$ profile for (100)Si/SiO_2/HfO_2/TiN gate stacks samples as in Figure 1 (open squares), the (100)Si/SiO_2 interface $D_{it}(E_g)$ profile following hydrogen detachment by a 1050°C RTA in N_2 (open circles) and the density of P_b defects determined in (21) (dotted line).

[1] These results are based on extractions from the CV responses at 10kHz. Extractions were selected for two reasons. Firstly, frequencies lower than 10kHz resulted in only marginal changes in the calculated peak $D_{it}(E_g)$ values. Secondly, extractions at lower ac signal frequencies (1kHz and 100Hz) were effected by leakage currents for the *n* type substrate samples especially for the higher temperature forming gas anneals 500°C and 550°C. For (100)Si/SiO_2/HfO_2/TiN gate stacks with no RTA or FGA the Berglund integral method overestimates the interface state density due to probing stress effects. This is discussed in the following section.

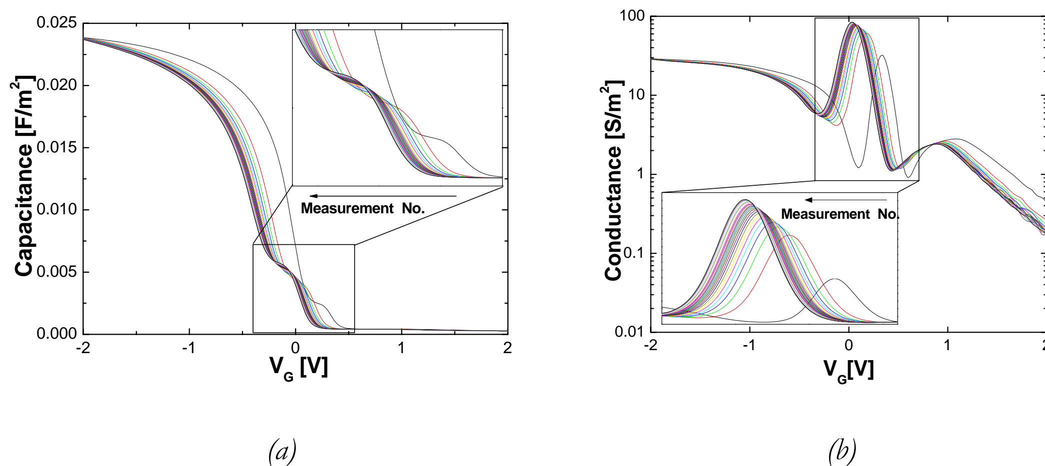
The similarity of the energy distribution for the (100)Si/SiO_x/HfO_2/TiN and (100)Si/SiO_2 structures suggests P_{bo} and P_{b1} centers as the dominant defects responsible for the high interface state densities often observed in (100)Si/SiO_x/HfO_2 structures. This interpretation is in agreement with analysis of the high-*k*/silicon interface from an electron spin resonance perspective for Al_2O_3, ZrO_2 and HfO_2 (8,9,22) and the work of Garros et. al., (12) based on modelling of the G(ω)V response of (100)Si/SiO_x/HfO_2/TiN/ polysilicon capacitor structures. Further support for this interpretation is based on a quantitative agreement between the density of P_{bo} defects and the density of electrically active interface states for (100)Si/SiO_x/HfO_2/Au structures (10). Finally, it is noted that this conclusion does not rule out the possibility that effects such as Hf-Si bonds at the silicon dielectric interface, isolated Hf atoms in the interface SiO_x layer or contaminants (C, Cl), contribute to lower levels ($< 1x10^{11}cm^{-2}$) of interface states.

Instabilities: Modification of Interface State Density during Measurements

Capacitor structures which experienced no RTA (T>600°C) or FGA following high-*k*/TiN formation were found to exhibit instabilities in the CV and GV response based on measurements performed over a bias range typical for the extraction of interface state density (± 2 volts). This is subsequently referred to as probing stress.

Measurements with Probing Stress

Figure 3 illustrates this effect, plotting 25 consecutive CV measurements on the same capacitor structure (no PDA). For the CV response (Figure 3a), a shift corresponding to an increase in positive oxide charge is observed as well as an increase of the peak in the CV characteristic associated with the interface defect response. The GV response (Figure 3b), which is recorded simultaneously with the CV, illustrates the same probing stress effect.



(a) *(b)*

Figure 3. The evolution of the (a) CV response and (b) GV response at 10 kHz for *p* type (100)Si/SiO_x/HfO_2/TiN structures for 25 consecutive CV measurements from inversion to accumulation with standard settings: (2.0 to -2.0V, 50 mV step, 2 averages, no light applied before/during measurement). The inset regions show a magnification of the CV and GV peaks versus measurement number on a linear Y scale.

An increase in positive charge is evident along with a corresponding increase in the peak conductance, indicating an increase in the interface state density with subsequent CV/GV measurements.

The conductance peak can be related to the interface state $D_{it}(E_g)$ through equation [1].

$$D_{it} = \left(\frac{\langle G_p \rangle}{\omega} \right)_{\max} [f_D(\sigma_s) q]^{-1} \qquad [1]$$

where $\left(\frac{\langle G_p \rangle}{\omega} \right)_{\max}$ is the peak value of the G_p/ω vs. $\log(\omega)$ curve, $f_D(\sigma_s)$ is a universal function of the standard deviation of the surface potential and q is the elementary charge (23). As the standard deviation of the surface potential is assumed to be zero for these samples, the formula is simplified further to equation [2].

$$D_{it} = \frac{2.5}{q} \left(\frac{\langle G_p \rangle}{\omega} \right)_{\max} \qquad [2]$$

From plots of G_p/ω versus log-f, the maximum values (unaffected by parasitic effects) were ~10 kHz. Consequently, the peak values in the 10 kHz conductance data (G_{top}) were taken to represent the peak interface state density.

Figure 4 illustrates the increase in the interface state density $\Delta D_{it}(E_g)$ [$cm^{-2}eV^{-1}$] and the fixed positive oxide charge ΔN_{ox} [cm^{-2}] as a function of the measurement number. Where $\Delta D_{it}(E_g)$ is calculated from equation [2] and ΔN_{ox} is calculated from the change in the voltage corresponding the $C_{acc}/2$ (where C_{acc} is the accumulation capacitance at –2 volts). The inset in Figure 4 shows the relationship of ΔN_{ox} and $\Delta D_{it}(E_g)$. The correlation factor R=0.99947 confirms that the two mechanisms are correlated. The result obtained support the model proposed by Houssa et al., (24) for the effect of stress on (100)Si/SiO_2/ZrO_2/TiN capacitor structures, were the voltage stress results in interface trap generation due to the hydrogen dissociation of $Si_3{\equiv}SiH$ centers resulting in $Si_3{\equiv}Si\bullet$ (P_{b0} centers) + H^+. As the traps are generated by electrical stressing, protons are trapped in the oxide giving rise to the correlated flat band voltage (V_{fb}) shift due to positive oxide charge. The results obtained indicate that the model is also applicable to (100)Si/SiO_{2x}/HfO_2/TiN capacitor structures. An exact 1:1 correlation of $\Delta D_{it}(E_g)$ to ΔN_{ox} is not straight forward as $\Delta D_{it}(E_g)$ obtained from the peak conductance *(G_{top})* is in units of [$cm^{-2}eV^{-1}$], whereas the fixed positive oxide charge ΔN_{ox} has units [cm^{-2}].

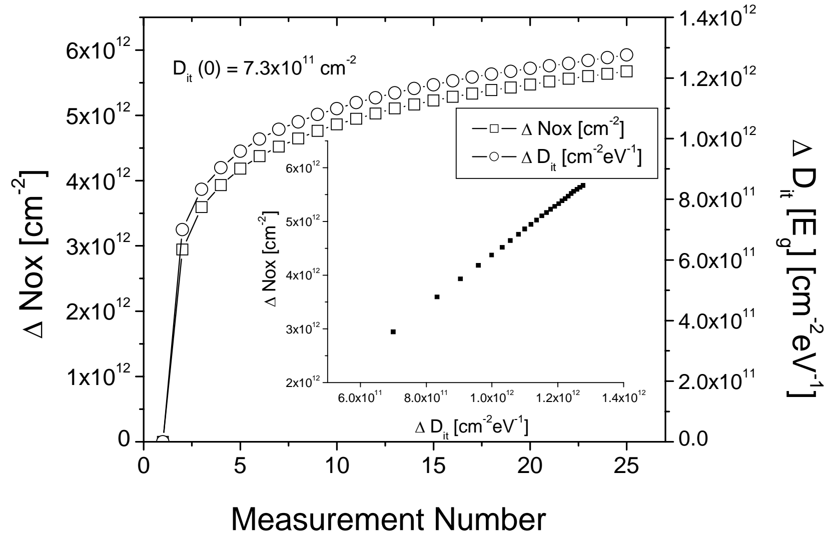


Figure 4. Increase in the interface state density $\Delta D_{it}(E_g)$ [$cm^{-2}eV^{-1}$] and the fixed positive oxide charge ΔN_{ox} [cm^{-2}] as a function of the measurement number. The fixed positive oxide charge is assumed to be located at the (100)Si/SiOx interface. Inset: correlation of $\Delta D_{it}(E_g)$ and $\Delta N_{ox.}$

Measurements Avoiding Probing Stress

From the results in Figure 4 it is evident that for (100)Si/SiO_{2x}/HfO_2/TiN with no RTA or FGA after gate stack formation, the measurement of the interface state density over a typical CV/GV bias range (±2 volts) modifies the interface state density. This raises the question of whether it is possible to measure the interface density in no PDA samples without changing the interface state density value. It is clear that the Berglund method cannot be used as the capacitors must be taken to strong accumulation to estimate the integration constant.

The results presented in Figure 5 illustrate CV and GV measurements taken over a large voltage range (±2 volts) and over a restricted bias range with the silicon/SiO_x/HfO_2 interface maintained in depletion (0…0.6 volts). Large voltage range CV/GV demonstrate an increase in negative (in inversion) and positive (accumulation) oxide charge for the first and second measurement respectively, while the conductance method, restricted to depletion, results in reproducible GV sweeps. Moreover, the peak value, G_{top}, was found to be stable for at least one hour during the application of the corresponding bias voltage. GV measurements in depletion are used in the subsequent sections to determine the interface state density without probing stress. The results in Figure 5 also indicate that there is an electric field or current threshold to interface state generation in the (100)Si/SiO_{2x}/HfO_2/TiN capacitor structures.

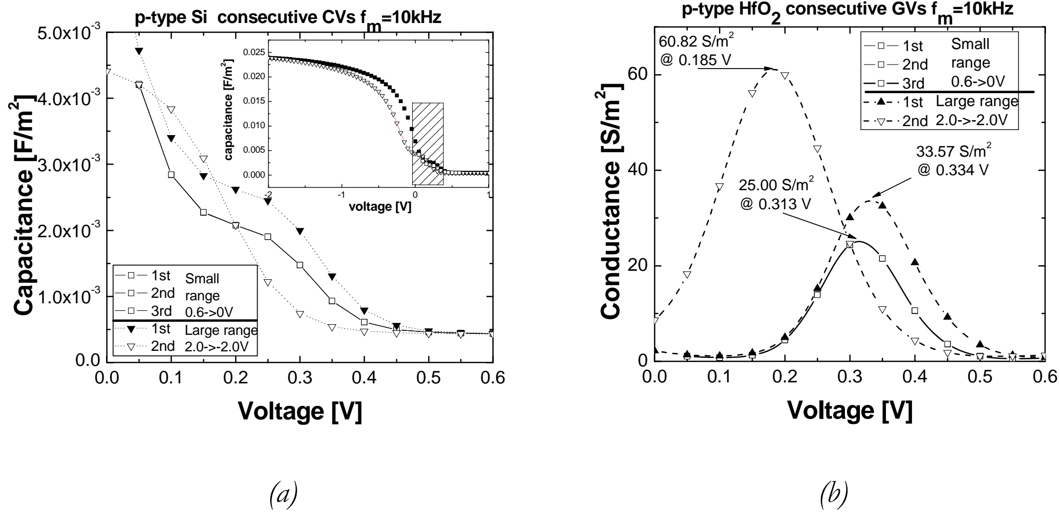


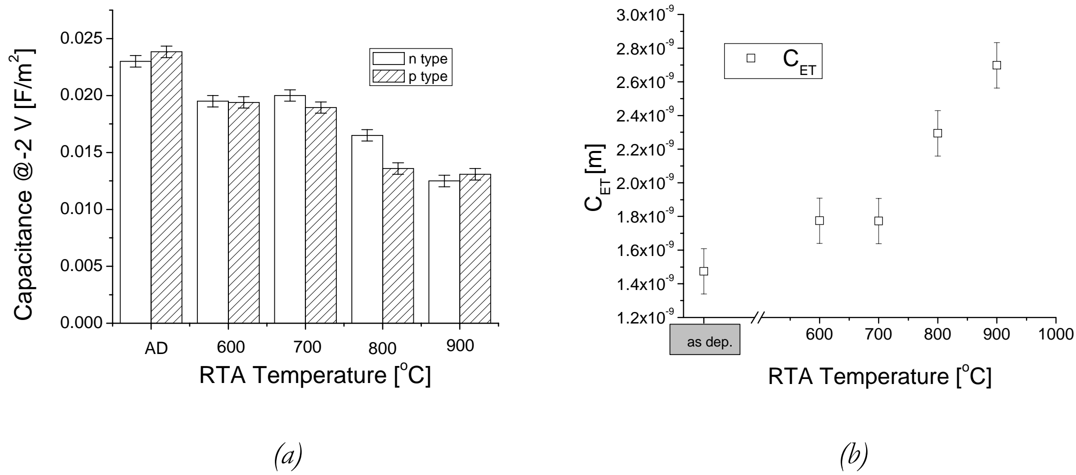
Figure 5. Consecutive CV (a) and GV (b) characteristics for a two previously un-probed test structures. Dotted lines represent scans from inversion to accumulation ('large range': 2.0 → -2.0V), solid lines represent three consecutive scans over a small voltage range within the range of surface depletion (0.6V → 0.0V). Inset (a): represents the full CV range and the small range (hashed region). For large range CVs, a shift associated with positive oxide charge and increase of the interface state density are observed. For large range GVs, a peak shift and an increase in both peak width and height are observed. Small range CV and GV responses are reproducible with no associated CV/GV shift or increase in interface state density.

Influence of Rapid Thermal Annealing in N_2 on Interface States in (100)Si/SiO_x/HfO_2/TiN Structures

Figures 6 and 7 show the effect of RTA (30s in N_2 at 600/700/800/900 ºC) on the accumulation capacitance and the interface state density response and the interface for *n* and *p*-type samples. The (100)Si/SiO_{2x}/HfO_2/TiN structures exhibit a significant degradation in the accumulation capacitance for RTA temperatures ≥ 800°C. The observations are in agreement with previous studies which demonstrated that the capacitance decrease was associated with the growth of an interfacial layer with a dielectric constant between 8 and 9, suggesting the interfacial layer following RTA contains hafnium silicate (25).

From Figure 7 for both *n*/*p*-type samples, the $\Delta D_{it}(E_g)$ is increased at 600ºC, but subsequently reduces to ~ $2.5\text{x}10^{11}$ cm^{-2} eV^{-1} for RTA temperatures of 800 and 900°C[2]. The increase in the interface state density following the RTA at 600°C can be explained by hydrogen detachment from interface defects during the RTA process. This has been demonstrated to occur for the Si/SiO_2 system (20,26). For the case of the thermally oxidized (100) Si/SiO_2 system interface state density continues to increase with increasing RTA temperature due to P_b-H detachment and additional P_{bo} creation.

[2] It is also evident from the figure that the RTA results in a decrease in the sensitivity to probing stress.



(a) *(b)*

Figure 6. Evolution of the (a) accumulation capacitance (C_{acc}) at ±2 volts and (b) the corresponding capacitance equivalent thickness (C_{ET}) @-2 volts for 30s RTA's in N_2 (600-900°C) for the (100)Si/SiO_{2x}/HfO_2/TiN capacitor structures over *n* and *p* type silicon.

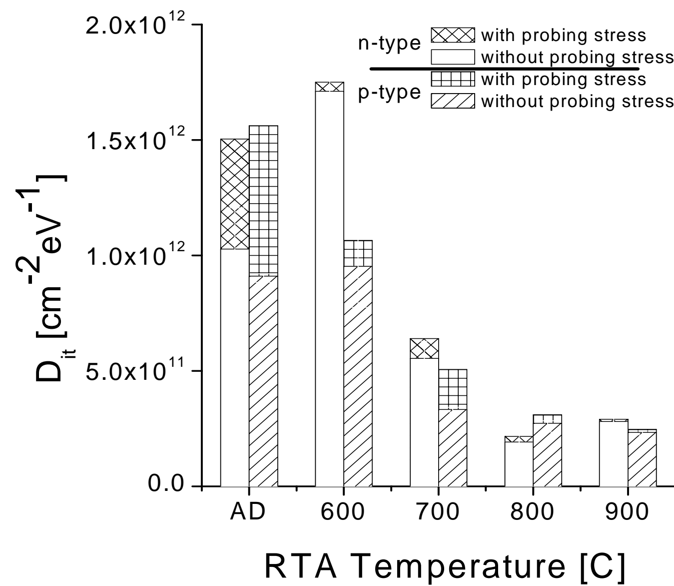


Figure 7. Peak interface state density evaluated from the conductance method in the lower energy gap region (*p* type) and upper energy gap region (*n* type) as a function of the RTA temperature for (100)Si/SiO_{2x}/HfO_2/TiN capacitor structures over *n* and *p* type silicon. The interface state density values are plotted with and without the effect of probing stress.[3]

[3] With probing stress is determined by the ratio of G_{top} of two consecutive 10k CVs measured in [-2.0…2.0] V. Without probing stress is a single CV/GV in depletion (typically 0…0.6 V)

This is not observed for the (100)$Si/SiO_{2x}/HfO_2/TiN$ capacitor structures and it is suggested here that this relates to the availability of hydrogen or hydrogen related species (H, H_2, H_2O, OH, …) present in the HfO_2 layer due to the deposition process. The available hydrogen species provide a source of hydrogen for passivation of the interface defects during the cooling phase of the RTA. The limited availability of such species in thermally grown Si/SiO_2 structures results in un-passivated P_{bo}/P_{b1} centers at the end of the RTA process. The reduction of the interface state density for RTA temperatures ≥700°C is consistent with the re-growth on the interface layer and the availability of hydrogen species provide for passivation of the interface defects during the cooling phase of the RTA.

Influence of Forming Gas Annealing on Interface States in (100)$Si/SiO_x/HfO_2/TiN$ Structures

The interface state density of *p*-type samples without PDA exposed to a 30 min FGA at 350/400/450/500/550 ºC are shown in Figure 8. The results indicate that the influence of probing stress is reduced for FGA temperatures ≥ 450°C. The minimum interface state density, when probing stress is avoided is 350°C. The impact of probing stress results in an apparent minimum at 450°C.

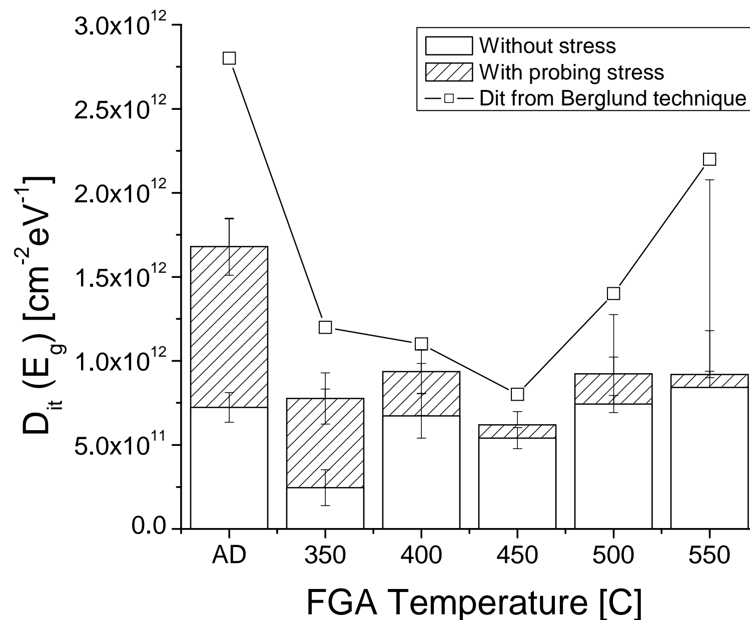


Figure 8. Peak interface state density evaluated from the conductance method in the lower energy gap region (*p* type) as a function of the FGA temperature for (100)$Si/SiO_{2x}/HfO_2/TiN$ capacitor structures. The interface state density values are plotted with (hashed) and without (clear) the effect of probing stress. The interface state density evaluated using the Berglund method from (13) is also plotted (open squares). Probing stress applied to these samples is equal to the probing stress experienced during the large range CV measurements used for the Berglund extraction.

The results obtained on the same samples using the Berglund method, which yield an increased interface state density due to probing stress, are also shown in the Figure. These results, which were published previously in (13), also indicate a minimum interface state density around 450°C. Isothermal anneals at 400°C (not shown here) indicate that D_{it} [cm^{-2}] values saturate after 30 minutes. The FGA (not shown here) also results in a dramatic reduction in the voltage shift of $C_{acc}/2$ between two consecutive large range 10k CV measurements, with a monotonic decrease from 180 mV for the as-deposited sample to 16 mV for the 550°C FGA.

The interface state densities of *p*-type samples, exposed to a 900°C RTA in N_2, followed by a 30 min FGA from 350 to 550 ºC, are shown in Figure 9. The effect of probing stress has now been minimized, with a clear minimum interface state density at 450°C. An optimum around 450°C does appear reasonable as following the 900°C RTA process interface re-growth occurs and the optimum passivation temperature for high temperature thermally grown Si/SiO_2 is in the range 400-450°C (27). It is interesting to note that the optimum FGA conditions ~450°C reported here for capacitors with a 900°C RTA does not correspond to polysilicon gate $(100)Si/SiO_x/HfO_2$ stacks (11), or to $(100)Si/SiO_2/HfO_2$/TiN/polysilicon gate stacks (12), where optimum values in the range 520-530°C are reported. The samples reported in (11,12) had polysilicon gates, otherwise there are no significant differences in the processing. It was noted in (12) that for full MOSFETs 425°C was sufficient for interface state passivation.

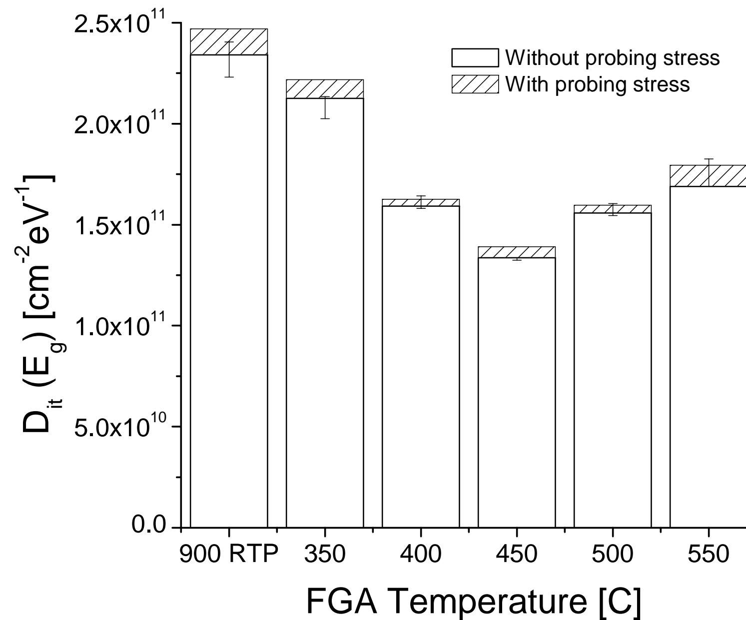


Figure 9. Peak interface state density evaluated from the conductance method in the lower energy gap region (*p* type) as a function of the FGA temperature for $(100)Si/SiO_{2x}/HfO_2$/TiN capacitor structures, following the 900°C RTA. The interface state density values are plotted with (hashed) and without (clear) the effect of probing stress. With probing stress is determined by the ratio of G_{top} of two consecutive 10k CVs measured in [-2.0…2.0] V.

Conclusions

Electrically active interface defects have been examined for (100)$Si/SiO_x/HfO_2/TiN$ (65μm × 65μm) capacitor structures. Analysis of the interface state density over the energy gap extracted from the CV and GV characteristics, for samples with relatively high interface state densities (> $1x10^{11}cm^{-2}$), exhibit the electrical signature of the P_{bo} centre for the (100)Si/SiO_2 interface. These conclusions agree with ESR (8,9) analysis and with other studies based on CV and GV analysis of (100)$Si/SiO_x/HfO_2$ structures (7,12,17).

For (100)$Si/SiO_x/HfO_2/TiN$ capacitor structures which experienced no forming gas annealing or high temperature (T≥600°C) N_2 annealing following HfO_2/TiN gate formation, the CV and GV responses exhibit probing stress instabilities, where the interface state densities are modified by CV/GV measurements over typical bias (±2 V) ranges. The interface state density and fixed positive oxide increase during subsequent CV/GV measurements are correlated, supporting the model proposed by Houssa (24). The use of GV measurements restricted to the condition of surface depletion allow the interface state density measurements without probing stress. Probing stress instabilities are minimized by a FGA T ≥ 450°C or by a RTA in N_2 at T ≥ 700°C.

The optimum forming gas anneal temperature for (100)$Si/SiO_x/HfO_2/TiN$ capacitor structures following a 900°C RTA in N_2, where probing stress effects are minimal, is 450°C. For (100)$Si/SiO_x/HfO_2/TiN$ capacitor structures with no RTA following the HfO_2/TiN gate formation, the minimum interface state density, avoiding probing stress, is obtained at an FGA temperature of 350°C. The optimum anneal temperature obtained following the 900°C RTA in N_2 is lower than reported in other works (11,12) and this is an area which requires further study.

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