Integrated X-Band FMCW Front-End in SiGe BiCMOS

Erwin Suijker[#1], Lex de Boer[#], Guido Visser[#], Raymond van Dijk[#], Michael Poschmann*[2], Frank van Vliet[#]

[#]*Observation Systems, TNO Defence, Security and Safety*
The Hague, The Netherlands
[1]erwin.suijker@tno.nl

[*]*Infineon Technologies AG.*
Neubiberg, Germany
[2]michael.poschmann@infineon.com

***Abstract*— An integrated X-band FMCW front-end is reported. The front-end unites the core functionality of an FMCW transmitter and receiver in a 0.25 µm SiGe BiCMOS process. The chip integrates a PLL for the carrier generation, and single-side band and image-reject mixers for up- and down-conversion of the waveform. The front-end has been designed to co-operate with COTS integrated direct digital synthesisers and ADCs.**
The measurements show an output power of 0 dBm, P_{1dB} at the receiver input of -11 dBm and a side band suppression of the mixer in the transmit chain of >40 dBc. The MMIC measures 1.8x1.5 mm^2. This integrated front-end paves the path for future planar 2D integration of FMCW phased-array radars at X-band.

I. Introduction

X-band FMCW front-ends are generally made in a hybrid way with COTS components. However for 2D phased-array integration these components are too big, unless severe degradation of the specifications are accepted. The core functionality, thus including all X-band components, of an FMCW front-end has been integrated in BiCMOS and is presented in this paper. The chip with a size of 1.8x1.5 mm^2 (Fig. 2) can easily be packaged in a 5x5 mm^2 QFN package.

Besides the obvious size advantage for the integrated circuit, it can also be a cost advantage depending on the volume and simplifies board design as the only high-frequency connection is the transmission line to the antenna.

The MMIC has an on-board local oscillator (LO) source that is locked to an external reference around 65 MHz. With a switch in the LO path, the option of supplying an external LO is left to the user. The frequency of operation of the MMIC is from 8.5 to 11 GHz, with a limited range when used with the internal LO, as a tuning range of more than 20% was not deemed feasible.

The single-side band (SSB) mixer in the transmit chain requires IQ, differential signals for the waveform. This low-frequency signal is mixed with the LO to generate the transmitted waveform. A linear frequency sweep or up/down sweep is often used but any other signal can be used for advanced waveforms. The system has been designed with a single chip direct digital synthesiser (DDS) in mind. Alternatively, the IF inputs can be connected to DC voltages in such a way that the up-converter acts as a buffer amplifier and a swept LO can be used directly through the external LO input or via the PLL.

II. FMCW Front-End Components

A common architecture for an FMCW front-end is a high-frequency swept signal source, whose output signal is amplified and transmitted. The output signal (through a coupler) is also used in the receiver as the local oscillator for down conversion to base band. For increased flexibility we use an oscillator that is mixed with a baseband signal that contains the frequency sweep. This enables us to use different modulation forms, offsets per channel, MIMO configurations etc. Direct digital synthesiser components are envisaged for the frequency sweep at baseband. At TNO there is ample experience in using the Analog Devices AD9xxx series DDSes for hybrid FMCW front-ends. The integrated front-end works best with the double core DDS circuits that can generate IQ signals. In this case offsets down to DC can be used.

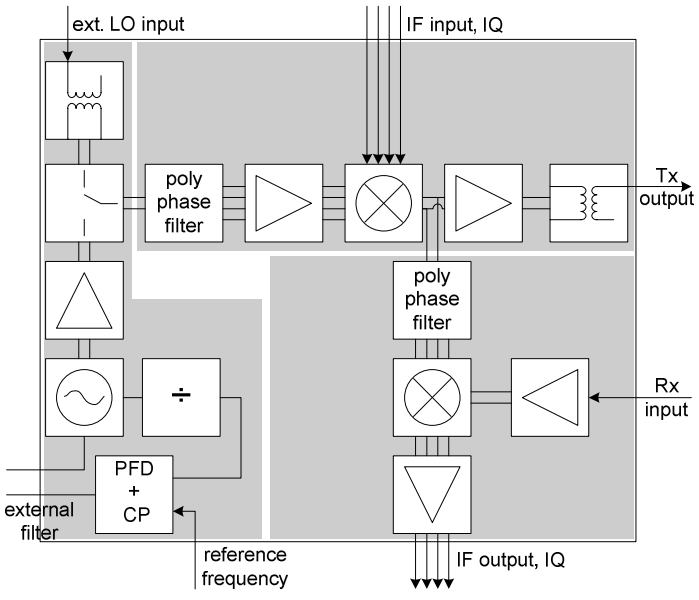

Fig. 1 Block diagram of the integrated FMCW front-end.

The components integrated on chip, grouped per function Tx, Rx and VCO plus PLL are drawn in Fig 1. The core of these FMCW front-ends are two mixers: a single side band (SSB) mixer in transmit and a image-reject mixer (IRM) in receive. Both mixer types are very similar and rely on IQ

signals to ensure proper cancellation of the unwanted products. The signals from the external LO to the SSB mixer and the connection from transmitted frequency-swept X-band signal to the receiver IR mixer both pass through a polyphase circuit to convert the differential signal to 0, 90, 180, 270° out-of-phase signals.

In the transmit chain an amplifier has been added to the output with a balun for a single ended output with a power level that can be used directly for short range FMCW systems. The balun adds the differential signals in-phase, provides impedance matching and the biasing of the output stage.

In the receiver a single ended input is low-noise amplified and made differential. This first amplifier should have a compression level of better than -20 dBm at the input. The isolation between input and output is of prime importance in FMCW systems as this will mask nearby targets. An isolation of minimal 30 dB is needed.

The LO signal is internally generated by a voltage-controlled oscillator (VCO) that is locked to an external signal by a phase-locked loop (PLL). The frequency of operation is determined by the PLL reference signal. An output frequency of 9-10 GHz is required. The output level of the VCO plus buffer should be +2 dBm for best performance of the mixer.

III. MMIC DESIGN

The 0.25 µm SiGe:C BiCMOS process of IHP (Frankfurt\Oder, Germany) has been used [1]. This process features npn-HBTs with 120 GHz transition frequency, lower speed HBTs with 7 V BVCEO and 5 metal layers. The additional CMOS options provide ample possibilities for future integration of extra functionality.

The chip can be divided into three functional blocks: the LO signal generation (VCO plus PLL), the transmitter and the receiver. The lay-out of the MMIC is adapted for packaging in a commercially available QFN package.

A. VCO and PLL circuit

The baseband signal is up-converted using an LO signal of 10 GHz. This signal can either be applied externally or internally by adjusting the on-chip switch to the required position. The internal LO is generated with a PLL circuit that consist of a VCO, divider circuit and a phase frequency detector with charge pump. The VCO is a neg-g_m topology, which has a better phase noise and higher output power than the Colpitts topology. A buffer amplifier and emitter follower are used to prevent the output of the oscillator from pulling effects and to drive a 100 Ω differential input of the switch. A divide-by-100 circuit transfers the 10 GHz signal to 100 MHz. The divider is composed of two divide-by-2 and two divide-by-5 circuits. Both circuits use a master-slave flipflop with bipolar transistors. The divide-by-5 circuit is a modified dual modulus prescaler of 4/5 and uses a NOR gate with three flipflops [2]. A trade-off can be made between current consumption and switching speed. The divide-by-2 circuit operates at 10 GHz and therefore has a higher power consumption than the divide-by-5 circuit, which operates at 2.5 GHz. The output of the divider is compared with a 100 MHz reference signal by a phase frequency detector (PFD) with charge pump.

The PFD is composed of standard digital gates in CMOS [3]. This was possible due to the low reference frequency. A D-flipflop topology with a NAND gate in the feedback is used for the PFD. The advantage of this type of PFD is a fast frequency lock, lower power dissipation, insensitivity to duty cycle variation and less sensitivity to power supply variation. A dead zone mitigation method is used: when the PLL is in lock the up and down pulses of the charge pump are shortly activated to eliminate dead zone jittering. The delay in the feedback is optimised to accomplish this. The charge pump circuit consist of a pair of switched current sources which either sink or source current pulses to a third order loop filter [4]. The charge pump is designed for currents between 100 µA and 1 mA, which is mostly determined by the K_{VCO}. With a lower current the size of the loop filter components could be small enough to be implemented on chip, but this will increase the phase noise. Therefore the current of the charge pump is set to 500 µA and an off-chip loop filter is used. The filter in the PLL is only partially integrated on the chip. It is combined with an external filter because the component values required cannot be realised efficiently on chip. This also gives the user the opportunity to adjust some of the PLL parameters.

ECL to CMOS converter circuits are used to match the voltage levels between bipolar and CMOS circuits in the PLL.

B. Transmit chain

The transmitter uses a single sideband mixer (SSB) for up-conversion of the baseband signal. The mixer consists of 2 Gilbert cell mixers and has four IF and four LO inputs. Both inputs are driven by differential and quadrature (I and Q) signals. At the output of the mixer the quadrature signals are combined to one RF differential output. The IF input of the mixer can be directly connected to a direct digital synthesizer (DDS), without using a buffer amplifier.

The external LO input is a single-ended port and a differential signal is generated by using a transformer as a balun which is connected to the input of the switch. The polyphase filter shifts the phase by 90 degrees to a differential and quadrature signal for the SSB mixer. The design of the polyphase filter has been a trade-off between the insertion loss and the frequency bandwidth. The loss is 13.5 dB for 8 - 13 GHz.

The output of the mixer is amplified through two stages to an output power of 0 dBm which is enough for low power applications. Before the signal is amplified it is split to the receiver part by a resistive splitter. The disadvantage of such a splitter is that it inserts an extra loss of 6 dB. The advantage is a frequency independent behaviour, small size and constant loading. The first amplifier stage is a differential amplifier with an emitter follower at both outputs. The emitter follower is used as an impedance transformer to match the output to the second stage.

The second stage of the amplifier is optimized for output power. The amplifier is terminated with a centre tapped transformer, which provides two functions. First the centre tap is used to bias the collectors of the differential pair. Second it

transforms the high output impedance of the amplifier to a lower value. This impedance is matched with an LC section to 50 Ω. The dimension of the transformer has been designed so the width of the inductor lines could sustain the currents drawn by the transistors. The line width also determines the inductor value and therefore the transformation ratio. The transformer has been simulated with the EM simulation tool Agilent ADS Momentum.

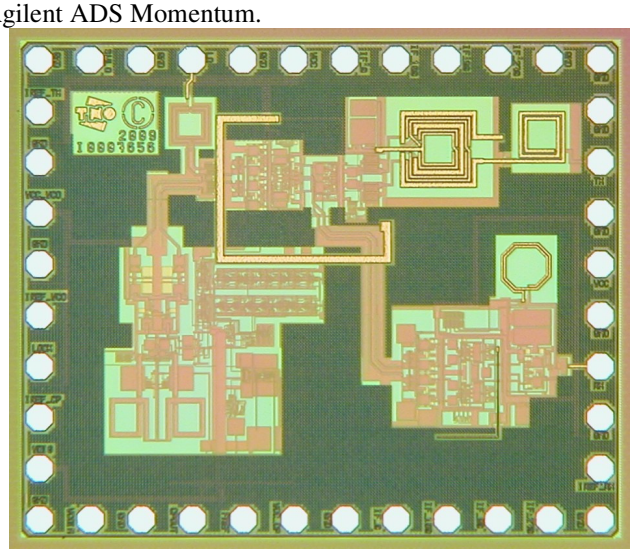

Fig. 2 Photo of the FMCW front-end. The transmitter is located on the top. At the bottom right is the receiver circuit, bottom left the VCO and PLL.

C. Receive chain

The receiver is based on two circuits; a low noise amplifier and an image reject mixer. The LNA is a single-ended amplifier, which is followed by an active balun amplifier to generate a differential signal. The matching of the LNA takes the bond wire inductance and package parasitics into account. The image reject mixer is the same as the mixer in the transmitter and also uses a Gilbert cell topology. The port connections are slightly different, because the input consist of two RF ports and the output has four IF ports. The LO port is still a quadrature differential input. The differential LO signal is coupled from the transmitter and transformed to a quadrature signal with a polyphase filter.

IV. Measurement Results

The MMIC has been measured in a 5x5 mm^2 QFN package with air cavity. The package has been mounted on a test board with the filter components for the PLL and decoupling. For the IF signals a waveform generator has been used that was loaded with sine and cosine waveforms of identical frequency. Transformer baluns were used to obtain IQ differential signals. Output signals are measured with an oscilloscope or spectrum analyser, depending on the needs. An HP noise figure meter has been used to determine the receive noise figure.

The transmitter operates at 5 V, 63 mA. The limits of the frequency band of operation, when defined related to the side-band suppression ratio and output power decrease of maximal 1 dB are 7.5 to 10 GHz. The transmitter output power is with -2…0 dBm 10 dB short of the simulated result (Fig. 3). With the available models and HFSS simulations of the package the discrepancy cannot be explained. When tested with a fixed IF of 200 MHz, the suppressed carrier power is -40 dBm and the lower side band is -40 dBc (Fig 4.).

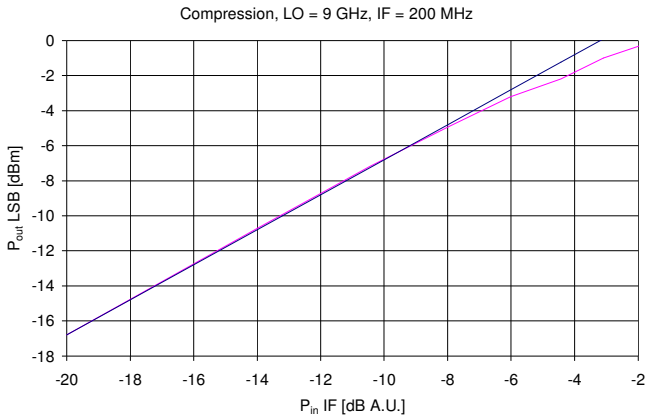

Fig. 3 Plot of the output compression of the transmit chain (including linear fit to determine 1 dB excursion).

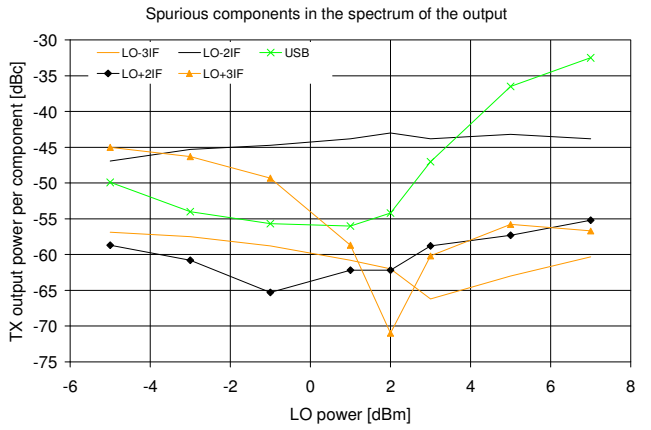

Fig 4 Plot of the spurious components of the transmit chain for different external LO powers.

The input 1dB compression point of the receiver is -11 dBm and the double side-band noise figure is below 7 dB up to 10 GHz, measured from the input to a single IF output (Fig. 5). The conversion gain is 6 dB.

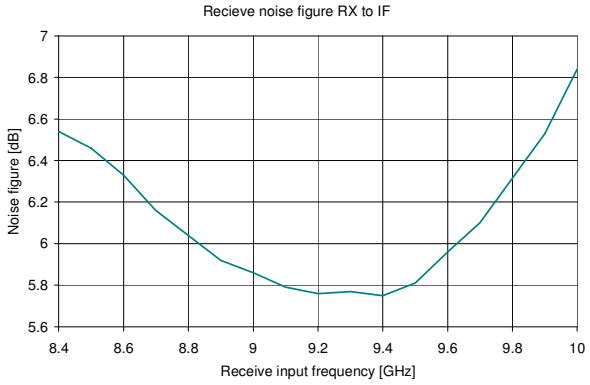

Fig. 5 Plot of the noise figure for the receive path. The signal from Rx input port to IF output has been measured.

These results suggest that although the transmitter output power is considerably lower, the power level in the interconnect from transmitter to receiver is of reasonable value. The two tone 3th order intercept point of the receiver is 0 dBm, where +2 dBm was simulated. The receiver is biased with 5 V, 70 mA.

The VCO is biased from a 5 V supply and draws a current of 45 mA. The PLL and some digital components are biased from a 3 V source at 26 mA. The tuning range of the VCO has been measured without the external filter in place. A total range of 1.2 GHz is measured (Fig 6). With the PLL in place the VCO can be tuned from 8.4 to 9.3 GHz by adjusting the reference signal.

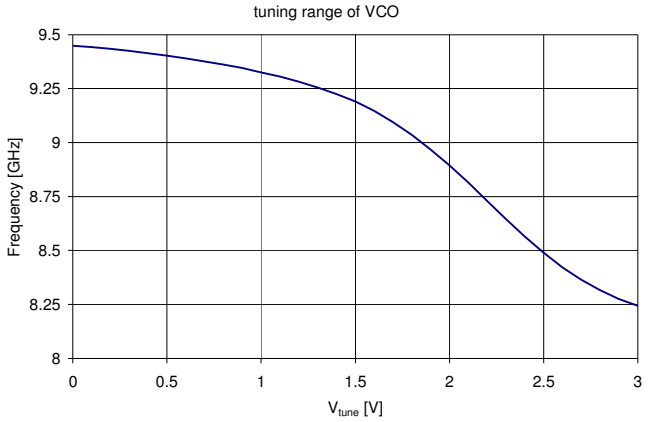

Fig. 6 Tuning range of the VCO in free running condition.

The spurious components originating from the PLL reference are lower than -53 dBc and the phase noise is -77 dBc/Hz at 10 kHz offset (Fig. 7), (Fig. 8).

The total power consumption for the MMIC is 770 mW.

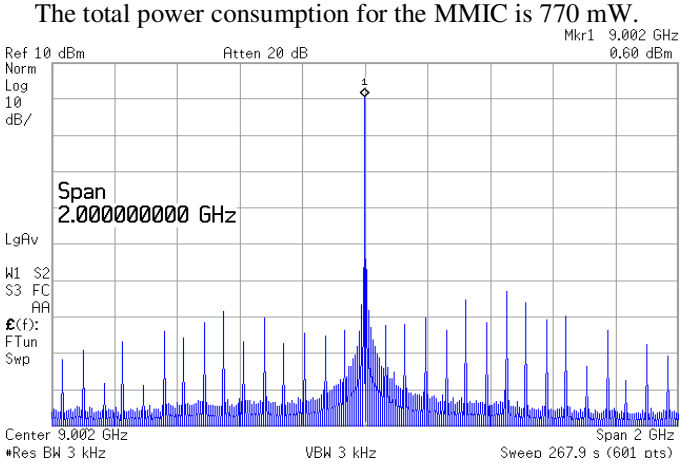

Fig. 7 Spectrum of the output signal of the transmitter with the internal LO at 9 GHz.

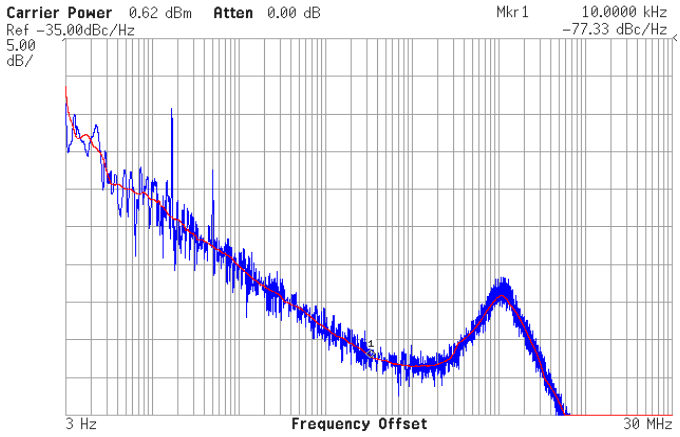

Fig 8. Phase noise plot of the PLL.

V. Conclusions

A single chip X-band FMCW front-end with integrated low-noise amplifier, mixers and local oscillator in a SiGe BiCMOS process has been presented. A chip size of 1.8x1.5 mm^2 opens the possibility of packaging in 5x5 mm^2 or even smaller QFN packages. Side-band suppression of 40 dBc and single-ended output power of 0 dBm has been measured. The frequency of operation of the MMIC with the internal LO is 8.4 to 9.3 GHz. The transmit chain and receive chain have a wider bandwidth which can be used only with an external LO connected. The phase noise of the internal LO source is -77 dBc/Hz at 10 kHz offset and spurious components are below -50 dBc. The receive chain has a noise figure of 7 dB.

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