3.7 A 1.0-to-4.0GHz 65nm CMOS Four-Element Beamforming Receiver Using a Switched-Capacitor Vector Modulator with Approximate Sine Weighting via Charge Redistribution

Michiel C.M. Soer[1], Eric A.M. Klumperink[1], Bram Nauta[1], Frank E. van Vliet[1,2]

[1]University of Twente, Enschede, The Netherlands,
[2]TNO Science and Industry, The Hague, The Netherlands

Phased-array receivers provide two major benefits over single-antenna receivers [1]. Their signal-to-noise ratio (SNR) doubles for each doubling in the number of elements, resulting in extended range. Secondly, interferers can be rejected in the spatial domain for increased link robustness. These arrays can be implemented by phase shifting and summing the signals from antenna elements with uniform spacing. For accurate interference rejection, a phase shifter with uniform phase steps and constant amplitude is desired. Several types of continuous-time phase shifters have been published, e.g. using injection locking [2], phase selection [3] and vector modulation [1,4,5,6]. This paper proposes a phased-array receiver architecture with a *discrete-time* vector modulator that takes advantage of the high linearity and good matching of switched-capacitor circuits, which are highly compatible with advanced CMOS. A simple charge-redistribution circuit is presented that performs a rational approximation of the sine and cosine needed for the vector modulator weights.

The principle of a vector modulator phase shifter is plotted in Fig. 3.7.1 (left) in the form of a phasor diagram. The desired phasor Z with arbitrary phase can be formed by the combination of orthogonal phasors X and Y. These phasors themselves are weighted versions of unity-amplitude phasors I and Q. A positive I and Q correspond to phasors in the first quadrant with a phase shift between 0° and 90°, while the other three quadrants are reached by using negative I and/or Q signals. Because the weights relate to the sine and cosine of the desired phase, a *uniform* step in phase will require a *non-uniform* step in the weights. In a straightforward implementation with uniform weight quantization, this will result in a large number of quantization steps for a much smaller number of phase steps. We propose to approximate the sine and cosine with rational functions $\alpha / (\alpha+¾)$ and $(1-\alpha) / (1-\alpha+¾)$ respectively (where α ranges between 0 and 1), which are plotted in Fig. 3.7.1 (right). With this rational mapping, a *near-uniform* step in phase corresponds to a *uniform* step in α. Moreover, the rational functions are equivalent to the transfer function of a two-element voltage divider, which is easily implemented in analog circuits.

To prove this concept, a 4-element phased-array receiver front-end is implemented in a zero-IF downconverter architecture (Fig. 3.7.2). For each element, a common-gate transistor realizes impedance matching and pre-mixer gain. A 4-phase clock is generated from an off-chip differential clock by division-by-two with dynamic transmission gate flipflops and used to drive a combined mixer/phase shifter implemented with switched capacitors. Summing of the element outputs is performed in the current domain through transconductances loaded by a common resistor. The stages after the common gate are copied four times and clocked with different LO phases to generate a differential in-phase and quadrature output for easy demodulation. The vector modulator phase shifter starts with a 4-phase 25% duty cycle passive mixer [7] that provides downconversion, generates the I and Q vectors (positive and negative) for the vector modulator, and converts the continuous-time signal to discrete time [8]. The discrete-time mixer outputs are buffered, weighted with switched-capacitor circuits, and then summed to form the phase-shifted signal. Because the switched-capacitor circuits run at the same frequency as the mixer, a post-mixer decimation filter is not needed.

One of the four mixer/phase-shifter slices is worked out in detail in Fig. 3.7.3. Not shown are the static switches that select the I and Q polarity. Summing into the final phasor Z is achieved by clocking the I and Q paths with opposite clock phases and connecting the path outputs. The required voltage divider for the sine/cosine approximation is formed by a charge-redistribution switched-capacitor circuit. During the first clock phase, the *variable* capacitor is charged to the voltage of the mixer output and the charge on the *fixed* capacitor is removed. During the second clock phase, the two capacitors are connected together and charge redistributes until the capacitor voltages are equal. Conservation of charge dictates that the resulting voltage is equal to the initial voltage times the ratio of the variable capacitance to the variable and fixed capacitance together. The correct transfer function is achieved if the variable capacitance ranges between *0* and *C*, and the fixed capacitor is *¾C.* As the sum of the two variable capacitors is constant, capacitance is effectively switched *between* the I and Q path and a *single* switchable capacitance bank can be used for each slice, where special care is taken to scale the switch parasitics with the capacitors. The 3b capacitor control enables 8 phases per quadrant, for a total of 32 possible phases (5b). Since the phase shift only depends on the capacitor ratios, the behavior of the proposed vector modulator is insensitive to bias, temperature and frequency.

The chip is implemented in 65nm CMOS (Fig. 3.7.7), with an active area of 0.44 mm^2. Figure 3.7.4 (left) plots the expected and measured vector modulator phasors. When compared to ideal, constant amplitude, uniform phase steps, the phase and amplitude errors of these phasors are plotted in Fig. 3.7.4 (right). The deviation from the expected rational functions of Fig. 3.7.1 is mainly caused by the parasitic capacitance on node Z of the vector modulator (Fig. 3.7.3), which creates coupling between the X and Y vectors. This decreases the phase error, but increases the gain error, resulting in a balanced RMS phase and gain error of 1.4° and 0.4dB respectively. Figure 3.7.5 (top) plots the gain, double sideband noise figure (DSB NF) and 1dB compression point (P_{1dB}) of a single element for different LO frequencies. The -3dB bandwidth after downconversion is 65MHz. Because the total 4-element array has an SNR improvement of 6dB, the sensitivity of the array is equivalent to that of a 4-to-5dB NF single antenna receiver. With a 5b vector modulator, it is possible to make 32 different beams in a phased array configuration. Figure 3.7.5 (bottom) plots eight array beam patterns, measured on packaged samples with four phase-controlled signal generators at the inputs. The beam shapes fit to theory and the depths of the nulls are more than 25dB below the main beam peak. This enables the suppressing of interferers by placing nulls on their angular location, which relaxes the linearity requirement of the baseband circuitry considerably.

The performance is summarized in Fig. 3.7.6. A low RMS phase mismatch of 0.2° and gain mismatch of 0.04dB between elements is achieved due to the good matching of the switched-capacitor implementation. Applications in crowded frequency bands, like the 2.4GHz ISM band, are enabled by the high -1dBm third-order intercept point (IP3). The proposed approximate-sine weighting is elegantly mapped on a charge-redistribution circuit and results in *all* vector modulator settings being used for effective phase shifts.

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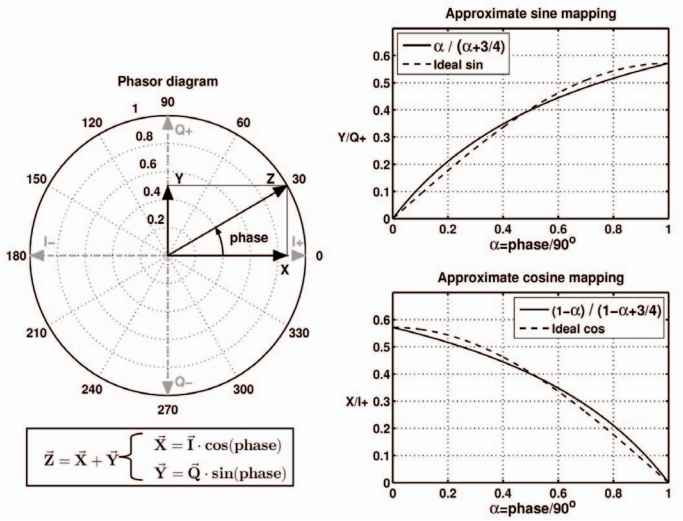


Figure 3.7.1: Vector modulator principle and sine/cosine approximation.

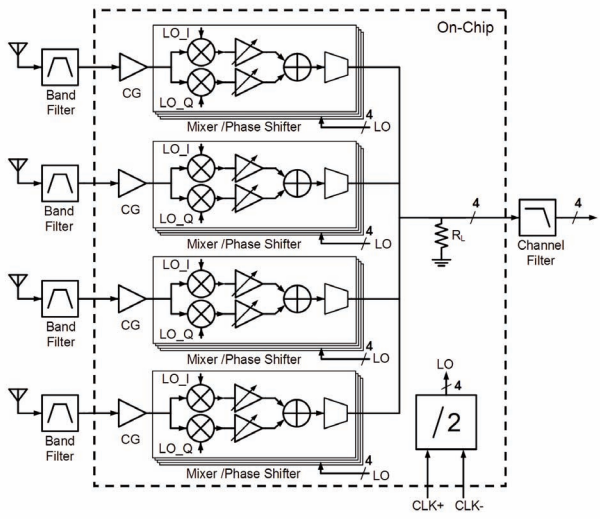
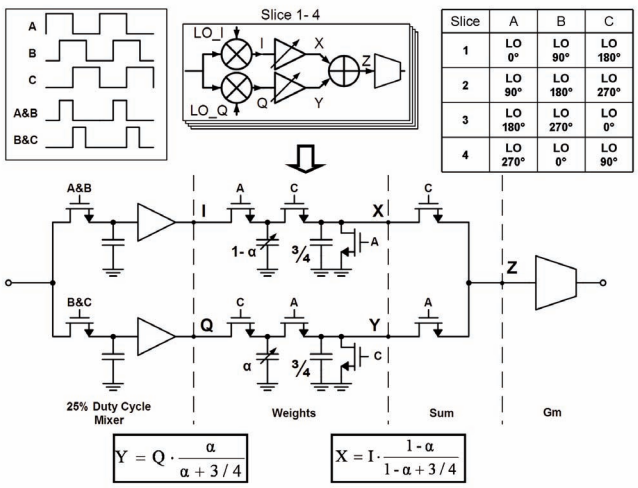


Figure 3.7.2: Phased-array zero-IF receiver front-end architecture.



Slice	A	B	C
1	LO 0°	LO 90°	LO 180°
2	LO 90°	LO 180°	LO 270°
3	LO 180°	LO 270°	LO 0°
4	LO 270°	LO 0°	LO 90°

Figure 3.7.3: Switched-capacitor phase shifter (α=phase/90°).

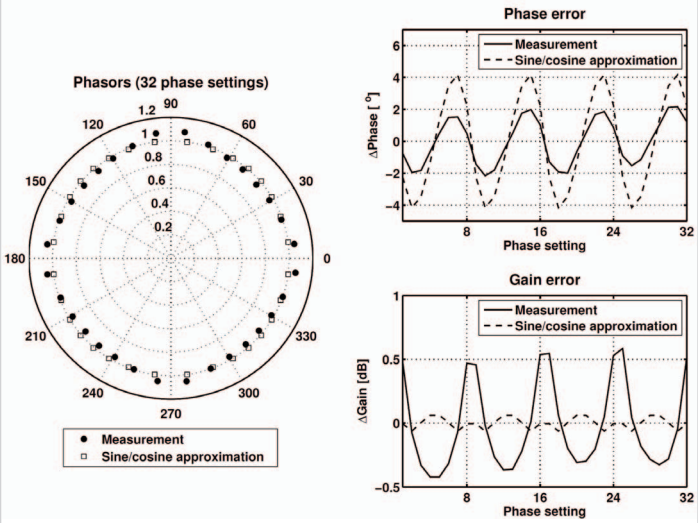


Figure 3.7.4: Measured 5b phase-shifter performance.

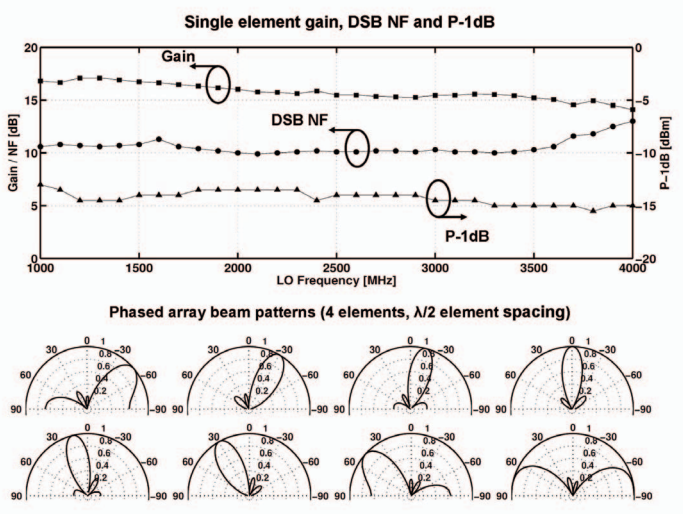


Figure 3.7.5: Measured gain, DSB NF, P_{1dB} and array beam patterns.

Technology	65nm CMOS
Die area	0.9x1.2mm²
RF frequency band	1 - 4GHz
Power consumption	308mW @ 1.2V [1]
Single Element Performance:	@ 2.5 GHz RF
Gain	16dB
Noise figure	10dB DSB
Input-referred 1-dB compression point	-14dBm
Input-referred in-band IP3	-1dBm
Input-referred in-band IP2	40dBm
Vector modulator control	5 bits
Phase shift step	11¼°(5 bits)
Phase error (RMS)	1.4°
Amplitude error (RMS)	0.4dB
Phased Array Performance:	
Array directivity	6dB (4 elements)
Element phase mismatch (RMS)	0.2°
Element amplitude mismatch (RMS)	0.04dB
Peak-to-null ratio	> 25dB

[1] 120mW static, 188mW dynamic @ 2.5GHz RF.

Figure 3.7.6: Performance summary.

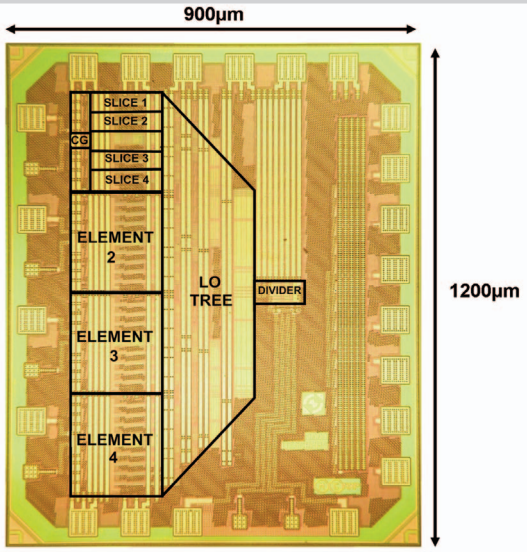


Figure 3.7.7: Chip micrograph.

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