Mismatch Sources in LDMOS Devices

Pietro Andricciola and Hans Tuinhout
Device Modeling and Characterization
NXP Semiconductors, Eindhoven, The Netherlands
Email: pietro.andricciola@nxp.com

***Abstract*— This paper discusses the influence of different sources of DC parametric mismatch in an LDMOS. By comparing measurements and statistical simulations the impact on mismatch of the most important fluctuation causes is qualitatively evaluated. We demonstrate that, whereas the shape of the doping profile in the channel has little effect, both interface states and series resistances play a major role in the mismatch. This work forms a crucial first step towards a better understanding of the random fluctuation mechanisms present in LDMOS devices used in MMICs.**

I. Introduction

The lateral diffused MOS transistor (LDMOS) is widely used in base stations, radar and broadcast applications because of its capabilities to sustain high voltages, delivering substantial power and having good RF performance [1]. However, in monolithic microwave integrated circuits, these devices are employed in analog circuit block implementations under relatively "low power" conditions. The DC parametric mismatch performance becomes important for the functionality of such blocks. Yet the information in the literature about matching of LDMOS [2] is scarce and the fluctuation sources are not analyzed. In this paper we show, for the first time, simulations and measurements on the mismatch fluctuation behavior of LDMOS transistors. In particular, we address the influence of channel doping profiles, random doping fluctuations, interface states fluctuations and series resistance on the different operating regions of the device. The impact of these sources of fluctuation is verified using statistical device simulations and analyzed through parameter extraction and mismatch signatures applied both on these simulations and measurements.

II. Device description

The device investigated in this work is representative of a class of RF-LDMOS transistors fabricated by NXP Semiconductors. A slightly simplified version of the actual LDMOS is reproduced with Synopsys' Structure Editor and simulated with the 2-D Sentaurus Device simulator [3]. A schematic cross section of such a structure is shown in Fig. 1. The channel region is defined by the lateral diffusion of a p-type implantation from the source side of the transistor. This means that the doping in the channel area has a strong non-uniformity along the lateral direction. It is typically about 0.3-μm long. A lightly n-type doped region (drift region) defines the end of the channel area and extends for about 3 μm in these simulations. The channel and the drift region are overlaid with silicon oxide (several tens of nm thick). In this study, the gate electrode covers only the actual channel area leaving the drift region gate-bias independent as is generally the case in LDMOS transistors for RF applications.

This work has been supported by the European Commission under the Marie Curie Action MOICCO and the ENIAC MODERN project.

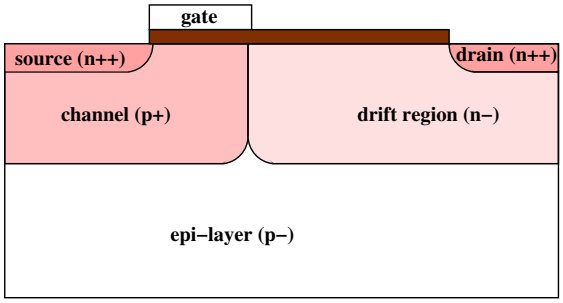


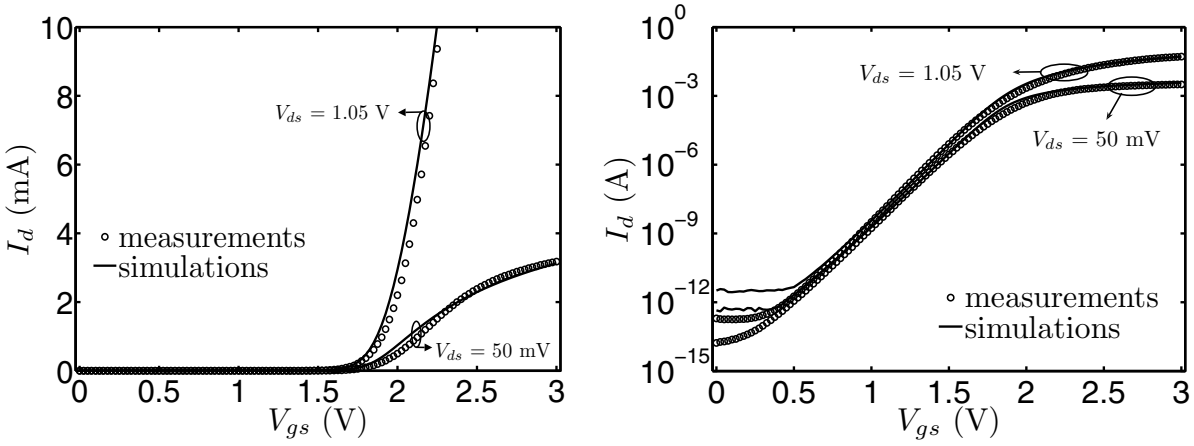
Fig. 1. Schematic cross section of the simulated LDMOS transistor.

III. Measurements

A. Experimental methodology

Parametric mismatch is evaluated by sequentially measuring two identical transistors (width of approximately 1300 μm) on two adjacent reticle placements of the same transistor. In this case implies a distance of about 1.1 mm between the two transistors of the pair. A population of 84 of these so-created "pairs" is spread out evenly over a 200-mm wafer. Measurement results reported in this paper are for two populations positioned on the same reticle field (in the rest of the paper these will be called population 'A' and 'B'). Although devices in a pair are not at the small distance normally applied for matched pairs (< 100 μm), the contribution of the deterministic gradient across the wafer was verified to be negligible compared to the random fluctuations.

The drain current of the LDMOS under test is measured at two different drain biases (V_{ds} = 50 mV and 1.05 V) while sweeping the gate voltage, V_{gs} = 0 to 3.0 V with 25-mV steps. The current of a typical device is plotted and compared with the results of TCAD simulations in Fig. 2. The simulated LDMOS reproduces the measurements very well, with the exception of low gate biases where the measurements and the simulations are dominated by junction leakage which is not tuned for this study. In the remainder of the paper the mismatch analysis will be done on measured (or simulated)



(a) (b)

Fig. 2. Median drain currents of measurements (symbols) and simulations (lines) for both drain-source biases plotted on linear scale (a) and on logarithmic scale (b). The scale of the graph (a) is limited to 10 mA for a better visualization of the curve at V_{ds} = 50 mV.

curves at V_{ds} = 50 mV as these are most suitable to analyze the principal device properties.

B. Results

Measurements of the full gate voltage sweeps as described in the previous section allow evaluation of the so-called mismatch signature. This signature consists of the mismatch fluctuation sweep ($\sigma_{\Delta I_d/I_d}$ vs. V_{gs} [4]), and a well-chosen autocorrelation coefficient curve (correlation between $\Delta_{I_d/I_d}(V_{gs})$ and $\Delta_{I_d/I_d}(V_{gs} = V_T)$ plotted vs. V_{gs}) [5]. Furthermore, the threshold voltage, V_T, and the current factor, β, are extracted (from measurements with V_{ds} = 50 mV) employing three-point extraction with fixed gate overdrive, as for instance described in [6].

The mismatch signatures of the two measured populations are depicted in Fig. 3. As the mismatch below 0.75 V is dominated by junction leakage fluctuations this region will not be considered hereafter. The behavior in weak and moderate inversion of both populations is similar to the one generally observed for conventional CMOS transistors. However, the signature of population 'B' indicates that an additional fluctuating component dominates the mismatch fluctuations in strong inversion (V_{gs} > 2.2 V). Also, the strong de-correlation between the mismatch at threshold voltage and at biases above threshold is more pronounced for population 'B'. This large fluctuation is ascribed to a series resistance variation attributed to a non-ideal probe-to-pad contact. This assumption will be verified with simulations in the next section.

In an attempt to avoid that these resistance fluctuations hamper the extraction of V_T and β, the gate overdrives were limited up to 0.7 V (V_{gs} < 2.5 V). This attempt led to approximately the same standard deviations of V_T and β mismatch for both populations but we had to conclude that the result for β is a grossly exaggerated value. In fact, we calculate a standard deviation of the threshold voltage mismatch of $\sigma_{\Delta V_T}$ = 2.0 mV and a standard deviation of the relative current factor mismatch of $\sigma_{\Delta\beta/\beta}$ = 1.2 %, yielding area factors of

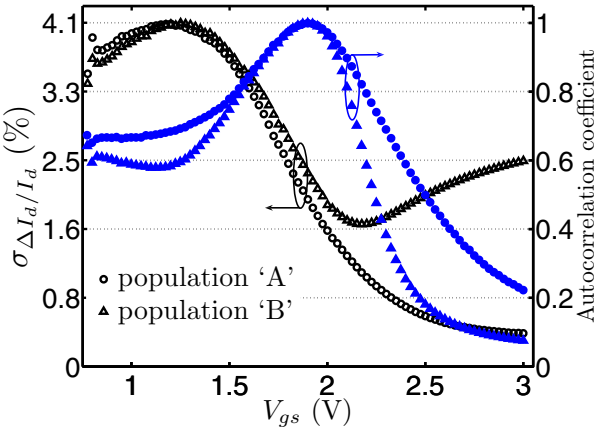


Fig. 3. Mismatch signature of the two measured populations (V_{ds} = 50 mV).

$A_{\Delta V_T} \approx$ 35 mVμm and $A_{\Delta\beta/\beta} \approx$ 21 %μm when the σ's are scaled with the estimated channel area [7]. This area factor of beta mismatch is extremely large when compared to what is expected in standard CMOS technologies (less than 2 %μm [8]). Also, the relative drain current mismatch for population 'A' goes down to about 0.5 % for V_{gs} > 2.5 V (in Fig. 3), while, in principle, the drain current mismatch in the strong inversion regime should be very close to the standard deviation of beta fluctuations [7].

For these devices a combined use of three-point extraction (for threshold voltage evaluation) and mismatch signatures (for drain current mismatch evaluation) is the best analysis method. This method is therefore also used to study how intrinsic device characteristic variations such as different channel doping profiles, dopants and interface states fluctuations as well as external factors, e.g. probe-pad contact resistance fluctuations, affect LDMOS transistors mismatch fluctuations.

IV. Simulations

The study of the possible effect of well defined perturbations to the LDMOS device DC parametric mismatch is performed

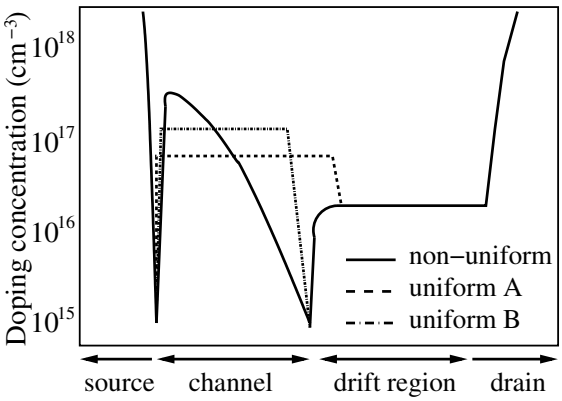


Fig. 4. Representation of the three doping profiles used in RDF-only simulations.

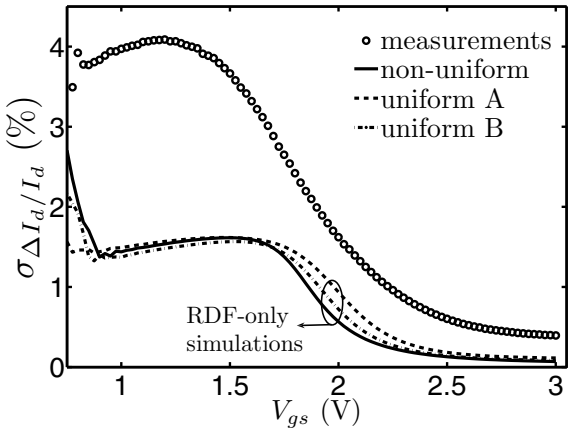


Fig. 5. Comparison between the fluctuation sweep of measured devices (population 'A') and RDF-only simulations with three different doping profiles.

using random device simulations. Three different mismatch contributors are applied to a tuned device through our doping and interface states randomizer [5] and then simulated using Sentaurus Device. The area, over which the doping and the interface states randomizations are applied, covers the channel as well as the drift region. For a good trade-off between computing time and statistical uncertainty the chosen population size is 51.

A. Influence of channel doping profile

An original concern was that the observed mismatch enhancements mentioned in section III-B could arise from the lateral non-uniformity of the channel doping. This has been reported, for instance, in long MOSFETs with pocket implantations [9]. To investigate this, random doping fluctuation (RDF) perturbations have been applied not only on a representation of a realistic laterally-diffused channel doping profile but also on two other devices with artificial constant doping levels. A schematic representation of the three lateral doping profiles is sketched in Fig. 4. The two constant doping profiles have different levels and channel lengths. The doping levels and the channel lengths have been chosen to reproduce approximately the measured electrical performance (for the considered biases).

The fluctuation sweeps of the three configurations, simulated with RDF-only, are compared with the measurements of population 'A' in Fig. 5. For a fair comparison, the results from the device with a longer channel have been scaled with $\sqrt{L}$. All three simulated curves show similar behavior but they all deviate strongly from the measured levels. Thus, when only RDF is taken into account, shape and level of the channel doping apparently have little influence on the overall mismatch performance. Furthermore, the standard deviations of the threshold voltage mismatch and the relative beta mismatch extracted for the three configurations are approximately the same and much lower than the measured values. We calculate for example for the 'uniform A' device (easily comparable with Stolk's theory [10]), $\sigma_{\Delta V_T}$ = 1.1 mV and $\sigma_{\Delta\beta/\beta}$ = 0.1 %. So, calculating the area factors, we obtain: $A_{\Delta V_T} \approx 20$ mVμm ($A_{\Delta V_{T\text{theory}}} \approx 19$ mVμm) and $A_{\Delta\beta/\beta} \approx 1.8$ %μm. Given these observations, the introduction of other sources of fluctuation becomes absolutely unavoidable for a better representation of the relative drain current matching behavior.

B. Other sources of mismatch

The strength of random-fluctuation simulations lies in the possibility of combining and precisely controlling alternative fluctuation causes on a level that is unachievable by technological experiments and measurements. We introduce two additional sources of fluctuations: random interface states (RIF) and random series resistance fluctuations (RSR). It is worth pointing out that the aim of these simulations is to obtain a qualitative description of the impact that a certain fluctuating source has on the mismatch behavior, rather than give a quantitative analysis. This study is primarily focused at identifying the mechanisms that can be held responsible for the observed matching degeneration. Thus, it should not be interpreted as an alternative method for extracting interface state densities or series resistance fluctuations.

As explained in [5], interface states with random energy, concentration and position are assigned to the interface between the gate oxide and the silicon. The energy is randomly selected in the bandgap of the silicon and the nominal concentration follows a parabolic shape that ranges from 1×10 cm^{-2} at midgap to 5×10 cm^{-2} at the extremes. RIF should affect primarily the mismatch below threshold.

Above threshold, however, series resistance fluctuations may dominate the fluctuations. The currents delivered by these 1300-μm wide test devices are of the order of milliAmps (Fig. 2). This means that a significant potential can drop over a contact resistance of few tenths of an Ohm. To investigate this impact on the mismatch signature, two series resistances are randomly varied and assigned to the source and drain electrodes respectively. In order to reach the two levels of fluctuation in strong inversion (for the two measured populations), as shown in Fig. 3, two different ranges of resistances, representing a 'bad' and a 'good' probe-pad contact, are simulated. The variations, around a median value of 1 Ω, are

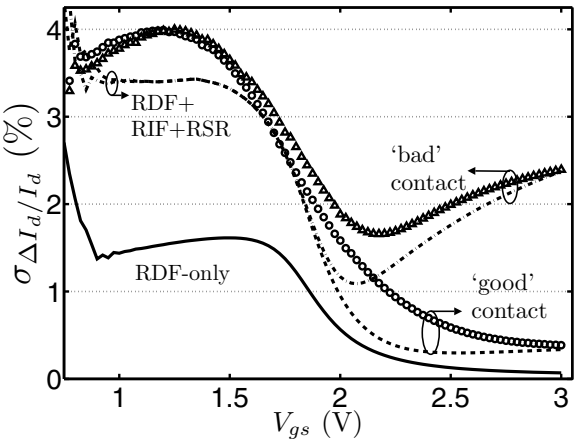


Fig. 6. Fluctuation sweeps for simulations of different sources of mismatch (lines) and measurements (symbols).

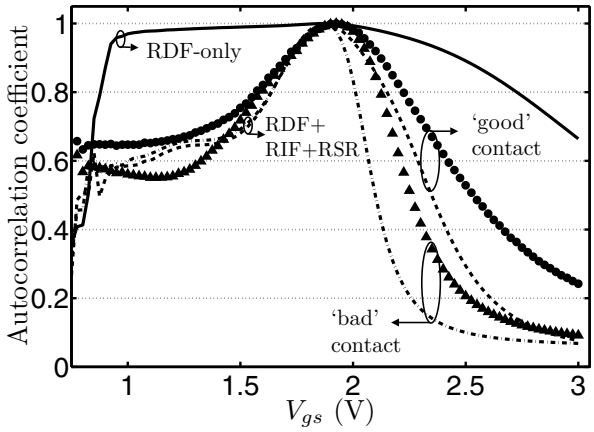


Fig. 7. Autocorrelation plot for simulations of different sources of mismatch (lines) and measurements (symbols).

chosen from a uniform distribution at $\pm$ 0.3 Ω and $\pm$ 0.05 Ω for the 'bad' and the 'good' contact respectively.

C. Discussion

Figures 6 and 7 show the mismatch signatures when RIF and RSR are added to the original RDF randomized device population with the non-uniform doping.

The level of mismatch in weak and moderate inversion is much better described by the combination of RIF and RDF (the current is too low in this region for the RSR to contribute). Also, the standard deviations of V_T and β mismatch now reach values comparable to the measurements: 2.3 mV and 0.8 % for $\sigma_{\Delta V_T}$ and $\sigma_{\Delta\beta/\beta}$, respectively. It is worth noticing that, unlike what was found for standard CMOS technologies, RIF strongly affects beta mismatch in LDMOS device populations when characterized near the peak transconductance point.

In the strong inversion region, the simulations with the two levels of RSR match very well with the two measured populations. The autocorrelation plot confirms the need of these additional independent fluctuation sources for a good description of the overall mismatch behavior. However, it cannot be denied that some discrepancies still remain in the moderate inversion region of the fluctuation sweeps (between 1.8 V and 2.5 V in Fig. 6), and between the autocorrelation plot of the simulated 'good' contact and the population 'A' (V_{gs} > 2 V in Fig. 7). These differences can most likely be minimized by optimizing the interface state density and energy distributions. This is however beyond the scope of this paper.

This analysis represents an important step towards performance improvements for MMICs through a better understanding of the mismatch dynamics in LDMOS devices.

V. Conclusion

This paper reports for the first time a study on parametric mismatch fluctuation causes in LDMOS devices. Measurements on transistor pairs show relatively large drain current mismatch fluctuations in all regions of operation. Three sources of fluctuations have been analyzed by statistical simulations. We found that, if only random dopant fluctuations are taken into account, the shape and level of the channel doping cannot explain the observed mismatch behavior of this category of MOS devices. On the other hand, random interface states significantly affect the behavior of the device in subthreshold as well as in moderate inversion, also increasing the fluctuations of beta. Finally, we showed that particular care must be taken during the characterization of these devices in terms of probe-pad contact resistance, as series resistance variation can easily dominate the fluctuations at high gate biases.

Acknowledgment

The authors would like to thank their colleagues Jan de Boet and Henk Jan Peuscher for bringing this interesting subject to their attention.

References

[1] [Online]. Available: http://www.nxp.com/rfpower
[2] W. Posch, C. Murhammer, and E. Seebacher, "Test structure for high-voltage LD-MOSFET mismatch characterization in 0.35μm HV-CMOS," in *Proc. ICMTS*, 2009, pp. 96–101.
[3] *Sentaurus Device User Guide (A-9.2008)*, Synopsys, 2008.
[4] N. A. H. Wils, H. P. Tuinhout, and M. Meijer, "Influence of STI stress on drain current matching in advanced CMOS," in *Proc. ICMTS*, 2008, pp. 238–243.
[5] P. Andricciola, H. P. Tuinhout, B. de Vries, N. A. H. Wils, A. J. Scholten, and D. B. M. Klaassen, "Impact of interface states on MOS transistor mismatch," in *IEDM Tech. Dig. Papers*, 2009, pp. 711–714.
[6] J. A. Croon, *et al.*, "A comparison of extraction techniques for threshold voltage mismatch," in *Proc. ICMTS*, 2002, pp. 235–239.
[7] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Webers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1433–1440, Oct. 1989.
[8] H. P. Tuinhout, "Electrical characterisation of matched pairs for evaluation of integrated circuit technologies," Ph.D. dissertation, Delft University of Technology, 2005.
[9] A. Cathignol, S. Bordez, A. Cros, K. Rochereau, and G. Ghibaudo, "Abnormally high local electrical fluctuations in heavily pocket-implanted bulk long MOSFET," *Solid-State Electronics*, vol. 53, pp. 127–133, Feb. 2009.
[10] P. Stolk, F. P. Widdershoven, and D. B. M. Klaassen, "Modeling statistical dopant fluctuations in MOS transistors," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1960–1971, Sept. 1998.