DIRECT ELECTROPLATING ON HIGHLY DOPED PATTERNED SILICON WAFERS

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Abstract *— Nickel thin films have been electrodeposited directly on highly doped silicon wafers after removal of the native oxide layer. These substrates conduct sufficiently well to allow deposition using a periferical electrical contact on the wafer. Films 2 μm thick were deposited using a nickel sulfamate bath on both n+ and p+-type silicon wafers, where a series of trenches with different widths had been previously etched by plasma etching. A new, reliable and simple procedure based on the removal of the native oxide layer is presented which allows uniform plating of patterned substrates.*
Key Words*: MEMS, nickel, silicon electroplating, electroforming*

I INTRODUCTION

The relatively inexpensive equipment together with the excellent via/trench filling properties are the major advantages of electrodeposition over other methods of thin film production. However, electrodeposition has one feature that can be a major disadvantage, namely the need of a conducting substrate or a substrate with a conducting seed layer previously sputtered or evaporated on top. The possibility of electroplating directly on semiconducting silicon substrates removes the need of using this seed layer making the process simpler. This has direct consequences in micromechanical systems (MEMS), for example in the three dimensional structuring possibilities.

Electroplating relies on making electrical contact from the power supply to the ionic solution through an anode and cathode (wafer). In order to avoid significant resistance to the current and to provide a uniform current distribution, the sheet resistance ($R_{\square}$) should be low, typically under 0.5 Ω per square [1]. In the case of a wafer with a 0.01 μm Cr adhesion layer and a 0.1 μm thick Au conducting layer on top, this resistance is about 0.2 Ω per square (Table 1). The resistance of the wafer should be taken into account when the conducting layer is left out. Normally doped silicon wafers (p or n-type) show a much higher resistance, two orders of magnitude higher than with conducting layer. Highly doped silicon wafers (p+ or n+-type) offer a resistance comparable to that of a normal wafer with a conducting layer. This means that only highly doped Si wafers can conduct sufficiently well to allow electrodeposition in the same way as wafers with a conductive seed layer on top.

In practice, another factor has to be taken into account when plating without a seed layer. An oxide layer of about 1 nm thickness is present on a silicon wafer as received from the supplier. This oxide is called native oxide and forms on every bare silicon surface exposed to air. This very thin layer of oxide offers a very high resistance to the current and it is enough to avoid electrical contact between the electrode and the wafer making it impossible to proceed with electroplating.

Although electroplating is typically carried out on a metal seed layer, deposition on silicon is not new and it has been reported a few times for different metals and metal alloys [2,3]. In the following sections a new procedure to electroplate nickel directly onto highly doped silicon wafers will be presented. This procedure leads to successful results when electroplating etched high aspect ratio trenches and buried channels. Removing the native oxide layer from the surface of the wafers and avoiding getting it again is a key issue during our experiments.

II BARE SI WAFERS

The experiments were carried out with four types of (100) oriented silicon wafers: p / Boron, n / Phosphorus, p+ / Boron and n+ / Antimony. The wafers were cleaned using HNO_3 to remove organic contaminants and then etched in 1% HF, to remove the native oxide and inorganic particles from the wafer surface. It is known from literature [4] that silicon surfaces etched in dilute HF solutions are highly resistant to oxidation in air due to the termination with hydrogen. After this the wafers were rinsed just for a few seconds with

deionized water using a shower head in order to remove the acid and then spin dried.
The nickel plating bath consists of eight liters of nickel sulfamate solution at 55°C with an insoluble Pt/Ti mesh anode. While the oxide growth on HF treated Si surfaces proceeds extremely slowly in air, it was observed that just a few seconds in the electrolyte at 55°C were enough to hinder the growth of nickel. In order to minimize oxidation reactions between the substrate and the constituents of the electrolyte, the anode was inserted in the bath with a second probe prior to the immersion of the wafer. Wafers of each type were used following this process using a current density of 4 A/dm^2 and pH between 4 and 4.5 at 55°C.
While successful results are obtained for the highly doped wafers (n+ and p+-type), n and p-type wafers remain unplated. In our set-up the contact to the silicon wafers of the plating power supply is applied at the perimeter of the wafers only, on the surface to be plated. Using this configuration the effective resistance is given by $R_{\square}$, which is directly proportional to the resistivity, and it is probably due to their much higher resistivity that the n and p-type wafers are not plated. When a large contact would be placed on the backside of the sample, a back plate electrode, the total resistance, $R_{\perp}$, becomes a function of the area to be plated (0.66 dm^2 in our case). This resistance calculated in Table 1 for the different possibilities is much smaller and in this way nickel plating on n and p-type wafers might be successful [3].

	Au/ Cr/ p						
	Au	Cr	n+	p+	n	p	
t (μm)	0.1	0.01	525	475	525	525	
ρ (Ω·μm)	0.022	0.13	200	150	50000	50000	
$R_{\square}$ (Ω)	0.2		0.4	0.3	95	95	
$R_{\perp}$ (Ω)	0.04		$1.6 \cdot 10^{-4}$	$1.6 \cdot 10^{-4}$	0.04	0.04	$R_{\square} = \rho / t$ $R_{\perp} = \rho \cdot t / A$, $A = 0.66 \cdot 10^9$ μm^2

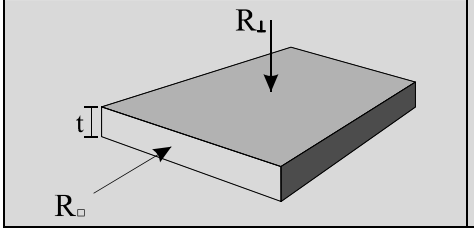

Table 1: Values of the resistivity (ρ), the sheet resistance ($R_{\square}$) and the wafer resistance ($R_{\perp}$) as a function of thickness and material

III PATTERNED SI WAFERS

An important issue during MEMS processing is the ability to plate and fill high aspect ratio structures evenly, enabling a void free nickel filled trench. Conformal plating is an even growth from all surfaces resulting in a deposit of equal thickness at all points. In order to study these trench filling capabilities, some tests were made on highly doped wafers.
After starting with a "standard" initial procedure, the results were used to come to an adapted procedure. Although the results improved, the adapted procedure was not yet satisfying and a final procedure was introduced.

III.1 INITIAL PROCEDURE

The trench pattern used in our experiments was defined by optical lithography using an EVG 620 mask aligner on p+-type (100) oriented silicon wafers from Okmetic Oyj. After spin-coating the wafer with the adhesion promoter HMDS and a 3.5 μm thick positive resist layer (Olin 908-35), it was exposed during 12 seconds to 12 mW/cm^2 UV light. After exposure the resist layer was developed in Olin OPD 4262. The wafers were then etched by plasma etching using C_4F_8/ SF_6 steps [5,6] forming vertical trenches.
After standard HNO_3 cleaning to remove the photoresist, the wafers were ashed in oxygen atmosphere at 800°C to remove the fluorocarbon film which is deposited during the plasma etching process on the walls of the trenches. The wafers were immersed for 5 minutes in 50% HF solution to remove the oxide film created during ashing and to lift the carbon residue from the oxide surface. Just prior to nickel plating the wafers were dipped in 1% HF, rinsed with a shower head and spin dried. Wafers following this initial procedure showed clear preferential areas to plate: the walls and bottom of the trenches (Fig.1a).

III.2 ADAPTED PROCEDURE

In order to avoid any contact of the surface of the wafer with water, delaying in this way the native oxide growth, it was decided to immerse the wafers in ethanol directly after the 1% HF dip and to spin them dry afterwards. This new step in the processing led to uniform coverage of the structures (Fig.1b).

(a) Initial procedure

(b) Adapted procedure

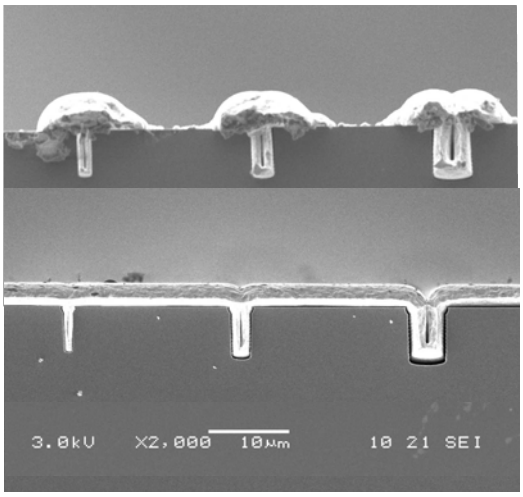

Figure 1: Cross section of a p+ silicon wafer with 7µm deep trenches on it and electroplated nickel on top.

At this stage it was also decided to eliminate the 50% HF step. It is known that 50% HF etches and chemically modifies the surface of the wafer changing it in an uncontrolled way. To remove the oxide layer, 1% HF solution during 5 minutes was found to be sufficient.

III.3 FINAL PROCEDURE

A consequence of removing the oxide layer with a HF solution is that wafers become hydrophobic, i.e. the wafer surface tends to avoid contact with water. However, the electroplating solution is water-based and therefore the silicon wafers tend to avoid contact with the nickel sulfamate, leading to trapped air bubbles in the structures. Especially the high aspect ratio smaller structures show this problem, resulting in bubble shaped areas that are hardly plated or not at all plated (Fig.2a). As the bubble shaped areas were found to be always at the same side of the trenches all over the wafer, it was concluded that air was trapped during immersion of the wafer in the electrolyte.

This inherent problem can be solved by spraying the wafers with ethanol just before introducing them into the plating bath. Although the wafers are hydrophobic, they are found to be "ethanolphilic", i.e. they are completely wetted with ethanol. In this way air bubbles are avoided leading to successful plating of all structures (Fig.2b). A big advantage of this wetting method is that due to the temperature of the bath, the ethanol is believed to evaporate leaving no traces in the bath solution as would be the case with conventional wetting agents.

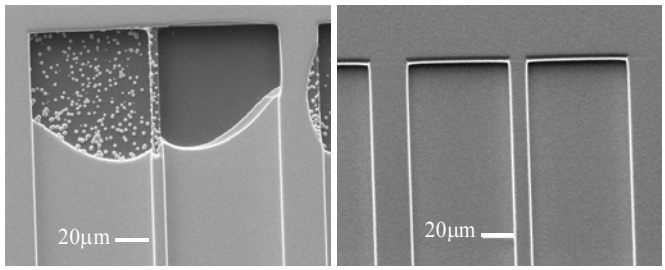

Figure 2: Top view of a silicon trench on a n+ wafer, covered with 2 µm nickel film. (a) Adapted procedure: in the left trench an air bubble was trapped and released after some time, in the right one the bubble stayed all the time inhibiting plating (b) Result after improved wetting conditions using the final procedure

The final procedure of direct nickel plating on highly doped silicon is then as follows:

- photolithography
- deep trench plasma etching
- HNO_3 cleaning
- ashing at 800°C in oxygen
- 1% HF dip during 5 minutes
- ethanol dip, 5 minutes
- spin dry.
- mount wafer on plating holder
- potential is applied with additional anode probe
- spray wafer with ethanol
- immerse wafer in electrolyte
- plate with nickel.

IV BURIED CHANNELS

Using this final procedure, trenches have been used as the basis for the fabrication of microchannels buried in n+ Si wafers [7] (Fig.3). The wafer is covered first with photoresist and patterned by lithography and directional etching. Trenches are conformally coated with a polymer which is removed at the bottom of the trench. The structure is isotropically etched in the bulk of the substrate. After stripping of the coating the structure is filled with nickel. Depending on the thickness of the nickel film and the dimensions, the trenches may be completely sealed.

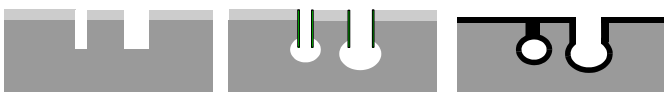

Figure 3: Buried channels fabrication scheme.

Three different wafers were prepared using different etching times for each:1, 3 and 9 minutes,

which led to depths of around 6, 13 and 23 µm respectively for the 2 µm wide trench. The samples were coated with nominally 2 µm of nickel (Fig. 4). In the close-ups it can be observed that the growth of the nickel layer is still in its early stadium for the deepest trench. There, the 3D nickel island growth can be clearly noticed. For the other two depths, the islands have already coalesced forming a continuous film. The nucleation and growth of electroplated nickel follows the Volmer-Weber model [8].

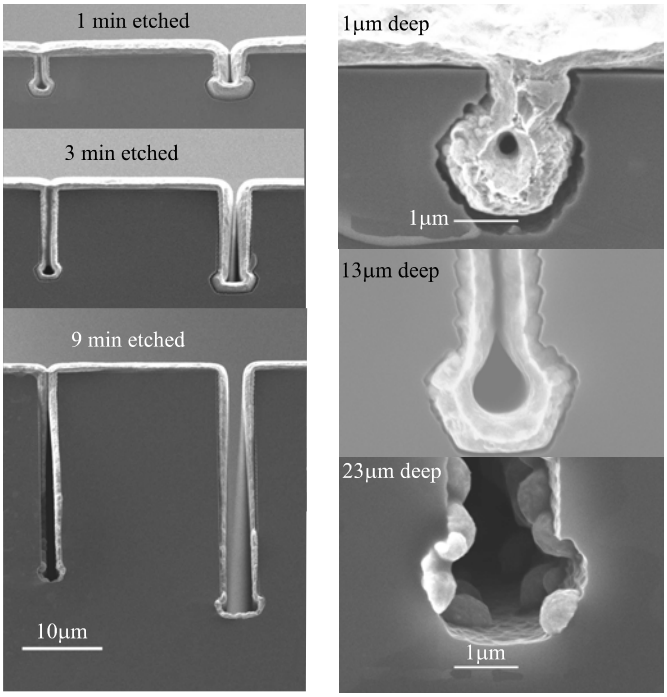

Figure 4: Cross sections of the nickel electroplated buried channels with a film thickness of about 2µm. On the left 2 µm and 4µm trenches are observed for different etching times. On the right close-ups of the 2 µm trenches show the difference in growth at the bottom.

During electroplating of high aspect ratio structures with different widths, the deposition rate decreases with increasing depth. This is probably due to the combination of two effects: diffusion and electric field effects. For deep narrow trenches mass transfer takes place via diffusion, which means that the nickel ions move from a higher to a lower concentration inside the trench. If the supply of nickel ions is hampered, a concentration distribution inside the trench can be expected. On the other hand, due to the trenches the electric field lines will also be disturbed. Because the trenches are conducting on the whole length not all the field lines will reach the bottom of the trench, causing in this way a lower current density and subsequently a thinner film. A thorough study of these effects is necessary to reveal the dominant cause.

V CONCLUSION

Electroplated nickel films have been successfully deposited on highly doped silicon wafers. A method to obtain conformal deposition in deep structures has been presented, where all the effort is put in removing the native oxide layer and avoiding getting it again. Both, applying the plating potential with an additional anode probe before immersion in the electrolyte and the use of ethanol instead of water after HF, are found to be crucial and result in uniform filling. The problem of air bubbles being trapped in the trenches as the wafer is introduced into the solution has also been solved using ethanol, this time as a surfactant.

The procedure presented here is an easy method to electroplate highly doped wafers and leads to full coverage of high aspect ratio trenches. It might also enable the plating of normally doped wafers using a back plate electrode. For deep and narrow structures, such as buried channels, it was found that at the bottom, the nickel layer is thinner than at the top. Future studies are necessary to clarify the causes of this effect.

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