Embedded Instruments for Enhancing Dependability of Analogue and Mixed-Signal IPs

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***Abstract*—The idea of an embedded instrument (EI) is to embed some form of test and measurement into silicon to characterize, debug and test chips. The concept of the EI is different from build-in self test (BIST) and other kinds of monitors by the fact that embedded instruments can provide the user with rich and detailed information with respect to the performances of the target, not just a *true/false* indication. In this paper, two embedded instruments for analogue and mixed-signal IPs focusing on dependability applications are introduced. They are the EI for measuring MOS transistors' threshold voltage and the EI for testing OpAmps' gain and offset. Measurements as well as simulation results are provided to validate these EIs and show their efficiency in monitoring the ageing of analogue and mixed-signal IPs in their life time, and enable the path to enhance dependability.**

I. Introduction

In safety-critical applications, such as automotive, dependability is used more frequently than reliability. Dependability is a group of concepts which is originally used in system-level specifications. In the case dependability is focused on the analogue and mixed-signal IP level, its definition is limited down to four concepts: reliability, maintainability, availability and safety [1]. In principle the dependability of an IP should answer the following questions: when the IP is expected to be out of performance due to ageing (Reliability), how to repair the IP when it is out of performance (Maintainability), how long is the IP not available due to this repair (Availability) and will the IP cause a safety problem due to its out-of-performance (Safety)?

In nanometre CMOS technologies, there are several reliability effects that prevail, such as negative/positive bias temperature instability (NBTI/PBTI), hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB) and channel hot-carrier (CHC). These reliability effects tend to increase the threshold-voltage of single MOS transistor in time and hence reduce its drain current. The consequence for analogue/mixed-signal IPs is certain performance reduction. For example, the NBTI reliability effect can increase the OpAmp's offset and reduce its gain [2].

The detection of such performance degradation is essential for further maintainability and availability related procedures. It could be a simple alarm signal and give an indication whether the circuit is within the specification or not. However, an accurate measurement for the degraded performance will be more preferred, because the function "repairing" can be done in the digital domain by pure software based on accurate measurement results. The hardware overhead will be minimized in that case.

An existing solution for measuring the degraded performance is using an embedded-instrument (EI) [3]. It provides on-chip test IPs which are connected through standard buses and protocols (IEEE P1687) [3]. These on-chip EIs are supposed to test basic physical parameters like voltages, currents, temperatures, as well as performance parameters of analogue/mixed-signal IPs. These embedded instruments are primarily aimed for functional tests. After functional tests they can be employed for dependability purposes during the SoCs life time as well. This paper will present two EI examples for the use of dependability. The first one is a threshold-voltage measurement EI for MOSFETs, which will be introduced in Section II. It can measure the threshold-voltage of a MOS transistor periodically and extract the change in threshold-voltage which is caused by reliability effects. In Section III, the second EI will be discussed, which is an offset and gain EI for analogue OpAmps. Simulations and measurements for these two EIs will be provided in Section IV. Section V will provide conclusions.

II. The Embedded Instrument for MOSFETs' Threshold-Voltages

The threshold-voltage is one of the most sensitive parameters in MOS transistors in terms of reliability. Many reliability effects, like NBTI/PBTI, HCI, TDDB and CHC, tend to increase the absolute value of the threshold-voltage with stress time. Therefore, measuring the threshold-voltage repeatedly during MOSFET's lifetime is highly demanded. Traditionally, the threshold-voltage is measured by complicated equipment like probe stations and a semiconductor parameter analyzer. It increases the cost and limits the time period to observe the threshold-voltage shift. On the other side, billions of SoCs are produced every year and used in almost all kinds of application areas. Most of them include both ADCs and DACs in moderate accuracy (10 to 12 bits). The EI introduced in this section provides a way to measure the MOSFET's threshold-voltage using these on-chip ADCs and DACs.

The threshold-voltage (V_{th0}) can not be measured directly [4]. It is normally extracted from the drain current measurement at various gate and drain voltages with compact models. The drain current can be measured in the sub-threshold regime or in the strong-inversion regime. Measuring in the sub-threshold regime needs a high accuracy and resolution; for

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example, measuring 100 pA with a resolution of 1 pA or better [5], which places a tough requirement on the design and offset calibration. Measuring in the strong-inversion regime takes advantage of the large drain current and low offset influence. However, it requires accurate compact models to extrapolate the drain current from the strong-inversion regime down to the sub-threshold regime. To be able to extract V_{th0} on-chip based on the drain current measured in the strong-inversion regime, a new MOS model for the nanometre MOS drain current I_d, which is valid for all MOS operation regimes, is expressed in (1) to (5) [6]:

$$I_d = F_{sd} - F_{ds} \tag{1}$$

$$F_{sd} = \frac{\beta \cdot ln^2\left[1 + exp\left(\frac{V_p - V_s}{2V_T}\right)\right] \cdot \left(1 + \frac{V_d - V_s}{V_A}\right)}{\left\{1 + x \cdot V_d \cdot ln^\alpha\left[1 + exp\left(\frac{V_p - V_s}{2V_T}\right)\right]\right\}^{\frac{1}{\alpha}}} \tag{2}$$

$$F_{ds} = \frac{\beta \cdot ln^2\left[1 + exp\left(\frac{V_p - V_d}{2V_T}\right)\right] \cdot \left(1 + \frac{V_s - V_d}{V_A}\right)}{\left\{1 + xV_s \cdot ln^\alpha\left[1 + exp\left(\frac{V_p - V_d}{2V_T}\right)\right]\right\}^{\frac{1}{\alpha}}} \tag{3}$$

$$V_p = \frac{V_g - V_{th0}}{n} \tag{4}$$

$$V_T = \frac{kT}{q} \tag{5}$$

The MOS terminal voltages are all refer to the substrate and expressed as V_d, V_g and V_s. In (1), the model employs a similar idea as the EKV model [7], which is the forward current F_{sd} and the backward current F_{ds}. However, unlike the EKV model where the forward current is independent of V_d and backward current is independent of V_s, the new model forward current (2) and backward current (3) are modulated by both V_d and V_s. V_T is the thermal voltage, which is around $26mV$ at room temperature. Parameters k, T and q are the Boltzmann's constant, temperature in Kelvin and the electrical charge of an electron respectively. V_p is the pinch-off voltage and n is the slope factor, which is linked to the weak-inversion slope. V_{th0} is the zero body bias threshold-voltage which is interesting with regard to reliability measurements. In (2) and (3), β is a fitting parameter for mobility, width-to-length ratio and gate oxide capacitance per unit area, like $\mu C_{ox} W/L$ in the classic square-law model. Parameters x and α take into account the velocity-saturation effect. Drain-induced barrier lowering (DIBL) and the short channel effect are taken into account by the parameter V_A.

One problem is the temperature, because this will change the V_{th0} too and has sometimes a stronger influence than reliability. In order to decouple the temperature influence from reliability-induced V_{th0} shift, normally an accurate temperature sensor would need to be incorporated. However, in our opinion the temperature effect can be disconnected without a temperature sensor. This is achieved by using a well matched MOS transistor pair as shown in Fig. 1. Ageing mechanisms in a nanometre MOS transistor which change V_{th0} like NBTI, PBTI, HCI, CHC and TDDB, are actually changing the surface-state charges in the silicon-dioxide. The threshold shift caused by the surface-state charges is NOT a function of temperature. This can be proven from the definition of the threshold-voltage expression (6). Surface-state charges are Q_{ss} in (6). It is divided by the gate-channel capacitance C_{ox} and then added to the threshold-voltage. No temperature is

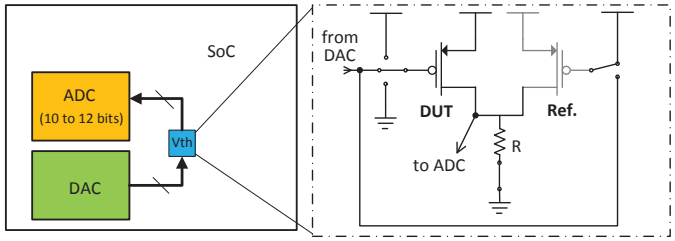

Fig. 1. The proposed EI for measuring the V_{th0} ageing behaviour inside a SoC.

involved when calculating the threshold-voltage change from the surface-state charges change. As a result, the V_{th0} shift by ageing can be simply measured by the difference in V_{th0} between the reference transistor and the DUT aged transistor. They are at the same temperature and matched well, so the difference in V_{th0} should all come from reliability effects (and initial mismatch).

$$V_{th0} = V_{FB} + \frac{Q_{ss}}{C_{ox}} + 2\varphi_b + \gamma_N\sqrt{2\varphi_b} \tag{6}$$

The idea to measure the V_{th0} on-chip is shown in Fig. 1 [6]. Two matched MOS transistors, *DUT*, *Ref.* and one load resistor *R*, are added into a SoC. The transistor *DUT* will be stressed, while transistor *Ref.* will be unstressed and works as a reference fresh device. A general purpose ADC and DAC in the SoC are applied to sweep each transistor's gate voltage and measure the voltage over the load resistor at the same time. The measurement results are processed by the embedded CPU inside the SoC with the help of the MOS drain current model. The gate of the transistor *DUT* is connected to the DAC to sweep the voltage from ground to the power supply. The transistor *Ref.* is turned off by connecting its gate to the supply (PMOS). The voltage at the load resistor *R* is measured by the ADC at each DAC sweeping step. Now the drain voltage V_d of the *DUT* can be calculated by the difference of the supply voltage V_{dd} and the ADC measured voltage V_{ADC}. The drain current I_d can be calculated as the ADC measured voltage V_{ADC} is divided by the load resistance R. With the help of the new MOS model in (1) to (5), the ADC measured voltage V_{ADC} can be expressed as in (7) and (8):

$$I_d = \frac{V_{ADC}}{R} = F_{sd} - F_{ds} \tag{7}$$

$$V_{ADC} = R \cdot F_{sd} - R \cdot F_{ds} \tag{8}$$

Based on the F_{sd} and F_{ds} expression in (2) and (3), it is interesting to note that the load resistance R can be absorbed into the parameter β as one model fitting parameter. So the accurate value of R is not required to be known in advance. Six model parameters (including V_{th0}) can then be extracted. After that the V_{th0} of transistor *DUT* is obtained. The same procedure can be applied to the transistor *Ref.*. At that time transistor *DUT* will be turned off and the gate of transistor *Ref.* will be connected to the DAC to be swept. The ADC measures the voltage at the same point. The V_{th0} of the *Ref.* can be obtained in the same manner as for transistor *DUT*. After the V_{th0} of both transistor *DUT* and *Ref.* are measured, the transistor *DUT* is connected to the stress voltage (for example, to the ground in Fig. 1). The transistor *Ref.* is turned off to

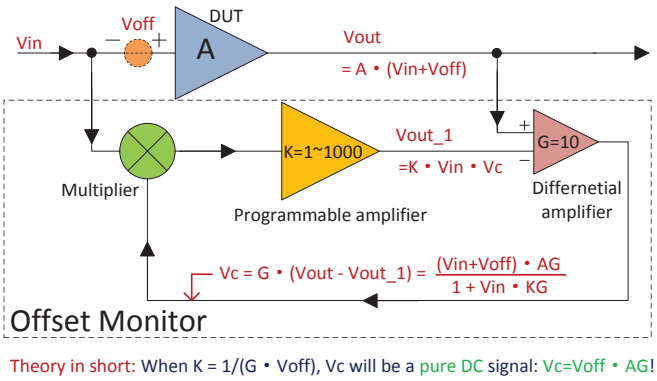

Fig. 2. Block diagram for the EI which measures the offset and gain of DUT OpAmp. [8]

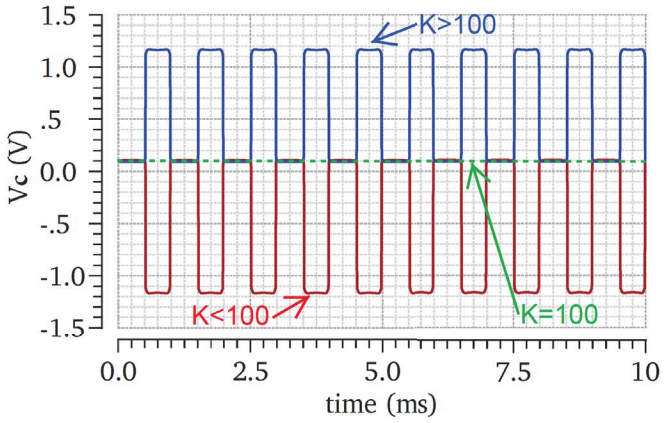

Fig. 3. The simulation for V_c vs. time under two adjacent programmable K values. [8]

remove any stress and hence remains fresh. The stresses will be periodically stopped and measurements will be done for threshold-voltages of transistor *DUT* and *Ref.*.

III. The Embedded Instrument for Offsets and Gains of OpAmps

The offset and gain of an OpAmp can be measured by the EI shown in Fig. 2 [8]. The input and output of the DUT OpAmp are both connected to the EI. The output of the DUT is compared with the signal from a gain-controlled amplifier. This amplifier has the same input as the DUT Opamp. Its gain is controlled by both the digital programmed number K and the compared result V_c. The analogue multiplier in Fig. 2 is introduced to realize such gain control mechanism.

From Fig. 2, one can derive V_c as (9).

$$V_c = \frac{(V_{in} + V_{off}) \cdot AG}{1 + V_{in} \cdot KG} \tag{9}$$

In (9), V_{in} is the original input signal of the DUT. V_{off} is the DUT input offset voltage. A is the gain of the DUT. G and K are gains of the comparison gain stage and the digitally programmable amplifier in the EI respectively. With different program settings, K can be changed from 1 to 1000. V_c is the output signal from the comparison gain stage. All these symbols are shown in Fig. 2 on their respective locations.

As shown by (9), V_c depends on the input signal V_{in} and K settings. Mathematically, the V_c could be driven to infinity if the denominator of (9) gets close to zero with the variation of input signal V_{in}. However, there is a special K setting for which V_c is independent on V_{in}. This special K value can be expressed in (10).

$$K_{spc} = \frac{1}{V_{off} \cdot G} \tag{10}$$

If the value of K_{spc} is known, the DUT offset voltage can be calculated from (10) as well as the value of G which is a fixed design parameter.

Fortunately, K_{spc} is not difficult to find. For example, if the input signal V_{in} is a sine wave, the K_{spc} can be found by sweeping the gain of the programmable OpAmp K. Arround the value of K_{spc}, the V_c signal will change dramatically from the blue line to the red line in Fig. 3.

However, every component inside the monitor has resident offsets. Reliability effects will also introduce extra offsets during the lifetime. So in reality, the offset being measured by the above method is a combination of all components' offsets based on some equations [8]. By doing several measurements with different configuration inside the EI, the DUT offset and other components' offsets, as well as the gain of the DUT can all be calculated by solving equations. The detailed information on resident offsets cancellation can be found in [8].

IV. Simulations and Measurements

A. Measurement results for the V_{th0} EI in 90nm

A long-time stress test on 90nm has been carried out. The test chip is put into an oven and is heated up to 127°C. The test chip contains 32 PMOS DUT transistors and supplied by a 1.15V power supply during the stress test. Measurements include two phases. The first is measuring the DUT drain current in moderate accuracy ($0.1\mu A$) with V_g and V_d sweeping from supply down to ground. The second phase is measuring the DUT drain current more accurately (around $1nA$) in the sub-threshold regime. For the same DUT transistor, these two kinds of tests are carried out at the same time (with only $20ms$ time difference, 0.000003% of the stress time) to avoid a recovery effect, and make sure that the V_{th0} extracted from both measurements should come from the same physical value.

The V_{th0} is extracted in three ways. First, all results of the drain current are measured at moderate accuracy which are used to fit the MOS model and extract the V_{th0}. The V_{th0} extracted in this way is referred to as "V_{th0} by the model" and can be used to validate the model accuracy. Second, select one pair of I_d and V_d for each set of V_g sweeping measured at moderate accuracy. The selected sub-group results are used to fit the MOS model and obtain the V_{th0}. The selection of I_d and V_d is based on $I_d = R_{load} \cdot V_d$, in which R_{load} is the load resistor as shown in Fig. 1. By this method, we imitate the measurement results of the V_{th0} EI test method which is proposed in Section II, and can validate the V_{th0} EI by various of R_{load} values. The V_{th0} extracted in this way is named as "V_{th0} by the EI". Finally, from the measured higher accuracy drain current in the sub-threshold regime, the real V_{th0} is

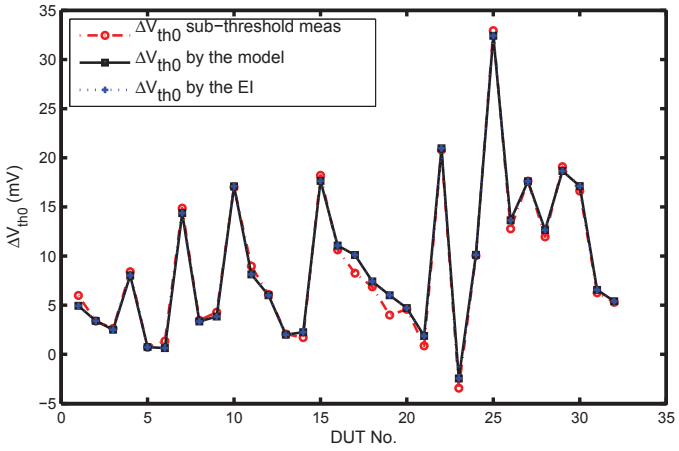

Fig. 4. After stress for 167 hours, comparing the measured V_{th0} change with the EI and another two methods in 90nm PMOS DUT transistors.

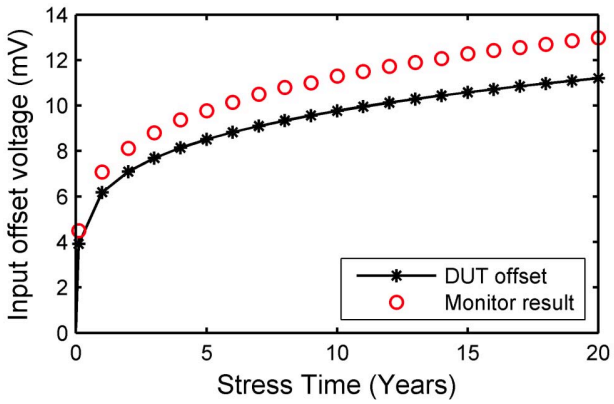

Fig. 5. DUT Opamp offset (mean value) increase with time due to reliability effects. The EI measurement results is shown as well. The DUT Opamp is stressed at normal supply 1.2V and 125C.

calculated and named as "V_{th0} sub-threshold measurement".

The change of threshold-voltage, ΔV_{th0} due to reliability effects is plotted in Fig. 4. The figure shows the ΔV_{th0} by the three methods of the same group DUTs after 1 week (167 hours) stress at 127°C. The "ΔV_{th0} by model" and "ΔV_{th0} by on-chip method" agree well. The maximum error between "ΔV_{th0} sub-threshold measurement" and the other two ΔV_{th0} methods is around $3mV$.

B. Simulation results for the OpAmp EI in 65nm

The proposed OpAmp EI which is shown in Section III is designed in TSMC 65nm low-power (LP) digital CMOS technology. It is a full differential system. The programmable amplifier is 10 bits and K is programmable from 1 to 1000. The digital programmability is realized by two "$R-2R$" resistor ladders. The comparison gain stage is realized via a subtractive circuit together with a gain G equal to 10.

The EI circuit has been simulated in Cadence Spectre with the help of RelXpert for reliability simulations. An full differential gain-boosted Opamp [2] is engaged as the DUT Opamp with a negative feedback loop and the close-loop gain is equal to 5. The input signal of the DUT is assumed to be a 1KHz sine wave with 20mV amplitude.

Due to reliability effects, the mean value of the DUT offset will degrade in time, which is shown in Fig. 5. The aged DUT offset is shown by black stars, and the EI measurement result in the corresponding time is marked as red circles. The EI result follows the DUT offset well and the error is around 10%. Therefore, the proposed OpAmp EI can be used as a dependability monitor for the DUT Opamp.

V. Conclusions

Two embedded instruments for dependability applications are treated. One is the EI for measuring threshold-voltages of MOSFETs. The other is the EI for measuring OpAmp offsets and gains. The threshold-voltage EI employs a new closed-form model for nanometre MOS transistor drain current to facilitate the threshold-voltage extraction. Measurements have been carried out in 90nm CMOS technology. Long-time stress tests show that the EI can characterize V_{th0} shift with 3mV accuracy. The EI using this new model can tolerate less accurate measurement results from the strong-inversion regime, which can be obtained by already existing general-purpose ADCs inside SoCs. The OpAmp EI for offset and gain measurement is designed based on a new theory. This EI can self-calibrate its resident offsets in the digital domain after measurement. The monitor has been designed in TSMC 65nm LP digital CMOS process. The simulation results show that the EI measured OpAmp offset changing with time is within 10% accuracy of the real ones. These two EIs can be used in analogue/mixed-signal IPs to help them to improve dependability.

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