

A CMOS CLASS-AB TRANSCONDUCTANCE AMPLIFIER FOR SWITCHED-CAPACITOR APPLICATIONS

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I. Abstract

A novel CMOS operational transconductance amplifier (OTA) is presented, using a fully differential single-stage core OTA as input stage and a differential to single current converter as output stage, each biased at a separate current level.

A large gain-bandwidth (GBW) product (2.7 MHz) and a high slew-rate (5 V/ μ s) can be obtained by applying a large bias current to the core OTA. Due to the class-AB operation of the output stage, a high output impedance can be obtained by applying a small bias current to the output stage, resulting in a high DC-gain (61.6 dB). The performance of this class-AB OTA will be compared with that of the basic single-stage OTA.

II. Introduction

The most suited amplifier for switched-capacitor circuits is the OTA, since the amplifier has to drive capacitive loads only. For a fast and complete charge transfer (settling) in these circuits, the amplifier has to meet three requirements [1]:

- a high slew-rate,
- a large bandwidth,
- a high open-loop DC-gain.

The high slew-rate and large bandwidth are necessary to obtain a fast settling response within the available time period. Particularly the DC-gain determines the maximum settling accuracy and is therefore of crucial importance in the final part of the settling period.

Figure 1 shows the basic single-stage OTA, with both input and output devices biased at the same current level.

Assuming strong inversion operation for all MOS devices [2], the GBW-product (which is equal to the transconductance of the input devices divided by the load capacitance) will be proportional to the square root of the bias current. The slew-rate is equal to the ratio of the maximum output current and the load capacitance and is therefore proportional to the bias current. The first two requirements can thus be met by applying a large bias current.

A high DC-gain, the product of the transconductance of the input stage and the parallel impedance of the output devices, will not be obtained since the output impedance of the amplifier is inversely proportional to the bias current.

One solution to boost the DC-gain is to increase the parallel output impedance by cascoding of the output devices. The major disadvantage of this solution is the limitation of the maximum output voltage swing.

Another method is the use of dynamic biasing techniques [2]-[4], in which a time variable bias current is used. At the beginning of the settling period a large bias current is applied to the input stage, resulting in a fast start of the response. At the end of the settling period, a high output impedance is obtained by applying a very low bias current. The major drawback of this approach is that both input and output devices are biased at the same current level. Although the output impedance increases during the settling period, the transconductance of the input stage decreases.

This paper proposes a novel class-AB OTA which circumvents the latter drawback. The amplifier consists of a fully differential single-stage OTA, biased at a high current level and a differential to single output stage, biased at a low current level.

Due to the class-AB operation of the output stage of the new OTA, the output current of this amplifier is not limited by the low current level of the output stage and is therefore equal to the output current of the differential implementation of the basic single-stage OTA of figure 1, assuming equal tail current biasing for both circuits.

For this reason, both designs will have equal transconductances.

The small-signal output impedance of the class-AB OTA is just determined by the low bias current of the output stage and will therefore lead to a significant increase of the DC-gain, with respect to the basic single-stage design.

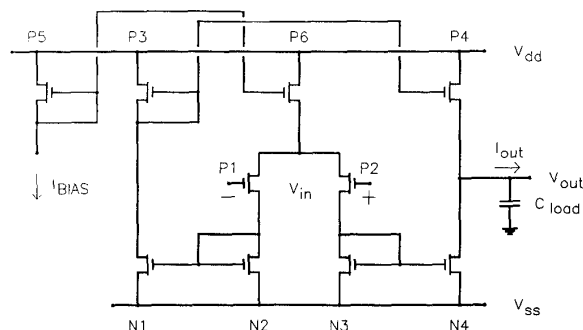


Fig. 1. The basic single-stage OTA.

III. Description of the class-AB OTA

The operational transconductance amplifier is shown in figure 2. The core amplifier within the dotted area is a fully differential version of the basic single-stage amplifier of figure 1, with a positive output node 1 and a negative output node 2.

In order to compare the performances of the class-AB OTA and the basic OTA, the dimensions of the input and output devices of both circuits are chosen equal and all current mirror ratios are set to one. Furthermore, the core amplifier and the single-stage amplifier are biased at the same current level.

The DC output current I_{out} of the offset-free single-stage amplifier (fig. 1) as a function of the input voltage V_n , normalised on the DC bias voltage of the input devices ($V_n = V_{in}/(V_{gs} - V_T)_{bias}$), can be written as the difference of the currents of the PMOS and NMOS output devices, resp. indicated by I_p and I_n

$$\begin{aligned} I_p &= I_{bias} \left[\frac{1}{2} + \frac{1}{2} V_n \sqrt{1 - V_n^2/4} \right], \\ I_n &= I_{bias} \left[\frac{1}{2} - \frac{1}{2} V_n \sqrt{1 - V_n^2/4} \right], \\ I_{out} &= I_{bias} V_n \sqrt{1 - V_n^2/4} \quad . \quad (1) \end{aligned}$$

Figure 3 shows these DC current transfer functions for the offset-free single-stage amplifier.

The current transfer functions of the class-AB amplifier (fig. 2), can be expressed as functions of the currents of eq. 1, assuming an offset-free core amplifier.

For positive input signals, the drain current of the diode device N9 will be equal to the output current I_{out} and N8 will be cut off.

For negative input signals, N9 will be cut off and the drain current of N8 will be $-I_{out}$. Depending on the sign of the input signal, the currents I_p and I_n of resp. the output devices P10 and N12, will either be equal to $I_B + I_{out}$ and I_B or I_B and $I_B - I_{out}$, as shown in figure 4 for $I_B = 0.1 I_{BIAS}$. The output current is only limited by I_{BIAS} .

Without affecting the slew-rate or the transconductance, the output devices can be biased at a low bias level I_B , resulting in a high small-signal output impedance.

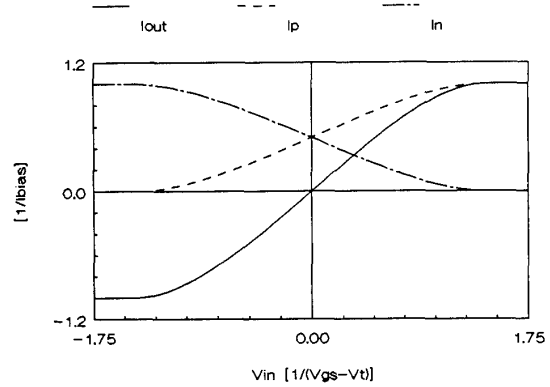


Fig. 3. Current transfer functions for the offset-free single-stage amplifier

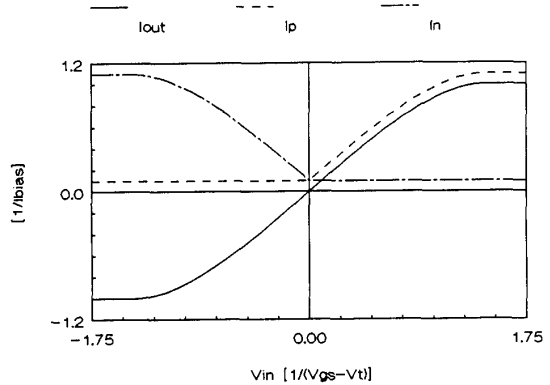


Fig. 4. Current transfer functions for the offset-free class-AB amplifier for $I_B = 0.1 I_{BIAS}$.

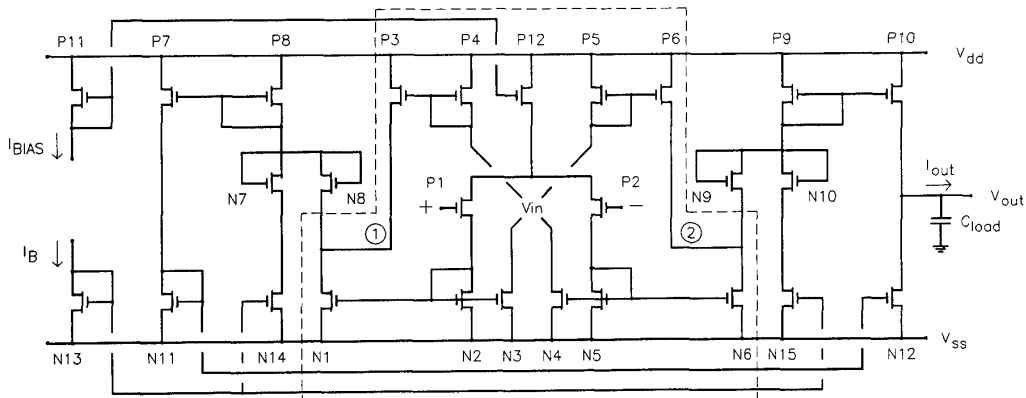


Figure 2. The class-AB amplifier

Due to the circuit symmetry, the systematic offset currents at the output nodes of the core amplifier will be equal in magnitude and sign. Since these offset currents originate from the finite output impedances of the current mirrors, they are both a function of the bias current and of the bias voltages at the output nodes, determined by the source voltages of the devices N8 and N9.

For a negative offset current I_{os} , the drain currents of the diode devices N8 and N9 show a positive offset. In this situation, both diode devices will be conducting for an input offset voltage range V_{os} , determined by the offset current I_{os} and the transconductance of the input devices. As a consequence, the transconductance is doubled in this input voltage range, but the current level of the output devices, determining the amplifier output impedance is also slightly increased. Figure 5 shows the current transfer functions for the situation $V_{os} = 0.25 (V_{gs} - V_T)$ and $I_B = 0.1 I_{BIAS}$.

For a positive offset current, flowing out the core amplifier output nodes, the diode devices N8 and N9 will not conduct for the input offset voltage range V_{os} as shown in figure 6.

In switched-capacitor applications, the amplifier is similarly used as in a unity gain configuration. At the end of the settling period, the differential input voltage of the amplifier is ideally zero. The use of a core amplifier with a positive offset current is therefore not allowed. For this reason, the core amplifier output nodes (impedances) are biased at a positive voltage in the realisation, creating a negative offset current.

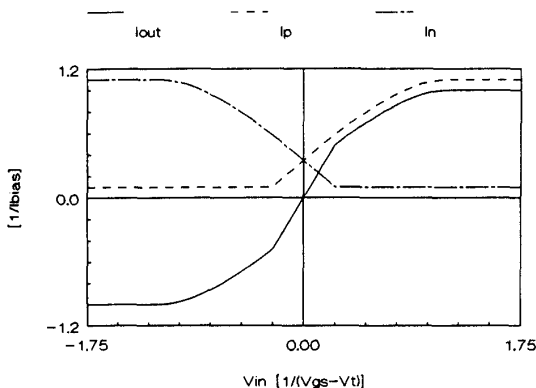


Fig. 5. Current transfer functions for the class-AB amplifier for a negative offset current of the core amplifier. ($V_{os} = 0.25 (V_{gs} - V_T)$, $I_B = 0.1 I_{BIAS}$)

Neglecting the influence of a small negative core amplifier offset current, it is shown that, under the given circuit constraints, the slew-rate and transconductances of the single-stage OTA and of the class-AB OTA are identical. The theoretical ratio between the output impedance and, using the previous assumptions, the DC-gain of the single-stage OTA and the class-AB OTA is equal to the inverse of the bias current ratio of their output devices resp. $I_{BIAS}/2$ and I_B .

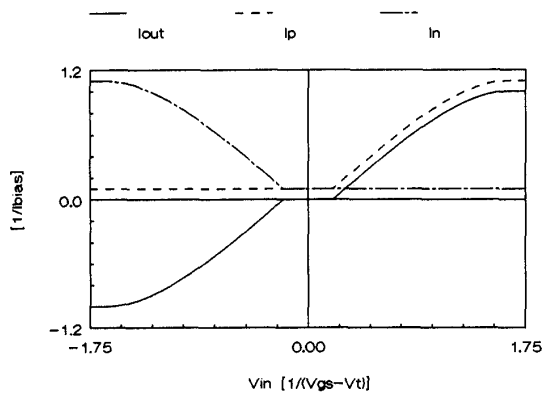


Fig. 6. Current transfer functions for the class-AB amplifier for a positive offset current of the core amplifier. ($V_{os} = 0.25 (V_{gs} - V_T)$, $I_B = 0.1 I_{BIAS}$)

If the current mirror ratios of the single-stage OTA are chosen larger than one, the transconductance is increased with the same ratio as the output impedance is decreased.

Due to the separate biasing of the core amplifier and the differential to single current converter output stage of the class-AB OTA, the transconductance of the amplifier can be increased by choosing the current mirror ratios in the core amplifier larger than one, without decreasing the output impedance of the output stage. Obviously, the impedances of the positive and negative output node of the core amplifier are affected by these current mirror ratios. In order to realise a core amplifier with a negative systematic offset current, the gates of the devices N8 and N9 can be connected to a reference voltage in stead of to their own drains.

The separate biasing of the core amplifier and the output stage has a positive influence on the PSRR and the systematic offset voltage of the complete class-AB amplifier. For low frequencies, the PSRR of the single-stage OTA can be approximated by

$$\begin{aligned} \text{PSRR}^+ &= g_{mP1}/(g_{ON1} + g_{OP4}), \\ \text{PSRR}^- &= g_{mP1}/(g_{ON1} - g_{ON4}), \end{aligned} \quad (2)$$

and the systematic offset voltage of this amplifier will increase with the bias current.

Due to the circuit symmetry of the class-AB amplifier, the transistors of the core amplifier will not contribute to the PSRR nor to the systematic offset voltage, if the output stage has an ideal performance. For low frequencies, the PSRR of the class-AB OTA can be approximated by

$$\begin{aligned} \text{PSRR}^+ &= g_{mP1}/(g_{OP10} - g_{OP7}), \\ \text{PSRR}^- &= g_{mP1}/(g_{ON12} + g_{OP7}). \end{aligned} \quad (3)$$

Both the PSRR and the systematic offset voltage will be fully determined by the output stage and will therefore only increase with the low bias current I_B . Compared to the single-stage OTA, the offset voltage of the class-AB OTA will approximately be decreased with the same factor as the DC-gain is increased.

IV. Experimental results

Both basic single-stage OTA and class-AB OTA are fabricated on a $3\mu\text{m}$ N-well CMOS masterchip by Philips Nijmegen, The Netherlands.

Figure 7 shows the DC-gain A_o of the class-AB OTA for a bias current of $100\mu\text{A}$ as a function of the applied current I_B . The output impedance of the amplifier is found to be not exactly inversely proportional to the current I_B , due to the internal drain offset current of the diode devices N8 and N9. As shown in section III, this offset current is a function of the output impedance of the core amplifier and therefore a function of the bias current.

The measured DC-gain of the basic OTA for a bias current of $100\mu\text{A}$ is 42.4 dB. Figure 7 shows that the DC-gain of the class-AB OTA is increased with respect to the basic OTA for a current I_B smaller than $50\mu\text{A}$, which is the bias current of the output devices of the basic OTA.

The measured output current transfer function is given in figure 8 and shows no nonconducting input voltage range, indicating a negative offset current of the core amplifier.

Table 1 gives measurement results for a current setting $I_{\text{BIAS}} = 100\mu\text{A}$ and $I_B = 2\mu\text{A}$.

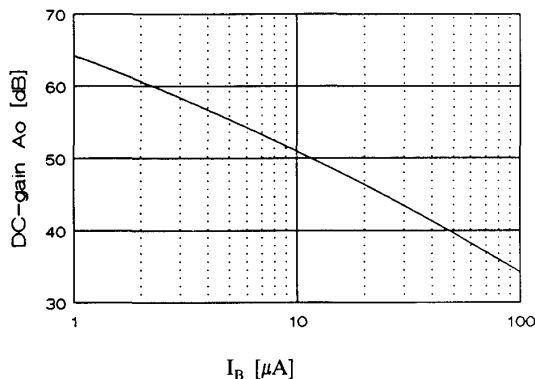


Figure 7. DC-gain A_o of the class-AB OTA as a function of I_B for a bias current of $100\mu\text{A}$ (A_o basic single-stage OTA = 42.4 dB).

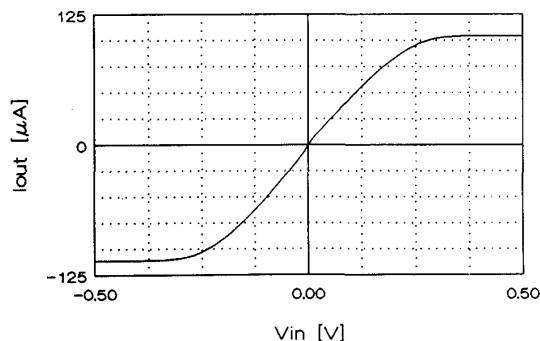


Figure 8. DC output current transfer function of the class-AB OTA for $I_{\text{BIAS}} = 100\mu\text{A}$, $I_B = 2\mu\text{A}$.

$I_{\text{BIAS}} = 100\mu\text{A}$, $I_B = 2\mu\text{A}$, $V_{\text{dd}} = -V_{\text{ss}} = 5\text{V}$, $C_{\text{load}} = 14\text{pF}$		
Performance parameter	Basic OTA	Class-AB OTA
DC-gain A_o [dB]	42.4	61.6
Unity-gain frequency [MHz]	2.7	2.7
Phase margin [deg]	76.0	58.0
Slew-rate+ [V/ μs]	5.1	4.9
Slew-rate- [V/ μs]	5.0	5.5
PSRR+ [dB] @ 100 Hz	38.7	67.7
PSRR- [dB] @ 100 Hz	48.6	51.9
Vos [mV]	21.0	2.2
Power dissipation [mW]	2.0	3.0

Table 1. Measurement results from both OTA designs.

V. Conclusions

A new class-AB operational transconductance amplifier is presented, combining a large bandwidth and a high slew-rate with a high DC-gain.

The amplifier consists of a fully differential single-stage core OTA as input stage and a differential to single current converter as output stage, each biased at a separate current level. Compared to the single-stage OTA, the output impedance of the class-AB OTA is increased without limiting the bandwidth or slew-rate.

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VII. References

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