Comparator Design Automation in SEAS

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Abstract

This article describes the development and realization of a synthesis program for CMOS *comparators. It was constructed following the* SEAS *framework for analog circuit design automation.*
Using this program, a number of comparators were synthesized, and tested using SPICE *simulations. All comparators generated performed well above their design specifications. This shows, that the* SEAS *concept is also applicable to the synthesis of non-linear circuits.*

1 Introduction.

Interest in the automation of the design of analog circuits has increased tremendously over the last few years. Analog design is still regarded as more a form of art than as an engineering discipline. Even for simple designs such as operational amplifiers and comparators a design time of over a months is still acceptable. This explains the research for tools that can aid the analog designer, thus making it possible to reduce the design time, effectively reducing the design costs.

Beginning 1987, a number of papers have appeared in electronics engineering literature, describing automated analog circuit design systems [1,2,3,4]. Most of these design systems are using OpAmps as a testcase[1]. The operational amplifier is a widely used circuit, and it behaves rather nicely: one can consider it as a completely linear circuit. However, in the field of analog design, the parts that take the longest time to develop, are the non-linear circuits. Among these circuits there are commonly used types such as analog multipliers and comparators. Analysis of this kind of circuits is difficult and time-consuming, so automation can improve a great deal over manual design. If an analog circuit design system is capable of synthesizing non-linear circuits, it can be considered to be more flexible in handling different circuit types than a system that lacks this possibility.

At the Electrical Engineering department of the University of Twente, the SEAS framework for analog circuit synthesis was developed [4]. To show that SEAS is suitable as a general synthesis tool that can handle linear as well as non-linear circuits, a comparator designer was implemented within this framework.

First, the SEAS framework will be discussed. After this, the selected design style is presented. This style is taken from various literature sources. An example of modelling and synthesis will be shown. Then some synthesized comparators are presented, together with some testing to confirm the validity of the internal models. Last, conclusions are drawn and the current state of the research on this subject is revealed.

2 The SEAS Framework.

The SEAS framework is can be subdivided into seven separate parts (see Figure 1):

- The System Expert: a part that takes care of communication with the outside world. Here the input files are processed and the output files are created.
- The Design Equation Database, where all design knowledge is kept. It consists of procedures that calculate the size of the transistors from the independent variables of the design and then gives the estimated performance of the circuit based on these transistors.
- The Initializer, that uses knowledge from the technology and specifications files, together with design style knowledge, to span the search space for the optimization procedure. The search

[1] In the OASYS system [1], also a comparator design automaton is implemented. However, it uses a more limited design style in comparison with this program.

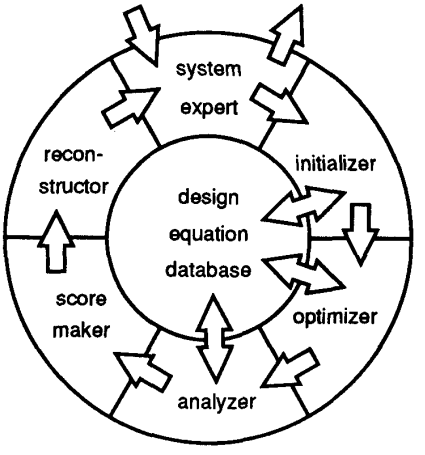

Figure 1: The SEAS Framework organization.

space is limited by physical limits, as well as limits posed by engineering knowledge.

- The Optimizer, where the design is optimized using the Simulated Annealing global optimization method.
- The Analyzer is a tool that analyzes the estimated behaviour of the designed comparator and compares this with the behaviour specified and expected by the user.
- The Score-Maker. If a comparator does not comply with the specifications, the fault in the design will have to be found. Now the faulty part of the comparator can be replaced by another, and be optimized for this part, too. To find out which part should be replaced, specific engineering expertise is present in the form of a scoring mechanism.
- The Reconstructor uses the fault analysis of the Score-Maker to replace the underscoring part.

Optimization is accomplished using the Simulated Annealing algorithm. This method is capable of finding the global optimum under certain conditions. Because the simulated annealing algorithm does not use derivatives of the design equations to move towards the optimum state, it is not necessary for the design equations to be differentiable, nor do they need to be continuous. Therefore, the full design equations can be used, not necessary the linearized ones.

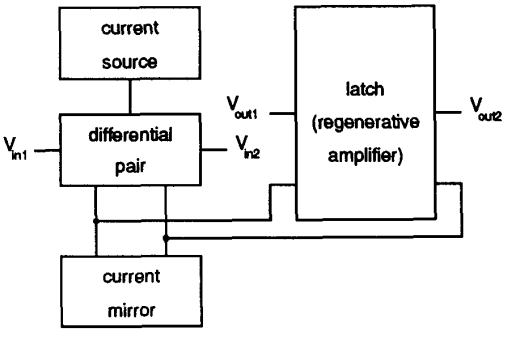

Figure 2: The block decomposition of the comparator design style.

3 The Comparator Design Style.

Not every comparator design style can be synthesized by SEAS in an efficient way. The system relies on the hierarchical decomposition of the design style to make an effective design. For the test case, a design style was chosen had to satisfy the following criteria: hierarchical in construction; a good comparison with designs in recent publications; and small, because it was primarily meant to be a testcase for non-linear design, not for state-of-the-art performance. However, the chosen design-style is still performing good, because a recent design is used.

Because the simulated evolution mechanism needed to be tested, for each subblock in the design hierarchy at least one alternative is available. Therefore, two designs have been integrated into one design style. This was possible due to the surprising similarity between the two published designs. The first is a design from Yukawa [5], that uses a differential amplifier at the input of a latch circuit. The second source is the comparator design style used in the OASYS design system [1]. Using the latter style, a direct comparison between the performance of the OASYS synthesized comparator and the one generated by the SEAS based designer, is possible. The block-decomposition of the chosen design style is shown in Figure 2.

4 The Implementation.

For each specification that can be specified by the user of the design system, a design equation is available. Again, these design equations are functions of

the sizes of the individual transistors in the circuit. These transistor sizes are also determined during the synthesis process. To determine the transistor sizes, the program uses "independent variables", i.e. currents and voltages inside the circuit that are independent of any outside factors nd of each other. As an example, the determination of the Slew Rate is discussed:

The Slew Rate can be determined easily by:

$$SR = \frac{I_0}{g_{m\ in}} \cdot \omega_{dom.} \qquad (1)$$

where I_0 the tail current of the differential input stage, g_m the transconductance of the input transistors, and $\omega_{dom.}$ the dominant pole of the input stage. The tail current is an independent variable, the transconductance is only dependent of the transistor size of the input transistor. However, the position of the dominant pole is dependent on the configuration of the differential pair subblock. For the simple pair, the characteristic equation is:

$$(1 + s\tau_{dp})(1 + s\tau_{cm})$$

where $\tau_x = -c_{g\ x}/g_{m\ x}$.

Then $\tau_{dom.} = -1/\omega_{dom.}$ is given by:

$$\tau_{dom.} = \max(|\tau_{dp}|, |\tau_{cm}|)$$

while for the cascoded differential pair, the following applies (as found from a symbolic analysis [6]):

$$(1 + (1 + s\tau_{casc}) \cdot s\tau_{dp})(1 + s\tau_{cm})$$

In this case, $\omega_{dom.}$ is not determined easily. The roots of this equation are:

$$\tau_1 = \frac{\tau_{dp}}{2} \cdot \left(1 + \sqrt{1 - 4\frac{\tau_{casc}}{\tau_{dp}}}\right)$$

$$\tau_2 = \frac{\tau_{dp}}{2} \cdot \left(1 - \sqrt{1 - 4\frac{\tau_{casc}}{\tau_{dp}}}\right)$$

$$\tau_3 = \tau_{cm}$$

After filling in the values, that come from the transistor design equations and the independent variables, the dominant time-constant can be determined:

$$\tau_{dom.} = \max(|\tau_1|, |\tau_2|, |\tau_3|)$$

As a last step, the Slew Rate can be calculated using equation 1.

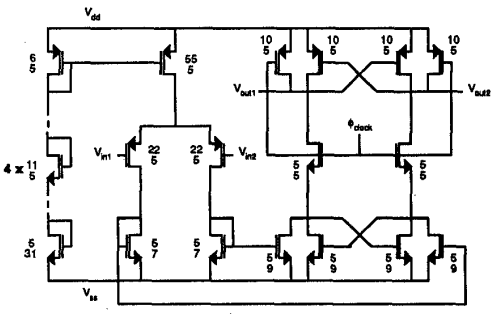

Figure 3: A SEAS designed comparator.

Parameter		Spec's	SEAS	SPICE
CMR^+	[V]	3.75	4.06	4.2
CMR^-	[V]	1.25	0.99	0.6
v_{offset}	[mV]	10.0	2.66	*n.a.*
$SlewRate$	[V/μs]	10.0	176	63
f_{clock}	[MHz]	10.0	58.6	$\approx$25.0
t_{prop}	[ns]	50.0	11.3	11.0
P_{DC}	[mW]	5.0	0.143	$\approx$0.15
$AreaUse$	[sq.]	250	56	*n.a.*

Table 1: Performances of the comparator of Figure 3, as specified externally, as predicted by SEAS, and from simulations with SPICE

5 The Results.

A circuit that was synthesized using the SEAS program for comparator design automation is depicted in Figure 3.

Using a circuit-simulator inputfile, generated automatically by the SEAS program, the results of the simulation are given in Table 1, as compared to the predictions made by the comparator designer. In Figure 4, a graphical representation of the *propagation delay time*, as calulated by SPICE, is given.

The predicted Slew Rate is too high. In the design equations, no parasitics were assumed. This turns out to be overly simplified. Neither the offset, nor the area use could be found with the SPICE simulation. The other parameters are close to their specifications, especially the propagation delay time, for which a complex model was developed.

The complete results of this research are published in the MSc. thesis of Kole [7].

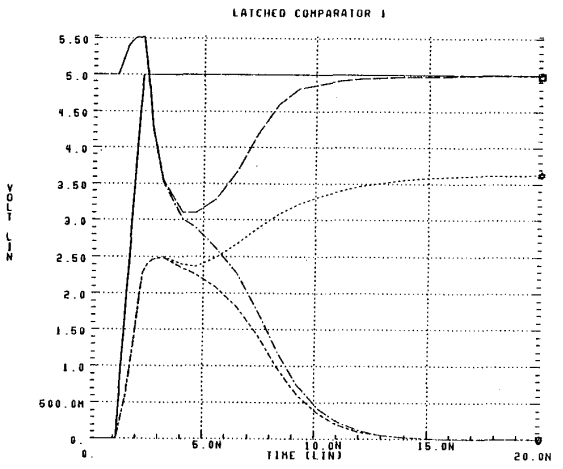

Figure 4: propagation delay of the comparator of Figure 3.

6 Conclusions.

Currently, the scoring mechanism is revised to move from the use of engineering knowledge towards a complete algorithmic approach. This is needed in those cases where little engineering knowledge is available, yet where automatic design is preferred over manual design. Few manual designs can accomplish design optimization at this small cost.

Also, we are working towards integrating general analysis tools for analog circuits, such as a symbolic analyzer, with the SEAS synthesis framework. Such an analog design environment should be able to boost the output of an analog designer tremendously.

References

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