Proceedings of The First Joint BMES/EMBS Conference **Serving Humanity, Advancing Technology** Oct. 13-16, '99, Atlanta, GA, USA

A GATE-ARRAY/MULTI-ELECTRODE DEVICE: CIRCUIT PERFORMANCE AND INTERFACING

Wim L.C. Rutten, Ed Droog, Mattias Rouw and Jos P.A. Smit
Institute for BioMedical Technology/ Faculty of Electrical Engineering
University of Twente, P.O.Box 217, 7500 AE Enschede, The Netherlands, rtn@el.utwente.nl

Abstract - The Twente 128-fold 3-dimensional multi-micro electrode device for endoneural stimulation is controlled by a 4x4 mm CMOS gate array chip. The chip contains the electronic circuitry, i.e. eight 16-channel multiplexers, eight double current sources and six differential amplifiers. Control of the gate array circuitry by a PC is done by a PCI interface. We present (aspects of) the design and realization of the PCI interface, as well as the simulated and measured performance figures of the current sources and amplifiers.

DESIGN SPECIFICATIONS

Data rate (clock frequency)
The Peripheral Communication Interconnect (PCI) controller enables to use high data rates, which are presumably needed to control the Gate Array (GA) circuits [1, 2]. Basically the GA has three registers: the CCR (16 bit shift Current Control Register), MCR (32-bit shift Multiplexer Control Register) and the TCR (32-bit Timer Counter Register). The specifications determine the clock frequency.
For endoneural electrical stimulation of nerve fibers a short cathodal pulse with a charge in the order of 1000 pC is needed. Cathodal 100 µs wide rectangular current pulses with amplitudes in the range 1 to 100 µA have proven to be sufficient for intrafascicular stimulation of motor nerve, from threshold of individual fibers to full recruitment. In a digital gate-array CMOS implementation of a programmable current source it is however advisable to fix current at 100 µA and vary pulse width between 1 and 100 µs, in principle this will have the same stimulation effect. Design and simulated switching behaviour of the current sources has been presented earlier, [2].
To perform twitch-force recruitment experiments , including tetanic force recruitment and fatigue behavior of motor-units, stimulus repetition rates of up to 200 Hz are needed.
In summary, both figures determine the minimally needed clock frequency of the gate array (GA): 1) a minimum electrode stimulus pulse duration of 1 µs 2) a maximum electrode stimulus rate of 200 Hz.
It is obvious that criterion 1) determines the minimal clock frequency needed. One can derive the following relation:

$f_{min} = CP * (P_{CCR} + 1) / T_{min}$, with

f_{min} = minimal clock frequency, CP= number of clock pulses for one period, P_{CCR} = number of periods needed to refresh CCR data, T_{min} = minimal stimulus pulse duration,
For CP=4, P_{CCR}= 16 and T_{min} = 1 µs, **f_{min} = 68 MHz.**

Current sources
The CMOS current source circuit has been presented in [2]. It has been realised as a double (biphasic) source, with the electrodes at half potential between Vdd (5V) and ground. The simulated switching behaviour over a load of 50 kOhm showed rectangular current pulse behaviour, with a maximal switching delay of 0.8 µs (load 50 kOhm).
Amplifiers
The amplifier must be able to record action potentials. Therefore, required bandwidth is 100 Hz-50 kHz, amplitude range 10 – 500 µV (i.e. output noise level preferably below 1 µVrms, for S/N ratio of 10, or 4.5 nV/ Hz ^{½}), gain around 40 dB, output impedance less than 1 kOhm, THD less than 1%. The amplifier is of a classical type, with a differential pair, a source follower output stage and the necessary bias circuitry, it has 10 CMOS FETs in total. Spice-simulation showed that the design amply met the specifications.

RESULTS

The **PCI** card included a Programmable Logic Device, programmed by the use of Altera software, and several circuits of the 74-series. The system functions correctly at a clock frequency of 64 MHz, very close to the specification.
Current source performance (mounted/interfaced chips): the maximal switching delay over a load of 10 kOhm (and rather long/high capacitance cables) was 3 µs. This is worse than specified, but will improve by another choice of cable.
Amplifier performance was as follows:
Test results, on-chip: (average of 7 chips), gain 41 dB, bandwidth: f_{-3dB} = 95 kHz; output impedance =3.8 kOhm; slew rate 0.3 V/µs.
Test results, when mounted and interfaced: gain 38 dB; bandwidth > 200 kHz; output impedance 4 kOhm; noise level 40 nV/Hz ^{½} ; slew rate 0.5 V/µs. The noise level is too high, but sufficient to record 10 µV action potential amplitudes with a signal-to-noise ratio of 2.

REFERENCES

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