Accurate automatic tuning circuit for bipolar integrated filters

Wim J.A. de Heij[1)], Klaas Hoen[1)] and Evert Seevinck[2)] (senior member IEEE)

1) University of Twente, Electrical Engineering Dept., IC-Technology and Electronics Group, P.O. Box 217, 7500 AE Enschede, The Netherlands.

2) Philips Research Laboratories, P.O. Box 80000, 5600 JA Eindhoven, The Netherlands.

Abstract

In this paper an accurate automatic tuning circuit, for tuning the cut-off frequency and Q-factor of high frequency bipolar filters, is presented. The circuit is based on a voltage controlled quadrature oscillator (VCO), is presented. The frequency and the RMS amplitude of the oscillator output signal are locked to the frequency and the RMS amplitude of a reference signal respectively. Special attention is paid to the actual Q-factor in the oscillator. Experimental results of a breadboard circuit operating from 136 to 317 kHz are presented. Eventually the circuit will be scaled up in frequency and integrated for on-chip tuning of bipolar video frequency filters.

Introduction

Bipolar technology has been used before to realize integrated continuous-time filters at video frequencies, operating from 5V supply [1],[2]. Modern Bi-CMOS processing [3] allows the combination of analog bipolar filters with digital circuits on a single chip. Bipolar analog filters may become even more attractive for this combination if the supply voltage, being dictated by the CMOS digital circuits, goes down to 3.3V in the future.

Recently a bipolar active-RC integrator (or transconductor-amplifier-C integrator) for video frequencies was presented [4]. In this integrator the high transconductance of the bipolar transistor was used effectively in the amplifier design. Furthermore, a simple tunable transconductor with good high-frequency properties and good linearity was designed for this integrator. Because of production tolerances and temperature dependence of integrated RC-products, automatic on-chip frequency tuning of filters is necessary to obtain the desired cutoff frequency. Especially at video frequencies we have to deal with a phase error (usually excess phase) of the integrator which must also be corrected by an automatic tuning circuit. Therefore the integrator circuit must have both tunable unity gain frequency and Q-factor.

The integrator circuit

Fig. 1 shows the concept of the balanced active-RC integrator [4]. To the left of the dashed line is a tunable transconductor, which is a parallel circuit of two fixed resistors $R_{1+}=R_{1-}=R_1$ and a variable active transconductance G_V. To the right is a transconductance amplifier (TA) with transconductance G_A with integration capacitors $C_{1+}=C_{1-}=C_1$ and variable resistors $R_{Q+}=R_{Q-}=R_Q$ in the feedback path. Output buffers drive the resistive load consisting of other transconductors. If the input and output resistance of the TA are assumed to be infinite, the following transfer function is found:

$$\frac{v_o}{v_i} = (1+R_1G_V) * \frac{G_A*(1-sC_1*(\frac{1}{G_A} - R_Q))}{sC_1*(1+G_AR_1)} \qquad (1)$$

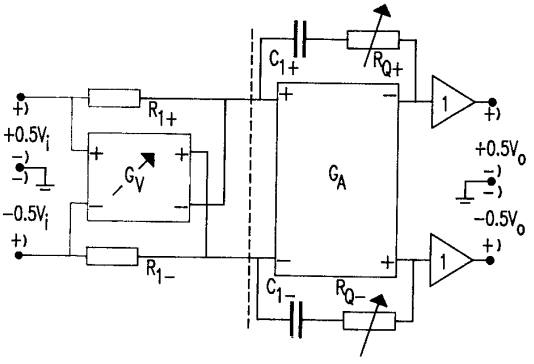

Fig. 1: Active-RC integrator concept.

The unity gain frequency f_o is tuned by G_V and phase is tuned by zero s_z, which is a function of the variable resistors R_Q:

$$f_o \approx \frac{1+G_VR_1}{2\pi R_1C_1} \qquad (\text{if } G_AR_1>>1) \qquad (2)$$

$$s_z = \frac{1}{C_1*(\frac{1}{G_A} - R_Q)} \qquad (3)$$

The circuit realization of the tunable transconductor shown in fig. 2 has the following transconductance:

$$G = \frac{1}{R_1} + G_V = \frac{1}{R_1} + \frac{I_1-I_2}{I_3} * \frac{1}{R_2 + \frac{1}{g_{m5,6}}} \qquad (4)$$

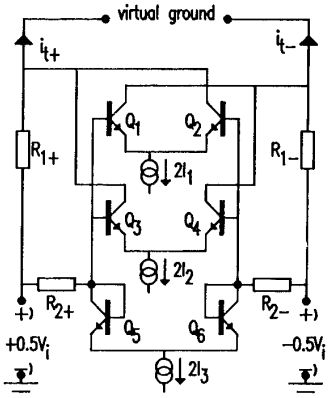

Fig. 2: Tunable transconductor circuit.

CH2868-8/90/0000-1159$1.00 © 1990 IEEE

The nominal design value is $1/R_1$. The second term describes the active variable part, which is a function of I_1-I_2. With the difference of I_1 and I_2, which are both positive currents, the total transconductance G can be tuned in both positive and negative direction.
Fig. 3 shows the circuit realization of the TA with feedback path and output buffers. The TA consists of differential pair (Q_1,Q_2), biased with $2I_S$. The diode connected transistors Q_3,Q_4 act as the variable resistors R_{Q+} and R_{Q-} in the feedback path. While the collector current through Q_1 and Q_2 is fixed to I_S, the collector current through Q_3 and Q_4 is adjusted to I_S-I_Q by the CMFB circuit Q_7-Q_{11} when the Q-tuning current I_Q is injected into the circuit via current mirror Q_{12}-Q_{14}. If $I_Q>0$ then $R_Q=1/g_{m3,4} > 1/G_A=1/g_{m1,2}$ and the zero is in the left half plane. In this way excess phase can be compensated for. Emitter followers Q_5 and Q_6 are used as output buffers. More details are given in [4].

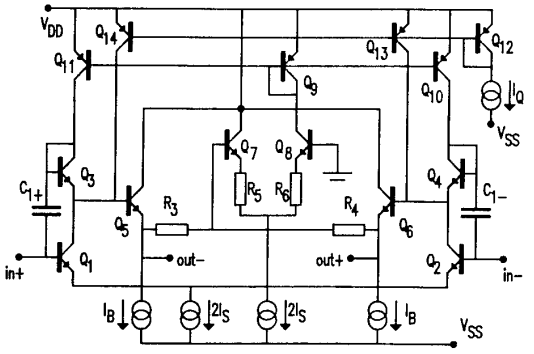

Fig. 3: Amplifier and feedback circuit.

The tuning circuit

Fig. 4 shows a block schematic of the complete tuning circuit. A quadrature oscillator, built as a two-integrator loop, is tuned in frequency and quality factor. From this tuning system control signals are derived which tune the cutoff frequency and Q-factor of the slave filter [5].

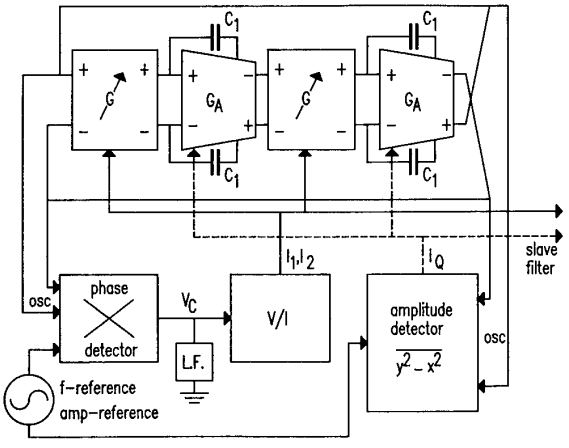

Fig. 4: Complete automatic tuning circuit.

The oscillation frequency f_{osc} is locked to the external reference frequency by the PLL. The multiplier, used as a phase detector, has a high output impedance resulting in a large voltage gain which makes a loop amplifier unnecessary. An emitter degenerated differential pair, used as V/I converter, converts the control voltage V_C into the tuning currents I_1 and I_2 which tune the variable transconductors. A passive RC loop filter (L.F.) at the high impedance node optimizes PLL performance.
In the amplitude detector the difference of the squares of the oscillator output signal and the reference signal is averaged and amplified to produce the DC Q-tuning current I_Q, which tunes the phase of the integrators. If the oscillator output signal is too large the current I_Q is increased, reducing the excess phase of the integrators and thus damping the oscillator. If the oscillator output signal is too small I_Q is decreased, increasing the excess phase of the integrators and thereby undamping the oscillator. The result will be that the RMS amplitude of the sine oscillator output signal is forced equal to the RMS amplitude of the reference signal, which may be a sine, square, triangle or other signal.

Phase detector and amplitude detector

Fig. 5 shows the Gilbert multiplier which is used as phase detector. The output currents are subtracted with an npn current mirror to avoid the β error of a pnp mirror, which would result in a large offset, and to obtain an output voltage around $(V_{DD}+V_{SS})/2$, which is also the bias potential of both inputs.

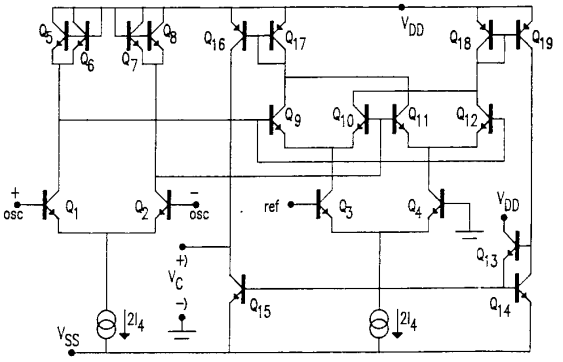

Fig. 5: Phase detector.

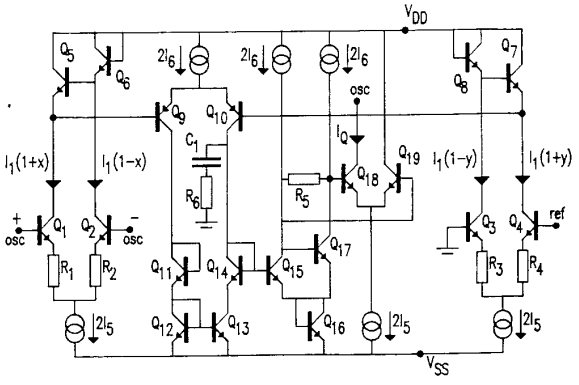

Fig. 6: Amplitude detector.

Fig. 6 shows the amplitude detector. The oscillator output signal and the reference signal are converted to currents $I_5(1+x)$,$I_5(1-x)$ and $I_5(1+y)$,$I_5(1-y)$ respectively by identical V/I-converters (Q_1,Q_2) and (Q_3,Q_4).

The translinear circuit Q_5-Q_{10} gives an output current which is proportional with the difference of the squares of modulation index x and y:

$$I_{out} = I_{c10} - I_{c9} = 2I_6 * \frac{x^2 - y^2}{2 - x^2 - y^2} \qquad (5)$$

Output current I_{out} is filtered by C_1. The DC component is amplified by the loop amplifier Q_{15}-Q_{19} to give I_Q. For DC and low frequencies Q_{15} is current driven so that I_{out} is amplified by β_{15}. Q_{15} is biased at $2I_6$ to cancel the error $2I_6/\beta$ of mirror Q_{12},Q_{13} and thus reduce the offset. Q_{17} acts as transimpedance amplifier with feedback resistor R_5. I_{C15} flows through R_5 and the voltage across R_5 is converted into I_Q by Q_{18} and Q_{19}. The total current gain is equal to $\beta_{15}R_5g_{m18}/2$, which was designed to be 350. Because of the high loop gain, the average value of I_{out} will be very small. It follows from (5) that the RMS-values of x and y will be equal, as required.
The current through Q_{16} is constant, so that the emitters of Q_{15} and Q_{17} are at virtual ground. The collector of Q_{10} is the only high impedance node in the amplitude detector, so that its frequency response is fully determined by the loop filter R_6,C_1.

Start-up conditions and accuracy

In the amplifier circuit shown in fig. 3 the current I_Q can only be positive and therefore the zero s_z can only be in the LHP or at infinity. As a result only excess phase can be compensated. If at f_{min} the excess phase is 0 for $I_Q=0$ the oscillator will only start up if reference frequency $f_{ref}>f_{min}$.
Besides $f_{ref}>f_{min}$ there is a second condition for correct start-up and convergence. If the oscillator does not oscillate, the control loops are in fact open. In such a situation the control signals V_C and I_Q should take on values which tune the oscillator to a frequency $f_{start}>f_{min}$ and undamp it. To achieve this the offsets in amplitude and phase detectors should be sufficiently small, which is the second condition.
Maximum Q-factor Q_{int} of the integrators is achieved at low oscillation amplitude. At low amplitude the active elements in the oscillator operate in a linear mode, so that the pole positions are not signal dependent. In case of steady oscillation at such low amplitudes, the Q-tuning current I_Q must have a value which puts the poles exactly on the jω-axis and I_Q should be practically independent of the amplitude, which is indeed experimentally verified.
For larger amplitudes the active elements do not operate fully linear and the pole positions become signal dependent, resulting in signal dependent damping. The relatively slow amplitude control can not correct this signal dependent damping and Q-tuning current I_Q will take on a value which puts the poles just off the jω-axis in the RHP for small output signal. In this case I_Q does not represent a correct pole position. Furthermore I_Q will decrease with increasing amplitude.
So to obtain high Q_{int} the oscillation amplitude must be chosen in a range where Q-tuning current I_Q is amplitude independent. Obviously harmonic distortion will be low at such amplitudes.
Compared with the tuning approach based on a voltage controlled filter (VCF) [6], this VCO tuning system has two advantages. First, correct start-up is easier to achieve, because oscillation is the only mode of operation for a VCO while a VCF can either perform as a filter or oscillator, the latter of which must be prevented. Second, the VCO tuning system does not critically depend on the accuracy of amplitude and phase detector, like the VCF system.
For both systems, matching between the integrators in the master VCO or VCF and the slave filter is the ultimate limit for accuracy.

Experimental results

The tuning circuit was breadboarded for low frequencies using bipolar transistor arrays from a standard 500 MHz technology.
The oscillator was built with $R_1=6.8k\Omega$ and $C_1=100pF$, resulting in a center frequency of 218kHz with $V_C=0$. Fig. 7 shows V_C and I_Q versus frequency for $R_2=4.64k\Omega$, $I_1+I_2=50\mu A$, $I_3=150\mu A$ (see fig. 2), the amplifier biased with $I_S=125\mu A$, $I_B=250\mu A$ (see fig. 3) and 5V total supply voltage. We find $f_{min}=136kHz$ and $f_{max}=317kHz$ which is a tuning range of -38% to +45% with respect to the center frequency. The pull-in range of the PLL is 136kHz to 288kHz (-38% to +32% tuning), which is sufficient in view of process tolerances and temperature dependence [3].

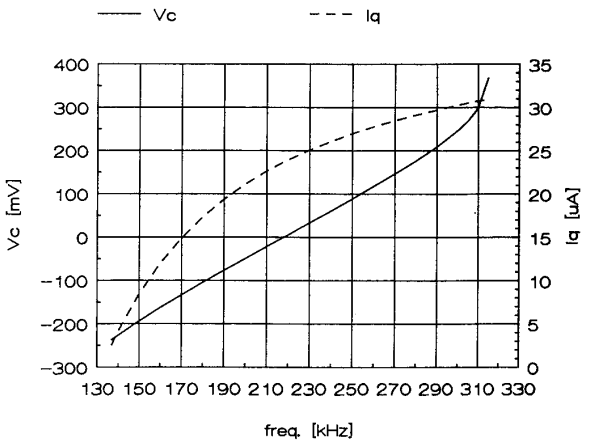

Fig. 7: V_C and I_Q versus frequency.

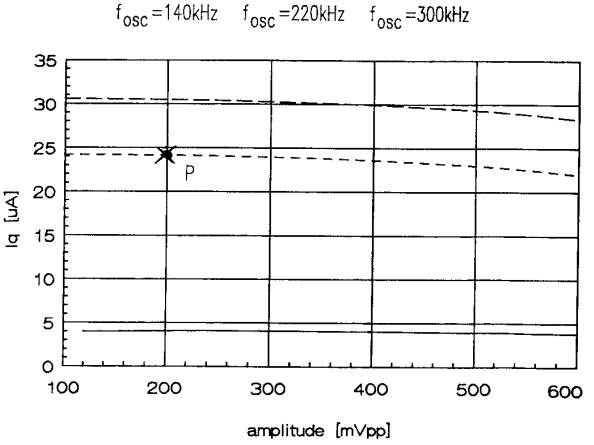

Fig. 8: I_Q versus oscillation amplitude.

Fig. 8 shows I_Q versus amplitude. We see that I_Q is practically independent of amplitude. As explained in the previous section this means that a very high Q_{int} is realized. At oscillation frequencies of 220 and 300kHz I_Q slightly decreases for amplitudes above $300mV_{pp}$, because of some damping by non-linearities.
Harmonic distortion should be low. Fig. 9 shows the output spectrum of the oscillator at a frequency of 220kHz and $200mV_{pp}$ amplitude (point P in fig. 8). The third harmonic is -43dB down (0.7% distortion). This distortion is mainly caused by the PLL. The same measurement with manual frequency control results in only 0.07% distortion.

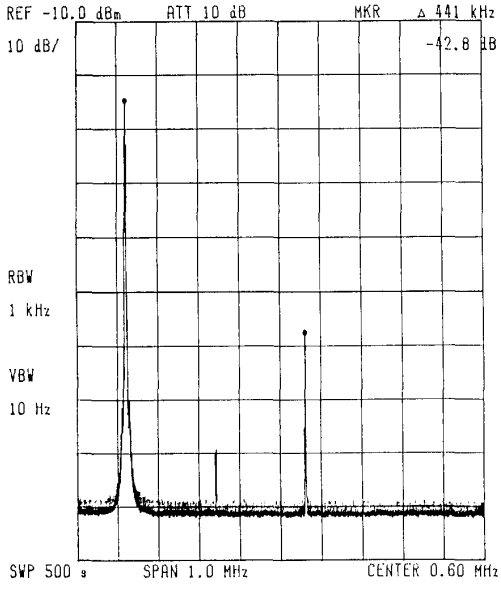

Fig. 9: Oscillator output spectrum.

The oscillator can be changed into a bandpass filter by capacitively coupling an input signal to the input nodes of the first TA in fig. 4, and taking the output signal from the output of the second TA. If the transfer function of this bandpass filter is measured, the oscillator Q-factor can be found from the magnitude response. For this measurement both control loops were opened and V_c and I_Q were manually set as close as possible to the values for point P in fig. 8. The transfer function of fig. 10 was measured with I_Q being only 1% larger than the closed loop value at point P, in order to damp the oscillator during measurement. Repeated measurements show oscillator Q-factors of 10000 or more. Because V_C and I_Q in this measurement are almost equal to the closed loop values in point P, it can be concluded that the tuning circuit yields very high integrator Q-factors.
Fig. 11 shows I_Q and the amplitude versus temperature. Reference was a $230mV_{pp}$ square wave, which theoretically would result in a $325mV_{pp}$ oscillation amplitude. The amplitude remains constant within 3% as temperature increases from 20°C to 100°C. I_Q increases because excess phase increases with temperature due to decreasing g_m of the transistors. Correct start-up and convergence of the tuning circuit was verified over this temperature range.

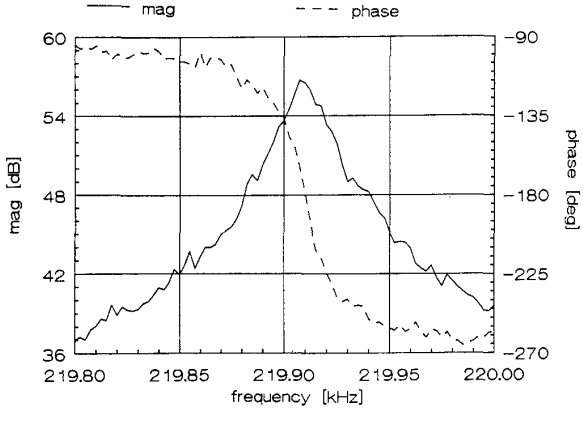

Fig. 10: Oscillator Q-factor measurement.

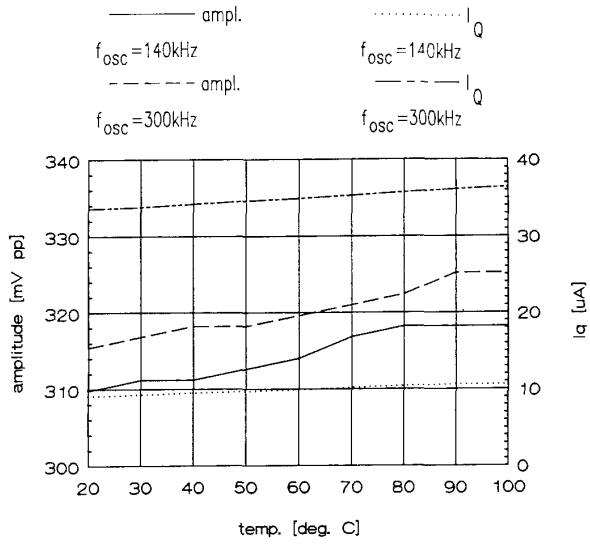

Fig. 11: Oscillation amplitude and I_Q versus temperature.

Conclusions

In this paper an automatic tuning circuit is presented for tuning both the unity-gain frequency and Q-factor of an integrator circuit for video frequencies [4] using a reference signal of arbitrary shape. Correct start-up and convergence are easily achieved. By means of a low frequency (136..317kHz) breadboard realization it is experimentally verified that very high integrator Q is achieved for oscillation amplitudes of $300mV_{pp}$ or less. Since Q is controlled via the oscillation amplitude, temperature stability of this amplitude is important. Experimentally the amplitude is found to vary only 3% for temperatures from 20°C up to 100°C. Correct start-up and convergence were verified over the same temperature range. The circuit will be scaled up in frequency and integrated in a 3 GHz Bi-CMOS process for video filter applications. The amplitude and phase detector have been simulated for video frequencies and correct operation of the integrator at video frequencies has already been verified with a test chip.

The authors wish to thank B. Nauta for fruitful discussions.

References

[1] S. Takagi, T. Anzai and T. Yanasigawa, "A Differential Input/Output Integrator Without PNP Transistors and its Application to Leapfrog Filter Synthesis", Proc. ISCAS 1988, pp. 2855-2858.
[2] H. Hagiwara et. al., "A Monolithic Video Frequency Filter Using NIC-Based Gyrators", IEEE J. Solid-State Circ., vol..23, pp 175..182, Feb. 1988.
[3] "BIMOS Design Manual", Internal publication of Philips Components, Nijmegen, the Netherlands.
[4] W.J.A. de Heij, E. Seevinck and K. Hoen, "Transconductor and Integrator Circuits for Integrated Bipolar Video Frequency Filters", Proc. ISCAS 1989, pp. 114..117.
[5] Y. Wang, F. Lu and A.A. Abidi, "A 12.5MHz CMOS Continuous-Time Bandpass Filter", Digest of technical papers, ISSCC 1989.
[6] C.F. Chiou and R. Schaumann,"Design and Performance of a Fully Integrated Bipolar 10.7-MHz Analog Bandpass Filter",IEEE J. Solid-State Circ., vol. SC-21 Feb. 1986, pp 6..14.