Technological aspects of gaseous pixel detectors fabrication

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***Abstract*—Integrated gaseous pixel detectors consisting of a metal punctured foil suspended in the order of 50µm over a pixel readout chip by means by SU-8 insulating pillars have been fabricated.**

SU-8 is used as sacrificial layer but metallization over uncrosslinked SU-8 presents adhesion and stress problems. In this paper we describe the several methods we have investigated to fabricate a metal layer on top of a partially crosslinked SU-8 film and the challenges we have encountered.

The fabrication process using wafer post processing has been proven, but in cases where single chip processing is desirable, edge bead is a major problem to overcome as it can cover a considerable chip area, reducing the detector performance; we show different techniques to reduce this edge bead and improve detection efficiency.

***Index Terms*— Integrated Micromegas; single chip processing; wafer post-processing.**

I. Introduction

Fabrication of integrated gaseous detectors [1,2] has reached a mature stage; this technology relies on the use of SU-8 negative photoresist [3] as both sacrificial and structural material [4] and the deposition of a punctured metal layer over the SU-8.

We would like design flexibility and we have investigated possibilities for thicker electrodes. Also the destructive discharges of the 500V applied on the top electrode is a problem (sparking), this would benefit from high melting point or spark-resistant materials, so research is being done in that direction.

The fabrication process has been successfully realized on 4" wafers and an inexpensive home made method has been used to perform single chip processing.

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II. Technological problems

For the construction of the 1µm thick punctured metal grid, aluminum sputtering was chosen as a first option, it shows good adhesion with SU-8 [5] and it is easy to deposit and pattern. Thicker aluminum films will be difficult due to the stress induced in the SU-8 layer beneath.

Other materials were deposited by sputtering in search of thicker electrodes with very different results.

Chromium and Titanium/Tungsten induced a lot of stress in the SU-8 layer and cracks in the metal appeared already after some hundred nanometers. On the other hand gold and titanium produced compressed layers with ripples, in both cases even metal peeled off the resist, showing poor adhesion, and it was not possible to perform lithographic process due to the roughness in the metal layer.

Silicon was sputtered on top of the SU-8. For layers thinner than ~300 nm a flat surface was obtained, while for thicker layers long cracks appeared in the silicon. Using a thin silicon film we could build a stack silicon/metal that is expected to bring a better performance in terms of protection against sparks [6,7] and increase the detector lifetime.

To produce thicker grids copper electroplating was successfully used, a 100 nm Al/Cu seed layer was deposited by sputtering and 4 µm Cu grid was electroplated, finally holes in the seed layer were opened by wet etching. The result can be seen in Fig. 1.

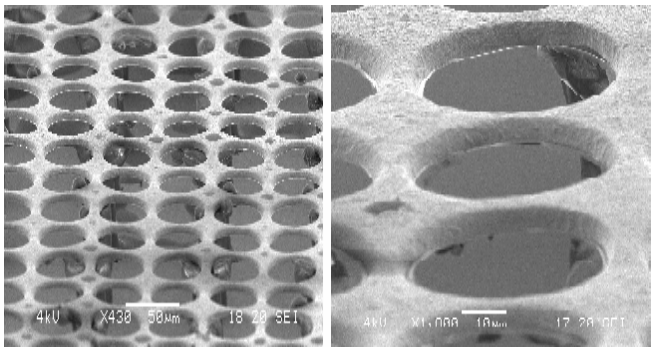

Fig. 1. 4-µm thick electroplated copper grid on SU-8.

Thicker grids made of copper, with a melting point higher than aluminum are thought to be more resistant against sparks because the grid will be more difficult to vaporize in the spot where the sparks is produced.

The main problem encountered during the deposition of the metal grid by sputtering was the crosslinking of the upper SU-8 layer because of the energy involved during the deposition (Fig. 2); some approaches found in the literature to solve this known problem are the use of thermal evaporation as a low energy deposition technique [4,8], the use of an embedded metal mask [9] or a light absorption layer [10].

As an alternative to sputtering thermal evaporation was tried for the fabrication of the electrode plane. However when a thick metal layer is needed, in the order of 1µm, even the energy involved during the evaporation is enough to crosslink the upper SU-8 layer.

The final solution consisted in spin coating standard Oir 907 positive photoresist on top of the SU-8, expose both resists at the same time and then sputter the metal layer. Later on this positive resist is easily removed in acetone.

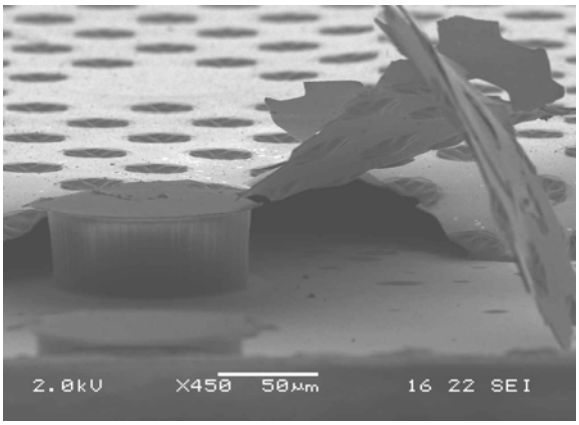

Fig 2. The aluminum grid shows thin skins in the holes. These are residues of SU-8, remaining through undesired cross-linking.

III. SINGLE CHIP PROCESSING

For our first prototyping experiments both single chip and wafer scale post processing were used. Photoresist spinning typically leads to a thicker layer at the wafer edge - the so-called *edge bead*. For wafer level processing edge bead does not present any complication during the rest of the processing, and no special steps are needed. However due to the limited availability of CMOS data processing chips Medipix2 or Timepix [11,12] sometimes single chip processing is needed. The chips have an active area of 14 mm x 14 mm so here the edge bead is on the active area of the chip. The resist homogeneity over the chip is insufficient, leading to an inhomogeneity of radiation detection across the device.

When spin coating SU-8 in a single chip the edge bead can be up to 50% thicker and it extends 4mm in the chip area (Fig. 3), this makes the device response not homogeneous. To overcome these problems some solutions were essayed.

In a first approach a fixed amount of SU-8 was deposited over the chip, and when heated it up its viscosity is reduced enough to use a scraper to spread it over the chip surface [13]. This solution reduces the edge bead, but the desired thickness was more difficult to control and to reproduce (Fig. 4).

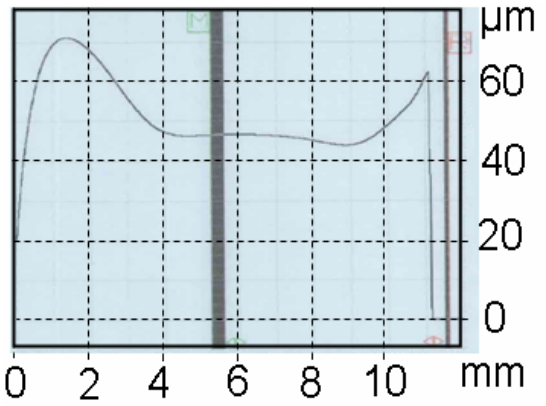

Fig. 3. SU-8 profile when using normal spin coating in a single chip.

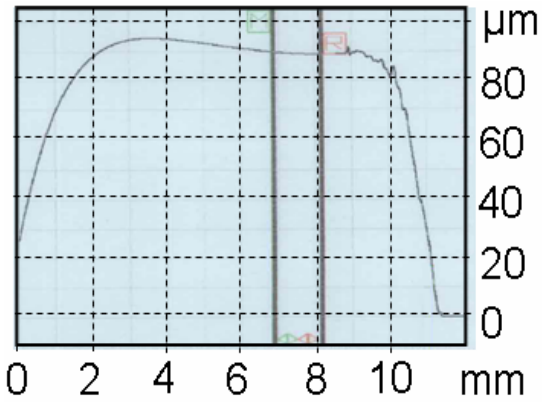

Fig . 4. SU-8 profile when scraping resist in a single chip.

Our final solution consisted in glueing the chip in the centre of a carrier wafer, and then glue dummy chips around this good chip. When spin coating SU-8 in this group of chips the resist profile in the good chip in the centre is very homogeneous (Fig. 5). In our application there was no need to dig a trench in the carrier wafer and place the chip leveled [14]. After spin coating the SU-8 a flat surface is obtained after a few minutes resting.

The rest of the process is performed with the chips on the carrier wafer, for convenience of handling. Finally the good chip is released by dicing the carrier wafer and separating the good chip from the dummy chips.

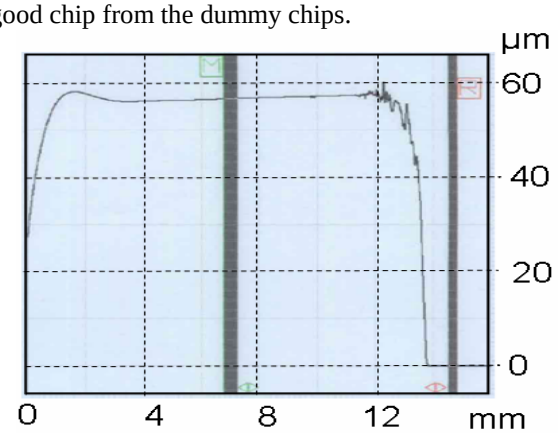

Fig. 5. SU-8 profile when spin coating in a chip glued to a carrier wafer and surrounded by dummy chips.

IV. RESULTS

For testing the post-processed chips, they were placed inside a sealed chamber flushed with a Helium/Isobutane (80/20) gas mixture and irradiated with ^{55}Fe, a commonly used radioactive source in this kind of detectors. Fig. 6 shows clouds of electrons produced by the ^{55}Fe conversions in the gas that are recorded by the chip.

The devices were irradiated for several hours and the image of all the ^{55}Fe conversions superimposed, the image shows a uniform response in all the chip area and no Moire effect [15] is present (figure 7), which is a commonly know problem for hybrid-assembled devices.

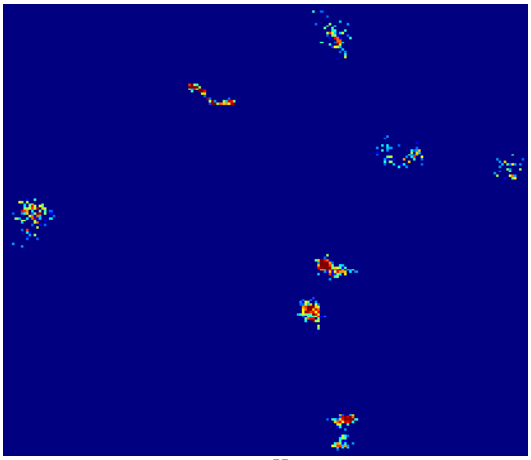

Fig. 6. Several clouds of ^{55}Fe conversions in the chip area.

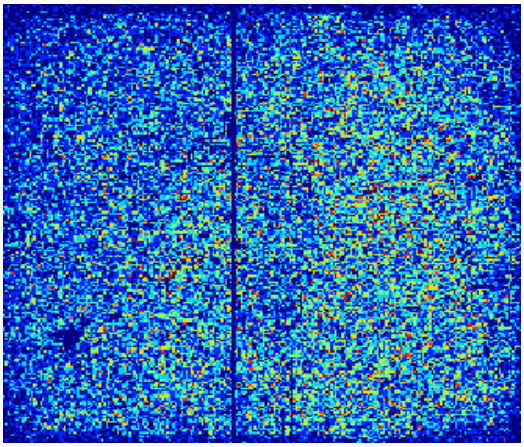

Fig 7. Image of the detector after being irradiated for several minutes with ^{55}Fe, homogeneous response as no Moiré effect is present.

V. CONCLUSIONS

Single chips were fabricated and tested under ^{55}Fe irradiation obtaining a very homogeneous response. Various materials and deposition techniques were essayed and new possibilities for the fabrication process were found which will bring a stronger and more resistant grid

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