Comparison of Gate Capacitance Extraction Methodologies

S. N. R. Kazmi and J. Schmitz

Abstract— **In recent years, many new capacitance-voltage measurement approaches have been presented in literature. New approaches became necessary with the rapidly increasing gate current density in newer CMOS generations. Here we present a simulation platform using Silvaco software, to describe the full chain from fabrication process until signal interpretation of an NMOS C-V test structure. The platform allows a verification of the validity of an assumed extraction procedure from high-frequency or RF C-V measurements.**

Index Terms— **C-V Measurement, Gate oxide, RF-CV, Device Simulations, Tunneling Current**

I. INTRODUCTION

DOWNSCALING the MOS transistor involves a reduction of the gate dielectric thickness [1]. When the dielectric material is kept the same, this reduction inevitably leads to an increase in the tunneling current through this dielectric. In present-day deep-submicron CMOS this dielectric tunneling current has become very significant, to a level that it influences the standby power of integrated circuits [2]. It also complicates (wafer-level) device measurements meant for technology assessment. In particular, charge pumping [3,4], the capacitance-voltage (C-V) measurement [5,6] and time dependent dielectric break down tests [7,8] are adversely affected by gate dielectric leakage.

For C-V measurements, recent literature reports of many approaches to deal with the gate leakage current. Most approaches use an elevated measurement frequency together with de-embedding approaches. Also, several equivalent circuits were reported to effectively describe the MOS capacitor under test, such as equivalent circuits using three, four or five lumped elements and a transmission line model [7,9,10]. The papers on the subject typically show a validation of a single methodology on a limited set of test devices only, while these devices are not always fully documented. Therefore a clear decision tree is missing when one needs to decide which test structure and capacitance extraction algorithm needs to be used.

To this purpose we set up a simulation chain, describing the MOS C-V test structure from process simulations and computing its response to electrical stimulus, by generating gate impedance or *S*-parameter data. With these simulated data, the capacitance extraction procedures can then be tested. In this paper the simulation approach is documented and first results shown.

II. RF-CV MEASUREMENTS

For a direct comparison of simulation results to published data, we go back our earlier work on RF-CV measurement [6,11]. The device in [6] was fabricated in a standard 0.12µm CMOS process flow and *S*-parameter measurements were carried out in a range of frequencies 0.1-10 GHz. SOLT calibration and open-short de-embedding were used.

A MOS transistor consists of a variety of resistive and capacitive components, as indicated in Figure 1 for accumulation. However, the device is designed in such a manner that a three-lumped-element equivalent circuit model (a capacitor with a series and a parallel resistance) describes it well up to ~4GHz.

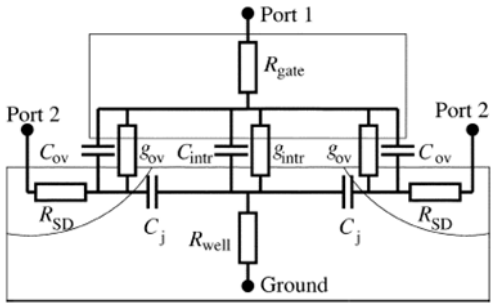

Fig. 1. Cross section of a capacitor (or transistor), with an approximated equivalent circuit in accumulation. All components in this diagram are bias dependent except R_{gate}, R_{SD} and R_{Well}. Figure reprinted from [11].

The key measurements in [6] are repeated here for convenience, in figure 2. The analysis of the *S*-parameters in this paper was carried out by (roughly) correcting the device characteristics for a fixed external resistance (mainly caused by R_{gate} in figure 1), then calculating *Y*-parameters from the *S*-parameters and taking the capacitance as $\mathrm{Im}(Y_{11})/\omega$. Also in

Manuscript received October 1, 2008. This work was supported in part by the Higher Education Commission (HEC), of Pakistan.

S.N.R. Kazmi is currently enrolled as a PhD candidate with MESA+ Institute of Nanotechnology, Faculty of Electrical Engineering, University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands e-mail: s.n.r.kazmi@utwente.nl).

J.Schmitz works at the University of Twente, 7500 AE Enschede, The Netherlands (e-mail: J.Schmitz@utwente.nl).

ref. [6] this approach was not fully documented which later led to some discussion in literature. Taking $C = \mathrm{Im}(Y_{11})/\omega$ from

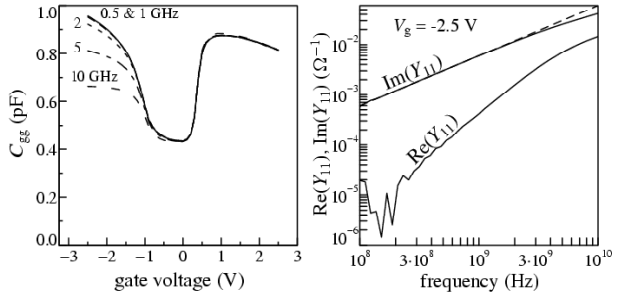

Fig. 2. (Left) Capacitance–voltage curve of a W/L = 384 µm/0.18 µm NMOS RF transistor as measured at various frequencies, after de-embedding. (Right) Real and imaginary parts of Y_{11} as a function of frequency at V_{gate}= -2.5 V. The dashed line shows the trend of a capacitor without series resistance. Figure reprinted from [6].

the device *Y*-parameters leads to a systematic error because the series resistance is neglected.

The decrease in the gate capacitance in accumulation mode observed in figure 2 for frequencies greater than 1 GHz and a downward bend of real part of Y_{11} is due to the fact that at high frequencies the external series well resistance R_{well} becomes significant limiting the response time of holes in the bulk. The capacitance in depletion around zero gate bias is still high, because of the considerable contribution of the gate/source and gate/drain overlaps in the measured device with submicron length. In inversion we see no frequency dependence, which is due to the optimized test structure design limiting the external resistance to be less than 1 Ω.

III. PROCESS FLOW OF MOS IN SILVACO

The block diagram for the electrical characterization of a semiconductor device using the process simulator ATHENA and device simulator ATLAS is shown in Fig.3 [12].

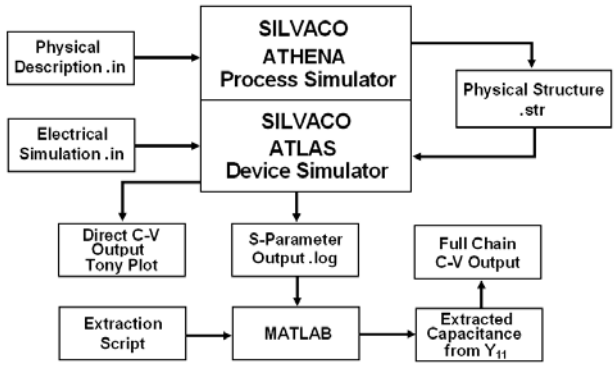

Fig. 3. Block diagram of flow in SILVACO.

The process flow of a simple MOS transistor using 0.18 µm technology is simulated in ATHENA with gate length 0.3 µm with a top bulk contact is shown in Fig. 4. This structure file is used in the device simulator ATLAS for small signal characterization of the MOS device for a range of frequencies at the gate terminal with shorted source and drain terminals. The tunnel current is not yet included in the characterization of the MOS transistor due to simulator limitations.

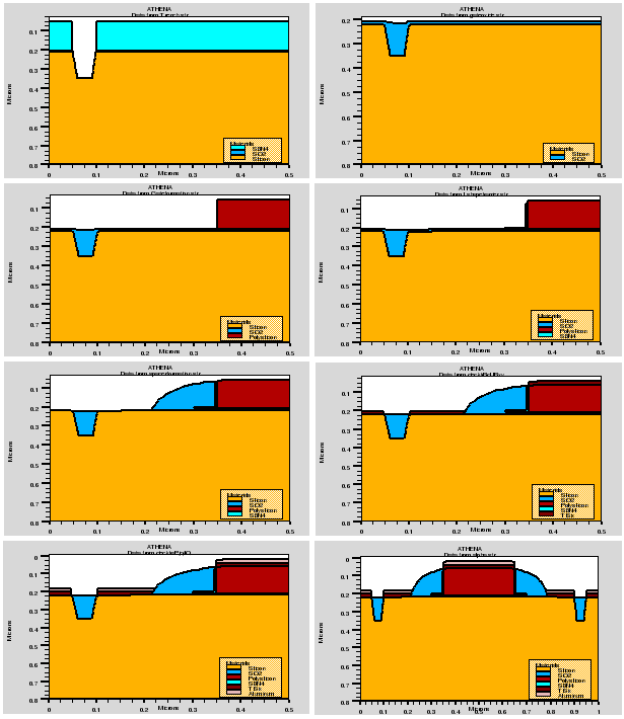

Fig. 4. MOS Transistor process flow in SILVACO.

IV. SIMULATION RESULTS

Fig. 5 shows C-V result directly obtained from the simulator generated output file, where the test frequency is varied in the same way as that for the RF-CV measurements in figure 2. However the curve in Fig. 6 represents the full chain of C-V extraction from the simulator generated *S*-parameters output file further translated into *Y*-parameters in MatLab and hence capacitance is extracted by $C_g = \mathrm{Im}(Y_{11}/\omega)$.

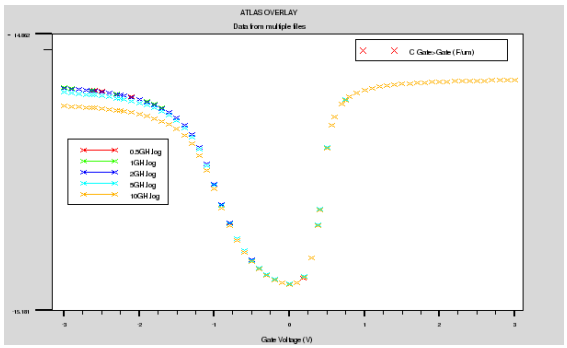

Fig. 5. Direct C-V Output at 0.5 GHz, 1 GHz, 2 GHz, 5 GHz, and 10 GHz.

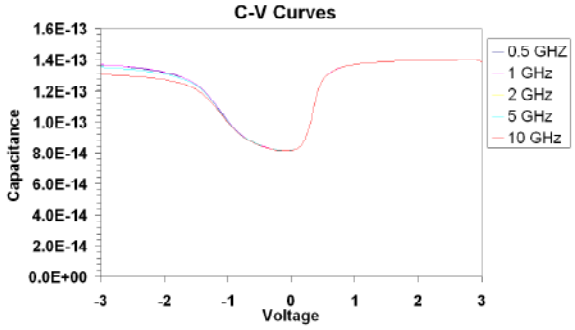

Fig. 6. Full Chain C-V Output at 0.5 GHz, 1 GHz, 2 GHz, 5 GHz, and 10 GHz.

The simulator reproduces the measured trend properly both with the direct and full chain C-V output, be it that the devices are not sufficiently matching to obtain a quantitative agreement. For instance, the gate depletion, observed in inversion in figure 2, is not seen here, indicating again that minor adjustments in the process simulation are still necessary. Further, a remarkable difference in the depletion region can be seen. The simulator indicates a much lower overlap capacitance than the data (as seen from a comparison between figures 2 and 5). This effect may be geometry-related and also deserves further attention.

V. CONCLUSIONS

In this paper a process and device simulator are employed to verify the validity of high-frequency C-V methodologies for MOS transistors. It presently offers the possibility to check capacitance calculations from S-parameters for various chosen test structure geometries. The future work would be extended to the comparison of the remaining gate capacitance extraction methods for C-V characterization of MOS transistor with varied channel length and well doping concentrations. Also the effect of the tunneling current through ultra thin gate oxide must still be incorporated in our simulations to study its impact on the C-V curve and its propagation into possible measurement errors.

ACKNOWLEDGMENT

The authors would like to thank J.L. van der Steen and R.J.E. Hueting for their support with the ATLAS device simulator.

REFERENCES

[1] J. R. Brews, W. Fochtner, E.H. Nicollian, S. M. Sze, “Generalized Guide for MOSFET Miniaturization” *IEEE Electron Device Lett.*, vol. 20, pp. 92–94, Feb. 1999.
[2] ITRS roadmap 2007, available: www.itrs.net.
[3] P. Masson, J.-L. Autran, and J. Brini, *IEEE ElectronDevice Lett.*, vol. 20, pp. 92–94, Feb. 1999.
[4] G. T. Sasse and J. Schmitz, IEEE Trans. El. Dev., March 2008.
[5] W. K. Henson, K. Z. Ahmed, E. M. Vogel, J. R. Hauser, J. J. Wortman, R. D. Venables, M. Xu, and D. Venables, IEEE Electron Device Lett., vol. 20, pp. 179–181, Apr. 1999.
[6] J. Schmitz, F.N. Cubaynes, R.J. Havens, R. de Kort, A.J. Scholten and L.F. Tiemeijer, IEEE El. Dev. Lett.., vol. 24, no 1, pp. 37-39, 2003.
[7] G. Ghibaudo et al., Micr. Rel. 39 (1999) 597.
[8] J. Schmitz, H. P. Tuinhout, H. J. Kretschmann, and P. H. Woerlee, *IEEE Trans. Device Mat. Rel.*, vol. 1, pp. 150–157, Sept. 2001.
[9] C.-H. Choi, J.-S. Goo, T.-Y. Oh, Z. Yu, R. W. Dutton, A. Bayoumi, M. Cao, P. Vande Voorde, D. Vook, and C. H. Diaz, IEEE Electron Device Lett., vol. 20, pp. 292–294, June 1999.
[10] D. W. Barlage, J. T. O’Keeffe, J. T. Kavalieros, M. M. Nguyen, and R. S. Chau, IEEE Electron Device Lett., vol. 21, pp. 454–456, Sept. 2000.
[11] J. Schmitz et al., IEEE Trans. Semicond. Manuf. Vol. 17 no. 2, pp. 150-154, 2004.
[12] E.W.M. van Luijk, “Comparison of RF C-V extraction methods using device simulations with focus on the influence of parasitics”, M.Sc Thesis, May 2006, Dept. Elect. Eng., Univ. of Twente, Enschede, The Netherlands.