Application of Functional I_{DDQ} Testing in a VLIW Processor towards Detection of Aging Degradation

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***Abstract*— In this paper, functional I_{DDQ} testing has been applied for a 90nm VLIW processor to effectively detect aging degradation. This technique can provide health data for reliability evaluation as used in e.g. prognostic software for lifetime prediction. The test environment for validation, implementing an accelerated test (AT), has been investigated and I_{DDQ} measurement data resulting from AT is presented. It is found that the quiescent current for the processor characterizes power degradation with a coefficient of 0.38 with the aging trend. This is in coherence with behaviour of the NBTI aging mechanism, but contradicting other mechanisms such as TDDB. It shows the NBTI aging is the dominant factor for processor technology of 90nm and beyond.**

***Keywords*—I_{DDQ} testing, NBTI, functional testing, reliability testing, DSP processor, aging, nanoelectronics**

I. INTRODUCTION

The most advanced technology nodes IC processors are expected to be less reliable due to aggressive manufacturing technology scaling and high system complexity. Key circuit and device parameters have been shown to change as chips age. For example, Negative-Bias-Temperature-Instability (NBTI), Hot-Carrier Injection (HCI) and Time-Dependent Dielectric Breakdown (TDDB) cause shifts in the threshold voltage V_{th}, leading to e.g. increased delay behaviour [1]. Quiescent power-supply current (I_{DDQ}) testing technology has been investigated in this paper with regard to its usage in aging-degradation monitoring.

I_{DDQ} testing has been typically developed to detect process-oriented physical defects, such as open and bridging faults. Test-vector generation for target DUTs (device under test) and a scan test are needed [2]. In the past a potential relationship has been made between I_{DDQ} tests and NBTI-related aging in (140nm node) SRAMs [3] as well as occurring leakage currents versus NBTI effects [4].

However, I_{DDQ} testing techniques are normally used to detect (potential) manufacturing defects. New possibilities for I_{DDQ} testing have to be investigated because in the case of the new generation of safety-critical systems, the reliability level has to be increased for final tests; in addition, also during the life-time usage a constant increase in terms of dependability is required by the market. Furthermore, for I_{DDQ} testing, a time-consuming current test is required, which is not suitable for large processors.

This paper deals with the enhancement of the reliability of a Very Large Instruction Word (VLIW) processor being used in high-level security (e.g. automotive and space) applications. In this research, functional I_{DDQ} tests are applied, in order to monitor the aging degradation of the processor during life-time usage.

Functional testing is based on developing suitable test programs to be executed in a target processor and observing the produced results; this is also referred to as Software-Based Self-Test (SBST) [5]. It has been employed in tests during the operational life cycle [6, 7], targeting for testing such as stuck-at faults [8] and delay faults [9].

Our work is focussed on three main topics: First, developing a suitable functional program for I_{DDQ} testing with regard to a target VLIW processor. It is important that the processor enters a quiescent state during the I_{DDQ} testing. Second, it is required to observe how our target processor is actually aging in order to see the efficiency of our designed test programs; we have developed an accelerated test environment for that purpose. Finally, we present the test results of our I_{DDQ} evaluations.

The paper is organized as follows. In section 2, the target application processor architecture is introduced. In section 3 the developed functional I_{DDQ} testing program is analysed. The designed accelerated test experiments are presented in section 4. In section 5, the measurement setup and data analysis is presented. Conclusions and future work directions are provided finally.

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II. IMPLEMENTED VLIW PROCESSOR ARCHITECTURE

In this section, the architecture of the target VLIW processor, the Xentium® will be briefly described. Based on that, the next section describes the design of the functional program for the I_{DDQ} test separately.

The implemented environment for our I_{DDQ} test is in an UMC 90nm technology Very Large Instruction Word (VLIW) processor, the Xentium® processor, which is designed by Recore Systems [10]. It has been designed for high-performance computing used in automotive as well as space applications, such as global navigation satellite system (GNSS) and beam forming [11]. Figure 1 shows the basic architecture of the Xentium core, which includes a datapath, a decoder / loop buffer unit, an instruction cache, a control unit, tightly coupled memories and interfaces such as the cache port and (Amba-based) HB Bridge.

In order to increase the parallelism, the Xentium datapath has been designed based on a VLIW architecture. It comprises of ten execution units and five register banks. Each execution unit is responsible for a certain class of instructions. For example, A and S units (A0, A1, S0 and S1) perform arithmetic and logic operations. C and P units (C0 and P0) perform instructions under the control of the program counter. M units (M0 and M1) are for multiplier arithmetic. E units (E0 and E1) perform load/store (LD/ST) instructions. All functional units can access five register banks (RA, RB, RC, RD and RE) in parallel (Figure 1).

Each execution unit is connected to the control and the decoder unit. The control unit is responsible for functions e.g. pipelined state machine, program-counter computation, while the decoder unit is in charge of performing the decoded instruction. Loop buffer is especially designed for loop instructions in order to decrease the number of decoder steps. The tightly coupled memories are low-latency SRAMs communicating with the datapath in parallel.

The goal of our research in this paper is to design special functional programs running inside each execution unit for the purpose of exploring the quiescent current signature for reliability monitoring / evaluation.

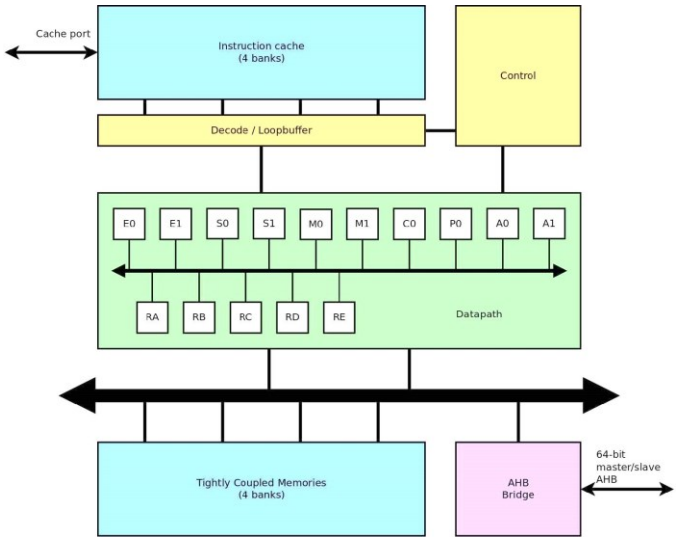


Figure 1. Xentium® processor architecture overview.

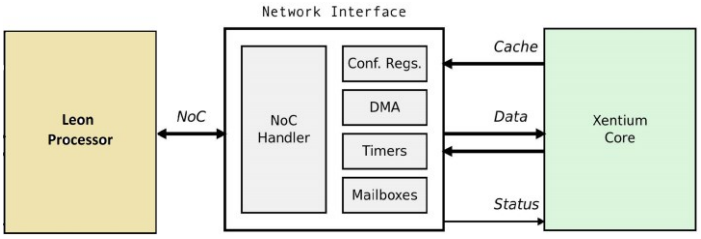


Figure 2. Access to the Xentium processor core via the Network Interface. A Leon processor is used for the control of the Xentium.

The Xentium processor (part of a very complex heterogenous multi-processor SoC) is evaluated in our functional program design combined with another embedded processor, the Leon processor, which will provide control signals to the Xentium via our Network Interface (NI) that directly links to Xentium data/instruction ports. Via control of the configuration registers, mailboxes, timers and direct memory access (DMA) inside the NI, the functional program can be uploaded or monitored. The communication infrastructure is illustrated in Figure 2.

III. THE FUNCTIONAL TESTING PROGRAM DESIGN

The I_{DDQ} functional testing program design will be outlined in this section.

The key idea behind the method for the I_{DDQ} testing lies in letting the Xentium enter a stable and repeatable state, or a quiescent state. For this purpose a '*WAIT*' instruction has been specially employed; it can be set in the configure registers of the Network Interface (Figure 2). It is used to wake-up the Xentium from the idle state and enter the wait state. This procedure can be found in various system specific use-cases, such as Mailboxes, Timers and Interrupts. The test flow for I_{DDQ} is shown in Figure 3.

On the Leon side, on-board switches are set to put it into the debugging mode, in which case the Xentium processor can be controlled by Leon. Next, the Leon processor is powered up. An Application Program Interface (API) in the Leon subsequently powers up the Xentium processor. The Xentium operating frequency is set to 31.25MHz by the Leon, which is directly linked to the sampling specifications of the QT1411 I_{DDQ} current monitor, which will be described in the fifth section.

The mailbox is a communication infrastructure in the Network Interface that can be accessed by the Leon as well as the Xentium processor.

The Xentium will wait and verifies if the Leon processor sends addresses of the executable code from the memory e.g. DDR to the mailbox. During execution of the I_{DDQ} functional program, if the mailbox is still empty, the Xentium will enter the wait for the mailbox state; the Xentium can provide an interrupt to the Leon when this is finished. From the Leon side, the Xentium clock will be shut off to stop synchronization in the processor. The Xentium processor will then enter the wait state, which is required for the I_{DDQ} measurement.

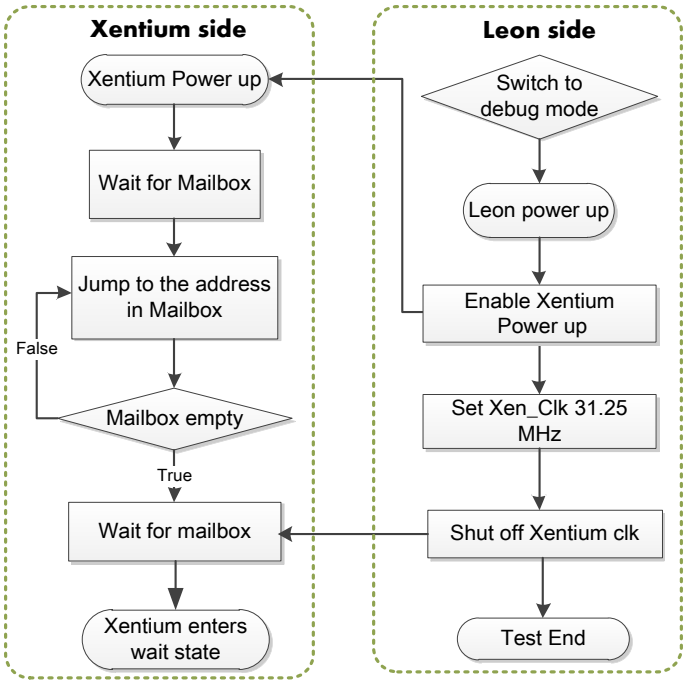


Figure 3. Test flow for the functional I_{DDQ} testing of the Xentium processor under control of the Leon processor.

```
start_IDDQ_testing:

1. INIT                          ;MACRO

2. E0 STW mb_base[MB0], 0
                                 ;First interrupt to Leon
                    indicating  Xentium is ready to perform test.
3. C0 WAIT                       ;Execute wait instruction

4. E0 LDW mb_base[MB0] ;Clear status bit of Mailbox

5. NOP                           ;LW delay slot

6. E0 STW dev_base[MB0], 0
                                 ;Second interrupt to Leon
                    indicating Xentium in wait state.
7. NOP                           ;LDW delay slot
```

Figure 4. Essential part of I_{DDQ} functional program code in Xentium processor.

Figure 4 shows part of the program code running in the Xentium processor during the I_{DDQ} testing. The key information within this code includes:

- INIT: the macro is used for the basic defining of e.g. address allocation for mailbox, local memories and program counter address registration etc..
- First store words (STW) in line 2: the first interrupt to Leon.
- *WAIT* in line 3: the instruction to let Xentium enter wait state.
- Second store words (STW) in line 6: the second interrupt to Leon. With the first interrupt, it is used for the handshake between Leon and Xentium to make sure the Xentium enters wait state, thereafter the Leon can shut off the Xentium clock correctly.

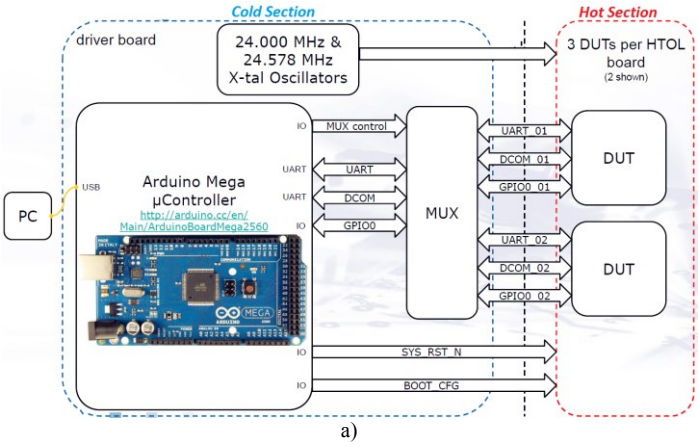
IV. ACCELERATED TEST EXPERIMENTS SETUP

In order to evaluate our approach of using a functional I_{DDQ} reliability test with regard to aging, periodic I_{DDQ} measurements over a period of 1000 hours (aging) of the Xentium processor have been carried out.

Ideally, the aging conditions should be close to the expected application mission profile. However, an *accelerated test* is required in order to reduce the normal-life aging time [12]. Stress can be applied in terms of the operational temperature, processor core power-supply as well as processor workload and processor clock frequency.

Our accelerated aging stress procedure has been carried out for a duration of 1000 hours High Temperature Operating Life (HTOL) profile according to the JEDEC standards [13, 14]. In order to compare the degradation rate of functional test results to the process variation, in total 24 devices have been stressed at a temperature of 125°C, a power supply of 1.2V (1V typical) and a stressed clock frequency of 240 MHz (200 MHz typical).

The basic setup [15] of our accelerated system is shown in Figure 5a, where the hot and cold zones boards are located at the right and left side, separated by the backplane edge connector. On the driver board, there are two crystal oscillators for the Xentium, as well as an advanced microcontroller used for getting *access* as well as generating the stress *workload* for the Xentium through wires e.g. UART, DCOM and GPIO. It is connected via an USB to a PC on which dedicated software runs. A photograph of the implemented printed circuit boards of the driver board, edge connector and HTOL test board is shown in Figure 5b.



a)

b)

Figure 5. a) Basic setup of the I_{DDQ} testing for the Xentium (DUT) scheme b) Actual design of the cold-zone driver board (left), edge connector (middle) and hot-zone HTOL test board (right) with three DUTs. (Courtesy of Maser Engineering).

At a 1-week (167 hours) interval, the stressed hot-section boards have been removed from the oven. The I_{DDQ} measurements for the Xentium processor have been carried out *during* the reliability tests using the driver board, a dedicated interposer board and an I_{DDQ} current sensor is employed during the measurement, which will be discussed in section V.

V. I_{DDQ} Measurement Results and Data Analysis

This section discusses the I_{DDQ} current sensor and measurement results, and analysis on the evaluation of aging detection capability based on these results.

A. The measurement setup

The Ridgetop QT1411 current sensor (Figure 6), having a maximum sample rate of 50MS/s, 100mA range, and a resolution of 12uA, has been employed for our current measurements.

For operating the QT1411, specific pulses and flows are required, which have been programmed via a Virtex4 FPGA board shown on the left (Figure 6). This control program involves the setting of operation commands dealing with I_{DDQ} measurements and proper storage in the flash memory of the QT board, as well as evaluation via a logic analyzer.

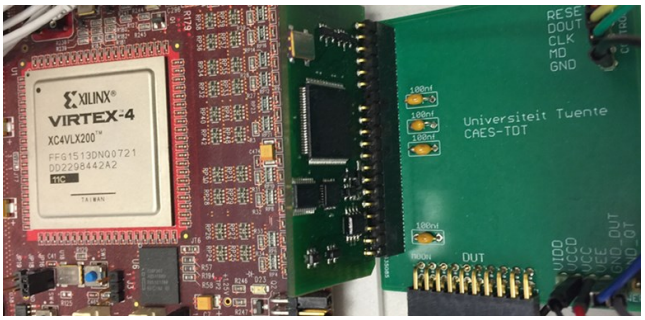


Figure 6. Photo of the Virtex-4 control unit (left), Ridgetop QT 1411 current sensor (vertical board) and developed HTOL interposer board. (Courtesy of Ridgetop Europe)

B. Measurement data analysis

It is expected that the leakage current I_{DDQ} decreases with aging time, as V_{th} increases with time due to NBTI in PMOS transistors.

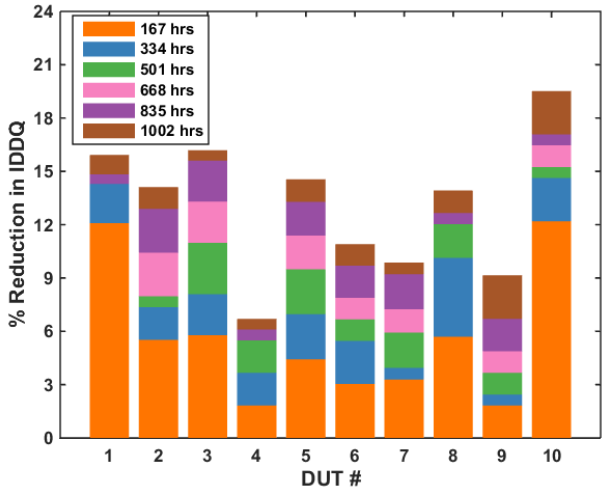


Figure 7. Measured I_{DDQ} reduction of 6 stress times for 10 DUTs under temperature of 30 degree centigrade, Vdd of 1 volt.

Figure 7 shows the reduction rate in I_{DDQ} values of different Xentiums over (aging) time, compared to the initial fresh stage. It can be found that the first aging time (167 hours) for most processors has the largest degradation compared with remaining aging times. The mean IDDQ value for these Xentiums degrades from 2.01mA (fresh state) to 1.65mA (after 1000 hours stress), therefore the degradation rate is $\frac{2.01mA-1.65mA}{2.01mA} \times 100\% = 18.4\%$.

Figure 8 depicts the reduction in I_{DDQ} of the Xentium processor while aging from the measurements results. 10 Xentium processors have been tested, and each stress hour marked on the x-axis. The blue lines are the plots of the mean I_{DDQ} values for these 10 processors. The ±15% variation lines are marked in grey lines.

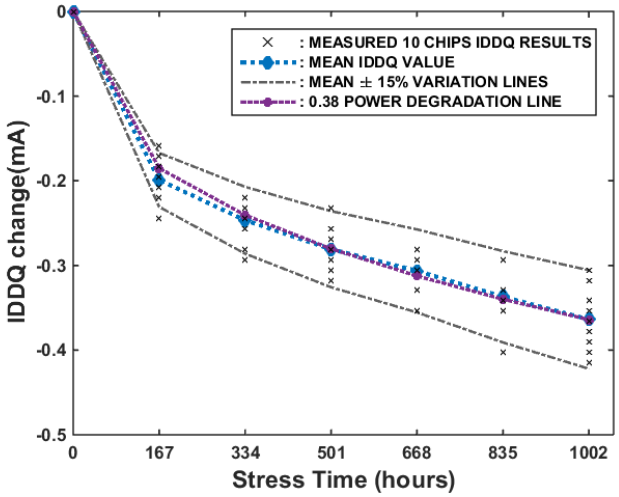


Figure 8. Aging dependent Xentium I_{DDQ} results.

These results show that for the Xentium processor, the mean I_{DDQ} value changes (ΔI_{DDQ}) have a *power* dependency with respect to aging time with a fixed coefficient of 0.38 (purple line in Figure 7). It can be seen the process variation is around 15%, which is less than the degradation rate from fresh to 1000 hours state (18.4%).

Considering the aging mechanism of NBTI, it has been verified through experiments that the threshold voltage has a power law increase under DC stress condition [16].

$$\Delta Vth(t) = Kd \times t^n$$

where *Kd* is a temperature, *VDD*, device geometry and technology dependent constant. This is in coherence with what we have found in the I_{DDQ} test of the Xentium processor, where the mean ΔI_{DDQ} is proportional to $t^{0.38}$. Therefore it has been demonstrated that our methods for aging detection is effective.

It should be noted that under other aging mechanism such as TDDB, the I_{DDQ} can increase with time [17]; the fact that this does not show up in our test results indicates that NBTI is already the dominating aging mechanism in 90nm technology and beyond.

VI. CONCLUSIONS

A detailed design and implementation of a technique for aging-related reliability detection for the 90nm Xentium VLIW processor has been presented, via functional I_{DDQ} testing. One 1000 hours HTOL accelerated test experiments with extensive measurements have been completed on 24 Xentium processors, showing that the I_{DDQ} test result has the power degradation trend that is in line with NBTI aging degradation of the threshold voltage. Therefore, it is testified that our functional I_{DDQ} testing is applicable in the processor aging detection.

This technique can be used in production processors to enhance the dependability with in-field health monitoring and evaluation, advancing with features of non-intrusive and non-cool down service time.

Future enhancements of the technique will include transient current (I_{DDT}) measurements as well, serving to complement our reliability evolution measures, to enable the lifetime prediction for our target processor.

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