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Structural Testing of RSFQ Circuits

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The RSFQ family of logic circuits built in Niobium (Nb) tri-layer processes are being widely used for designs in Superconductor Electronics (SCE). But little information is available about the defects and fault mechanisms occurring in an RSFQ Nb process. Automatic Test Pattern Generation (ATPG), which requires fault models, is a necessity for the efficient test of RSFQ logic systems. The translation of process defects into a corresponding faulty circuit using the presented fault models is a crucial step in this process. As part of the research, we have proposed fault models for structural testing of RSFQ circuits. An RSFQ D-type Flip-Flop (DFF) was used for this purpose and 32 possible defects that can occur in the circuit while processing, were identified. The appropriate defects viz. opens, shorts and defects in a Josephson junction were deliberately induced in the DFF circuit for the verification of these fault models. Extensive simulation experiments were carried out on these defectinduced circuits. The conducted experiments in the test circuits proved that ATPG could be possible in SCE. Special logic test circuits were developed including the Design-for-Testability (DfT) hardware for actual verification of the fault models. This will be the first step towards the development of dedicated ATPG for SCE.