Power-Dissipation Comparison of Two Dependability Approaches for Multi-Processor Systems

Yong Zhao, Xiao Zhang and Hans G. Kerkhoff
Testable Design and Test of Integrated Systems (TDT) Group
University of Twente, Centre of Telecommunication and Information technology (CTIT)
Enschede, the Netherlands
h.g.kerkhoff@utwente.nl

***Abstract*—The additional power dissipation involved in introducing a high dependability in multi-processor systems is nowadays becoming a major concern (power-aware dependability). In this paper[1], the power dissipation components of a recently implemented scan-test based dependability testing approach for a multi-processor Systems-on-Chip (SoC) is evaluated. It is shown that the application of scan-test vectors to the cores is the major power contributor. To avoid this dissipation and hence scan test, a new prognostic approach for life-time prediction using on-line health monitors is proposed accomplishing the same high dependability. It will be shown that the latter approach consumes less power under the *same* dependability specifications. Actual measurements and theoretical calculations are provided as well as a suggestion for future dependable systems given.**

Keywords- MP-SoC systems; power-aware dependability; on-line health-monitoring; dependability testing; prognostics.

I. INTRODUCTION

Recent progress in digital processor SoC implementations show an increased usage of multi-processor SoCs (MP-SoC) to reduce clock frequencies and hence power dissipation while still maintaining a high data throughput [1]. The number of processors in an advanced multi-processor system can vary between two and several hundred [2]. This trend is of course stimulated by the ever decreasing minimum dimensions in CMOS and hence allowed complexity growth. However, the downside of this trend is the increase in variability and decrease in reliability of the components [1, 3].

Reliability is a very important attribute in dependability [4], and hence also the dependability will be degraded. To counteract this loss, several options for increasing the dependability specification have been suggested [5]. The majority of researchers apply Dual Modular Redundancy (DMR) or similar techniques; also the usage of different coding techniques is quite popular. Which approach is chosen in a particular case depends on the application area (e.g. space or security) and allowed types of faults (permanent or dynamic). Our generic *dependability* approach uses internal tests or measurements on processor cores and subsequent repair of faulty processors by remapping and rerouting (spare) correct cores using run-time mapping software.

This paper deals with enhancing (long-term) dependability of multi-processor SoCs being used in high-level security and automotive applications[1]. In our case, aging faults (e.g. NBTI [3]) will degrade system performance and finally result in system failure due to permanent faults. The additional power dissipation resulting from required dependability enhancements is becoming increasingly important [6]. As an example in this paper, our recently built dependable MP-SoC target system will be used; it is based on a BIST approach using structural scan-testing of the cores and core repair via software remapping [7].

In section II, the additional power dissipation of the different hardware and software parts in this system will be calculated which are *only* active in the dependability-testing mode; also system power-dissipation measurements during dependability tests will be presented. It will be shown that the major power contribution of the dependability test is the generation, transportation, application and response of the structural scan-test vectors of the cores.

To fundamentally circumvent this major source of power dissipation, a *new* approach is presented for constructing highly dependable MP-SoCs in section III. It features the *same* dependability (being the attributes') specifications as the scan-test example (assuming the same boundary conditions), but it consumes considerably less energy for its dependability actions. This new prognostic approach for life-time prediction uses on-line health monitors and advanced prediction algorithms to ensure a high dependability and is a good example of the new generation power-aware dependability systems. Finally, conclusions are provided in section IV.

II. POWER DISSIPATION IN A STRUCTURAL SCAN-TEST BASED DEPENDABLE MPSOC

Recently, a nine-processor SoC has been designed, implemented and tested by us in 90nm TSMC technology [9], as shown in Figure 1. The SoC design has been enhanced with

[1] This research has been conducted as part of the Sensor Technology Applied in Reconfigurable systems for sustainable Security (STARS) project and the ENIAC "ELESIS" project financed by Agentschap NL.

978-1-4673-6040-1/13/$31.00 ©2013 IEEE

TABLE I. Main dependability specifications and silicon overhead of dependable MP-SoC performing the "mailbox" SW application [9]

Attribute	Value / Range
Reliability (15 years)	0.99 (Failure rate: 76 FIT)
Non-availability (MDT)	Less than 96ms (@100 MHz clock)
Maintainability (MTTR)	Less than 10ms (@ 100 MHz clock)
Silicon area overhead	Less than 5%

an on-chip dependability manager Infrastructural IP denoted (IIP). Under control of an ARM926 embedded General Purpose Device (GPD), the dependability manager (DM) can generate and multicast deterministic scan-based test vectors for the Xentium™ reconfigurable processor hard IP (Figure 2, Test-Pattern Generator TPG). The DM also compares the results of three Xentiums in parallel (Figure 2, Test-Response Evaluator TRE). A new packet-switched Network-on-Chip (NoC) with routers (R) including network interfaces (NI) was used for communication. To enable the proper tests for the Xentiums (standard 3 at-a-times) wrapper circuits were developed. The systems' dependability attributes and specifications are shown in TABLE I. In this table, MDT denotes the Mean Down Time, while MTTR refers to the Mean Time To Repair. Some key features of our approach are:

- periodic full-scan *structural* test for Xentium logic and memory BIST of all processor cores (three at-a-times)
- full parallel on-line operation of the NoC for normal functional applications and multi-casted structural tests
- highly efficient fault detection (stop on failure)

To our knowledge this is the only highly-dependable MP-SoC approach which has been proven in *practice* for 45 cores in a high-performance real-time 8-beam, 16-channel beam-forming application [8].

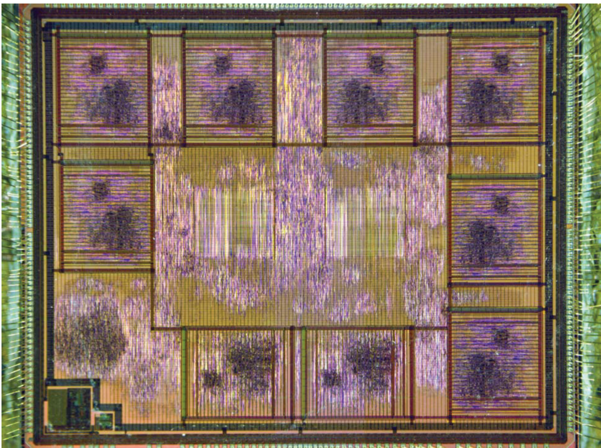

Figure 1. Photomicrograph of our 9-processor core SoC used for dependability-test power measurements (DM located in second left bottom corner).

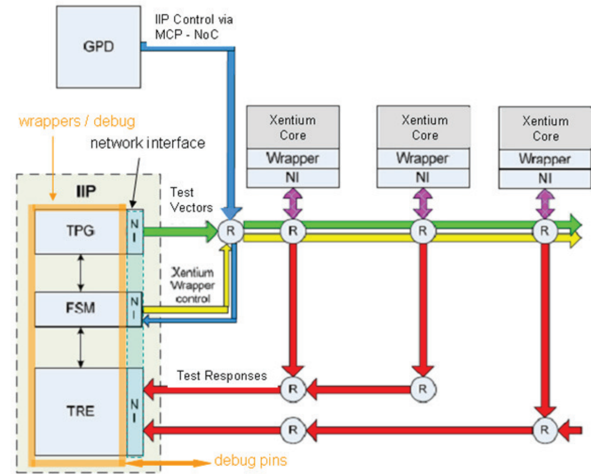

Figure 2. The set-up of the Dependability Manager IIP, NoC, GPD (ARM-based) and three Xentium cores involved in the dependability test. R denotes a router. The local control part is a finite state machine (FSM)

Referring to the previous remarks, it is crucial to known how much power is dissipated by the dependability test and which parts contribute most. The well-known triple modular redundancy (TMR) approach, for instance, is obviously power-greedy; note that our approach has *nothing* to do with TMR. How to calculate the power dissipation of the different parts in the scan-test based approach will now explained in detail (Figure 2).

In order to understand which components are involved and hence dissipate power in the dependability test we refer to Figure 2. The Linux-based *ARM* (GPD) starts to instruct the DM IIP to test a set of three specific Xentium cores. Next the built-in TPG in the *DM* will start generating scan-test vectors. After the network interface (NI) these are multi-casted over the *NoC*. Subsequently these tests will run in parallel on three *Xentium* cores, hence dissipating a substantial amount of power. Next, the output results from the Xentiums are transported over the NoC, back to the DM, more in particular to the TRE. Finally, the results of the comparison will be fed back to the ARM processor.

In this processor, the software remapping to exclude failing and include new Xentium cores for tasks is carried out. For more details is referred to [8]. From the previous paragraph it has become clear that the DM, ARM processor, NoC and Xentiums are involved in the dependability test power dissipation; their contributions to the overall power dissipation will be explained in detail below.

A. *Power dissipation in the Dependability Manager IIP*

The dynamic and leakage (static) power of a logic gate in the used 90nm TSMC CMOS technology is known [9]. The operating clock frequency is 100MHz and all DM blocks (Figure 2) in terms of transistors are completely known to us as designers. The DM is continuously generating test vectors

during the dependability test, and the switching activity was determined to be 80%. As for the gate count, most of the DM complexity is within the TPG part (80%). The DM-NI complexity is only 5% of the DM. After adding the static and dynamic components, the total power dissipation of the DM is calculated to be 13.6mW.

B. *ARM running dependability software*

If one considers that in the structural scan-test based approach only at the start, headers for Xentium™ tests and user-defined periodic polling of DM (@ 100KHz) are communicated by the ARM processor, then it is obvious that not much power is dissipated in the ARM. The power dissipation of the idle ARM processor core is 34mW, while at full performance (e.g. Fast Fourier Transform) it is around 70mW [10]. The run-time mapping of failing processors running on the ARM will not be included here, as will be discussed later. Hence, only a close to idle power dissipation is used, ~ 35 mW.

Besides the ARM processor itself, there are other peripherals and SRAM chips associated to it. Currently it is difficult to *calculate* the exact power dissipation of these parts at board level. Thus when comparing the calculated and measured power dissipation, the peripherals and SRAMS power measurement results are used in *both* cases.

C. *NoC power dissipation*

The power dissipation of our used NoC type (packet-switched NoC with virtual-channel flow control) has been extensively researched in terms of link and router energy being 150pJ for a 256-bit packet. In our approach, scan-test vectors are transported from the DM to three Xentium tiles over the NoC and back. The test-data volume involved is 26 Mbit, and if it is assumed that on average 50% of the routers is active, a power dissipation of 0.4mW can be calculated for a dependability test which lasts for 300ms.

D. *Power dissipation of the Xentium cores*

The dependability tests are carried out in parallel on three Xentiums tiles, which employ a number of parts. In terms of hardware, the Xentium wrapper, Xentium network interface (XNI) and Xentium core scan-chains are involved. Of the leakage power, only the wrapper is included as the rest is already present in absence of a dependability test. First the BISTs of the eight embedded data and instruction-cache SRAMs (192Kbit) in the core are carried out; this is a short burst in comparison with the time required to subsequently perform the deterministic scan tests. On the basis of our design, a total amount of 149mW is dissipated. It is obvious that the latter is the *major* power dissipation contribution, as other parts are negligible.

E. *Added total power dissipation for dependability test*

The total power dissipation of the circuit parts being DM, ARM, NoC and Xentiums during the dependability test is about 198mW (13.6+35+0.4+149). Adding the *measured* PCB peripherals and memory chips dissipation of 115 mW, results in an estimation of 313mW added power dissipation for a dependability test.

F. *Measurements*

Besides the above calculations, primarily meant to determine the dominant power dissipation contributions, also *actual* power measurements were carried out. The CRISP printed circuit board [7] was used at 5V power supply, using a 100MHz clock frequency in combination with an Agilent N6705B power analyzer. The measurement result is shown in Figure 3. The first 400ms in Figure 3 reflects the power dissipation in the *absence* of a dependability test. The peaks during the next 600ms are due to the dependability test of a single MP-SoC on three Xentium cores. When the dependability test has been completed, the system power dissipation drops to the original level.

The dependability test starts at 400ms and lasts for about 300ms. The averaged power increase of this part (the higher peak) is around 300mW. After the dependability (scan) test has been carried out, the ARM and some other board peripherals and the SRAM chips on the PCB continue to be active for some 300ms. The lower peak represents their activities and the average power of this part is about 150mW. It should be noted that this part of power dissipation persist in the higher peak during the dependability test. Thus the measured power increase caused by the dependability circuits (DM, ARM, NoC and Xentium) and peripherals is 300mW, which is close to the theoretical calculation of 313mW.

As the measured power increase is caused by the dependability test and its related activities, it can be concluded that the overall measured power increase related to the dependability *test* (not repair) of three Xentiums is about 225mW being the *average* of 300mW and 150mW.

In practical cases, dependability tests usually do not have to be carried out continuously. All nine Xentiums in the MP-SoC can be evaluated within 1800ms. Only the power increase for evaluating three Xentium cores will be used, as this is sufficient for our purpose in this paper.

One can conclude that the measurements are sufficiently in line with the theoretical calculations. It has also been shown that the scan-tests of the three Xentiums form by far the major

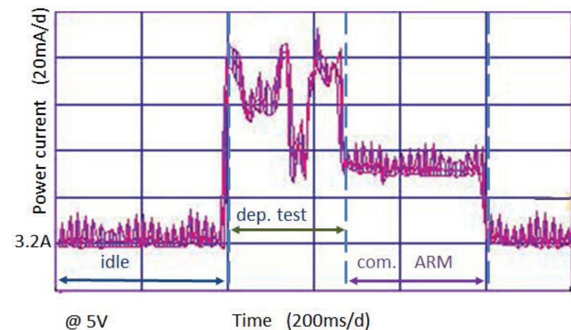

Figure 3. Screenshot of the power dissipation increase during a dependability test. Horizontal axis 200ms/div, vertical axis 20mA/div.

contribution in power for the dependability test and even more in terms of energy. If one has to reduce this significant power dissipation, an alternative would be to circumvent the structural scan testing of Xentiums completely. This leads to a new approach which will be the subject of the next paragraph.

III. Power dissipation in a health-monitoring prognostics-based dependable MP-SoC

The previous scan-test based approach detects a faulty Xentium processor which is a reaction *after* the occurrence of a fault. Our new approach avoids scan-tests completely and uses health monitoring (HM) and prognostics for predicting (action *before* fault occurrence) at which moment a processor core becomes a potential risk for correct operation with a certain confidence (e.g. 90%). In this case, a number of relevant parameters are monitored *for each* Xentium processor core (e.g. temperature, delay, voltage, and current) which relate to its life-time (i.e. health). To be able to compare this approach with the previous, we used the same minimum dependability attribute specifications and conditions as listed in TABLE I for our target system. It is noted that for *both* dependability approaches the same mission (automotive, NXP) profile has been assumed. Furthermore, as in the scan approach, only devices are delivered to customers if the Xentium key parameters are within their tolerance bands. This also holds for the monitors; during final test, their first measurement results are digitally stored. This takes care of gross process variations.

Key features of this approach are:

- during the dependability tests, all Xentium cores can work in normal operational mode. Only current and voltage monitors are connected to the local IP pins.
- multiple physical entities (temperature, delay, voltages and current) can be used (non-invasive) for accurate scalable prognostics
- full on-line operation of the NoC for normal functional applications and health-monitors measurement data transfer in parallel

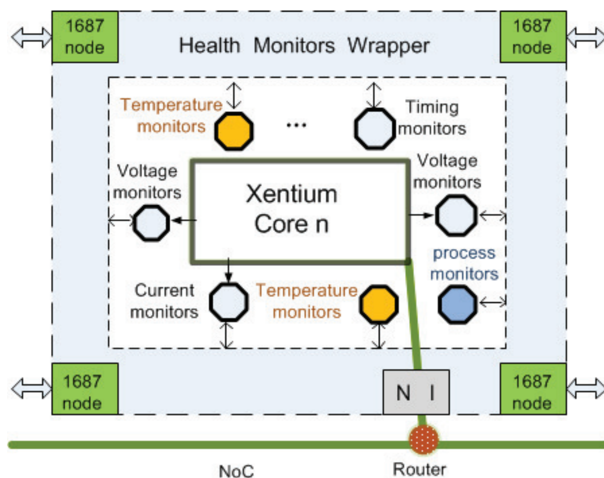

Figure 4. Symbolic drawing of a single Xentium™ core with health monitors (HM), monitors wrapper and network interface (NI). *Optionally* P1687 nodes, P1687 client/host network and TAP controller.

Figure 4 shows the schematic setup of a *single* Xentium core, surrounded (wrapped) by several monitors. In practice, several (e.g. four) strategically placed temperature sensors and voltage monitors are located near the core. Only one non-invasive delay monitor is used [11]. The same holds for the (power) current monitor [12]. Optional are monitors which provide information on changing process parameters, e.g. NBTI via V_{th} measurement [13]. The signals from the monitors are if required, converted to digital data in the health monitors wrapper (Figure 4). Worst case this requires (shared) amplification and data conversion (ADC) in the monitors' wrapper, but all-digital versions are in progress to appear soon. The digital HM data is subsequently transported via the network interface (NI) and NoC (Figure 4) to one of the two ARM cores (Figure 5) in the anticipated STARS SoC. An alternative option, not to be discussed here any further, is regarding the monitors as *embedded instruments* and proposes the usage of the P1687 protocol.

Our experiments have shown that temperature and I/O stress are important reliability factors. Based on periodic measurements from the monitors, parameter data enters our (software) life-time prediction (LTP) model in an ARM core, and finally results in an advice to e.g. switch-off the Xentium prior to break-down. As can be seen from Figures 4 and 5, this innovative approach therefore involves health monitors (sensors), possibly analog front-end (AFE) circuits and registers in the monitors' wrapper, the NoC and an ARM processor. The MP-SoC architecture in Figure 5 is targeted at high-speed massive signal processing for high-level security applications. It features high-speed I/O (electrical as well as optical), 48 (6x8) Xentium™ cores, NoC communication, several SRAM tiles, and dual ARM cores.

The first step in the dependability test of the HM prognostics approach (Figure 5) is to send a message from an ARM core via the NoC to (a) Xentium core(s) which monitor(s) have to start a measurement. Next, a monitor has to start measuring the parameter concerned, e.g. the temperature, and in case of an analogue output, it has to be converted into a digital word in the AFE in the monitors' wrapper (Figure 4). This data is subsequently sent (in parallel with the normal application data) over the NoC to the ARM core (Figure 5). Based on this data, the ARM updates the lifetime prediction of this Xentium core and decides to label it correct or potentially faulty. In the same way as in the scan-test approach, the repair actions can be carried out being to take out a potentially faulty core, remap its task to a spare processor and connect it. This is the reason why this part has not included in the power-dissipation *comparison* calculations.

From the previous remarks it is clear that the health monitors and AFE, NoC and one ARM core are involved in the dependability test power dissipation. Their contributions to power dissipation will be explained in detail below and reveal its major contributors. Notice that the Xentium core itself is not used at all in terms of its logic in the decision process.

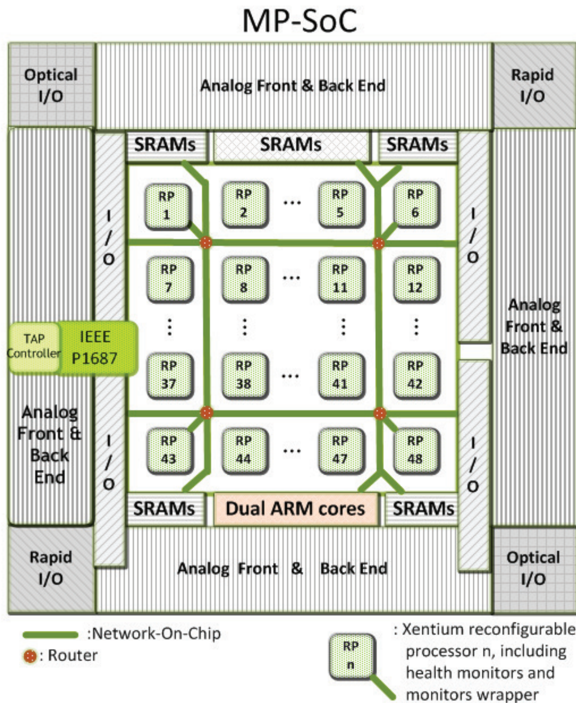

Figure 5. Highly dependable power-aware MP-SoC using prognostics and health monitors.

A. *Power dissipation of health monitors*

Several options for on-chip sensors for health monitoring in terms of power dissipation have been investigated: temperature T, currents, voltage and delay monitors. Their specifications and measured power dissipation are summarized in TABLE II. Our current approach will use four temperature sensors at different locations around the core; two voltage monitors are employed, and a single delay and a current monitor. The monitor selections are based on HAST experiments of the Xentium core, its stress conditions and measurements. Also the parameters of the LTP models are derived from that and this determines the actual dependability accuracy; for small (tolerated) process variations, the decision criterion can be changed and stored after final test. The usually multiple data of the same monitors (T) will be averaged in the ARM processor. The total power dissipation for a *single* Xentium is 11.3mW (V_{dd} @ 3.3V).

B. *Analog Front End power dissipation*

In the health monitoring system, the AFE is optional and it will only be active if the analog sensors are active. The current AFE consists of an OpAmp and an ADC. The continuous power consumption of our OpAmp with a high gain (>50dB) is 1.4mW; in the case of our pipelined ADC with an accuracy of 12-bit, the continuous power consumption is 4.1mW. Hence in the case of a shared AFE this results in 5.5mW. As a continuous operation is not necessary even for multiplexed health monitors, a practical operation below 1mW is possible. Purely digital health monitors are obviously always preferred and the future way to go.

C. *NoC power dissipation*

In the health-monitoring approach, only very few simple sensor commands like e.g. “start measurement” and few data such as periodic measurement results of around eight 12-bit words a time are transported over the NoC to the ARM. Hence its contribution to power dissipation is completely negligible.

D. *Power dissipation of the ARM core*

The tasks of the ARM core are significant in the health-monitoring approach for MPs. First some basic control has to be provided such as generation / transmission of Xentium core headers and monitor(s) assignments to start measurements. This requires a maximum of 100 instructions. The same holds for closing the HM activity by the ARM. The next step requires reading of 12-bit data of a maximum of 8 monitors at a time from the NoC and to store this data with a time stamp. This step requires around 1300 instructions. However, the most complex part for the ARM is the life-time prediction calculation. Our current experience with the combined linear/exponential stochastic degradation path model shows this will require a program size of around 15kB. This translates into roughly 50k instructions [14]. The last step involves storage of crucial (abstracted) data from the calculations (e.g. modified model) in the memory requiring a maximum of 100 instructions. The total number of instructions in the ARM core for determining the lifetime for a Xentium core, and storing crucial data is therefore 51.6k instructions. Following the power-estimation model of an instruction set simulator (ISS) as suggested in [15], based on actual values of the physical current during execution of an instruction, the total software-program power consumption W_p can be written as:

$$W_p = V_{dd} \times \sum_{i=0}^{N-1} (I_i \times N_i) \qquad (1)$$

V_{dd} denotes the supply voltage, I_i is the current during the execution of each instruction for the task i, and N_i the number of instructions per second of the task i. The power consumption for software is the difference that the ARM core processor is turned from idle mode (W_{idle}) to the active mode (W_{act}). The mean speed for our ARM processor N_u is $200MIPS$ (million instructions per second) [17]. Working under the condition of $V_{dd} = 1.2V$, the mean current per instruction can be calculated from:

$$I_u = (W_{act} - W_{idle})/(V_{dd} * N_u) \qquad (2)$$

This results in our case in $0.15nA$ per instruction. The total software power dissipation for the ARM is hence 51.6k multiplied by the above current per instruction, being 9.39mW. Using the idle power value of the ARM and add the I/O (34mW) and the previous program dissipation, a total of around 44mW results for the contribution of the ARM core.

TABLE II. Specifications and measured *continuous* power dissipation of four types of health monitors

Monitor	Range	Resolution	Power (mW)	Analog /Digital
Temperature	-50ºC ~150ºC	±0.8 ºC	0.0037	Digital
Current Idd	0 - 100µA 50 µA - 100 mA	50nA 50 µA	0.160 0.075	Digital *Analog*
Voltage	0 – 1.2V	1mV	5.5	*Analog* Digital
Delay	0 – 4ns	0.8ps	0.11	Digital

E. *Additional power dissipation for the dependability test*

One may conclude that the health monitors (11.3mW) and AFE power dissipation (5.5mW) are responsible for 16.8mW in the *continuous* mode for a *single* Xentium core. The ARM power dissipation (44mW) is the other power contributor, amounting to a total of 60.8mW for a single Xentium during 258µs. For three Xentiums the time required will be 774µs. This power dissipation is less than in the scan-test approach.

IV. CONCLUSIONS

Power dissipation calculations/simulations as well as measurements have been carried out during dependability tests of existing, dependability-enhanced MP-SoC. Standard software loads were used for the cores, and temperature and V_{dd} lab-controlled. A detailed power-dissipation evaluation revealed that in this case the required scan-tests contribute by far to the dependability test power dissipation. To reduce this dissipation, a new approach for dependability enhancement has been investigated, based on health monitoring and prognostics. Although the two approaches are fundamentally different both accomplish the same minimum dependability specifications, under the *same* mission profile and process-variation tolerance bands. The first approach uses structural scan testing of Xentium tiles and subsequent mutual comparison. Based on the results it commands the run-time mapping software in the ARM to isolate a *faulty* core and

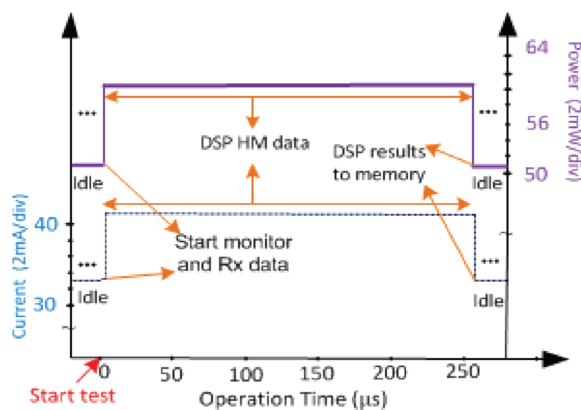

Figure 5: Graph of simulated power dissipation during the dependability test of a *single* Xentium in the case of health monitoring. Horizontal axis 50µs/div, left vertical axis is 2mA/div, right axis is 2mW/div.

introduce a spare processor and then remaps tasks. The second approach, based on health-monitors per Xentium processor, comes also to a conclusion on whether or not to remove a *potentially* faulty processor. After that, the steps of remapping are exactly the same as in the first approach. As the latter steps are the same, the difference in power dissipation is just in the decision-making which processor has to be removed. Calculations and some measurements show that the health-monitoring approach requires less power (127mW during 774µs) as compared to scan-testing (225mW during 600ms). The test-based approach involves testing of the Xentium cores leading to a major cause for power dissipation, while the ARM hardly dissipates power. In the health-monitoring approach the situation is more balanced. Even more important, there is a significant difference in test duration, which is 600ms for the scan-testing approach while only 774µs for the health-monitor approach. Therefore in terms of *energy* the latter is more than 1380 times more efficient, and hence a health-monitoring approach is favoured over BIST approaches in dependable MP-SoCs.

REFERENCES

[1] International Technology Roadmap for Semiconductors (ITRS) 2011, " Reliability & Manufacturability," (http://www.itrs.net), 2011.

[2] S. Borkar, "Thousand core chips - A technology perspective," in Proc. Design Automation Conference (DAC), pp. 746–749, 2007.

[3] Y. Cao, P. Bose, and J. Tschanz, "Reliability challenges in nano-CMOS Design," IEEE Design & Test of Computers, pp. 6-7, 2009.

[4] A. Avizienis, J.-C. Laprie, B. Randell, and C. Landwehr, "Basic Concepts and Taxonomy of Dependable and Secure Computing," IEEE Trans. on Dependable and Secure Computing, vol. 1, pp. 11-33, 2004.

[5] D. Gizopoulos et al., "Architectures for on-line error detection and recovery in multi-core processors," in Proc. DATE, Germany, 2011.

[6] S-K. Eo, S. Yoo and K-M. Choi, "An industrial perspective of power-aware reliable SoC design," in Design Automation Conference (ASPDAC), pp. 555-557, March 2008.

[7] X. Zhang and H.G. Kerkhoff, "A dependability solution for homogeneous MPSoCs," in 17th IEEE PRDC USA, pp. 53-62, 2011.

[8] T. Ahonen et al., "CRISP: Cutting Edge Reconfigurable ICs for Stream Processing," in Reconfigurable Computing: From FPGAs to Hardware/Software Codesign, Springer Verlag, London, 2011.

[9] T.S.M. Company (TSMC), "TSMC 90nm Core Library Application Note," editors, January 2006.

[10] H. Kim et al., "Industrial case study of ARM926 power modelling," in Journ. of Semicon. Techn. & Science, vol. 5, no.4, pp. 221-228, 2005.

[11] K. Tae-Hyoung, et al., "Silicon Odometer: An On-Chip Reliability Monitor for Measuring Frequency Degradation of Digital Circuits," IEEE Journal of Solid-State Circuits, vol. 43, pp. 874-880, 2008.

[12] V. Stopjaková, "Accurate Dynamic IDD Testing and Localization of Defective Parts in Mixed–Signal Circuits," Journal of Electrical Engineering, vol. 58, pp. 26-32, 2007.

[13] C. Shi-Wen et al., "Fully on-chip temperature, process, and voltage sensors," in Proc. ISCAS, pp. 897-900, 2010.

[14] V. Tiwari, et al., "Power analysis of embedded software: a first step towards software power minimization," IEEE Transactions on VLSI Systems, vol. 2, pp. 437-445, 1994.

[15] ARM Limited. (2000). ARM9TDMI (Rev 3) Technical Reference Manual. Available: http://infocenter.arm.com/ help/topic/com.arm.doc. ddi0180a/DDI0180.pdf