An A/D D/A board using IEEE-1355 DS-links for a heterogeneous multiprocessor environment

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Abstract. In our approach for developing heterogeneous control systems, we have developed a real-time A/D D/A board called "the Raptor". The Raptor communicates over high speed and highly reliable DS-links (IEEE-1355). To obtain highly accurate analogue conversions, the A/D and D/A converters have a 12-bit resolution. We measured a maximum sampling frequency of 90.5 kHz on each A/D channel. For communication with the rest of the control environment, two 100 Mbit/s DS-links are available. The Raptor forms a part of a heterogeneous multiprocessor closed-loop control environment. This new environment can be used, amongst others, for controlling heavy robot applications. The work on this environment takes place in scope of the JavaPP (Java Plug & Play) project. The software will be developed together with the CJT-library that provides inherent object-oriented and parallel design patterns, according to the CSP paradigm, in Java.

1. Introduction

For heavy mechatronic and robot applications, the need exists for a high-performance real-time control environment. Typically, sampling frequencies lie in the range of up to approximately 10 KHz. Oversampling can be applied, such that derivatives of the acquired signals can be achieved by digital filtering (e.g. velocity out of position).

Our existing control environment (Bruis et al, 1993), which uses transputers and transputer links as computing power and means of communication, is becoming obsolete since development in transputers has stopped and they get outperformed by modern microprocessors.

In order to prevent this situation from happening again, the transputers are being replaced by a heterogeneous mixture of microcontrollers. This way, the entire control environment will not be dependent on the developments in one line of processors.

We want to preserve the benefits of the good-old transputer concept, therefore a substitution for the transputer OS-links is needed. Walker (1996) showed that *IEEE-1355 Data-Strobe links (DS-links)*, which have communication speeds up to 100 Mbit/s, are a competitive alternative for OS-links, which only have communication speeds up to 20 Mbit/s.

A first search for commercially available boards fitting this configuration and our specific needs has been performed, but no such boards were found. Therefore we decided to re-design our existing environment, to fit our specific needs.

This paper presents the new control environment, and more specifically, an A/D D/A interface board called *the Raptor*. The name Raptor has been chosen rather arbitrarily since it sounds good, as such it does not constitute an acronym, nor bears any reference to the US F-22 advanced tactical fighter plane. In chapter 2 our control environment and the design goals for the Raptor are discussed. Chapter 3 deals about sampling with the Raptor. In chapter 4 the actual realisation of the Raptor is described. Chapter 5 discusses the performance of the A/D and D/A converters of the Raptor, along with the performance of the DS-links. Finally, in chapter 6 the conclusions and recommendations are stated.

2. The architecture of the control environment

The basic architecture of our existing control environment is still useful, therefore the new environment uses the same architecture. The core is formed by interface boards with microprocessors and I/O hardware, interconnected via communication links, which are routed via a router chip located on a separate routing board (see figure 1). All boards are connected via a *backplane* (the *Twente LINX Backplane*, Schwirtz et al, 1992a), and the network implements a star topology, with the router in the centre of the star, the interface boards as nodes, and communication links as edges.

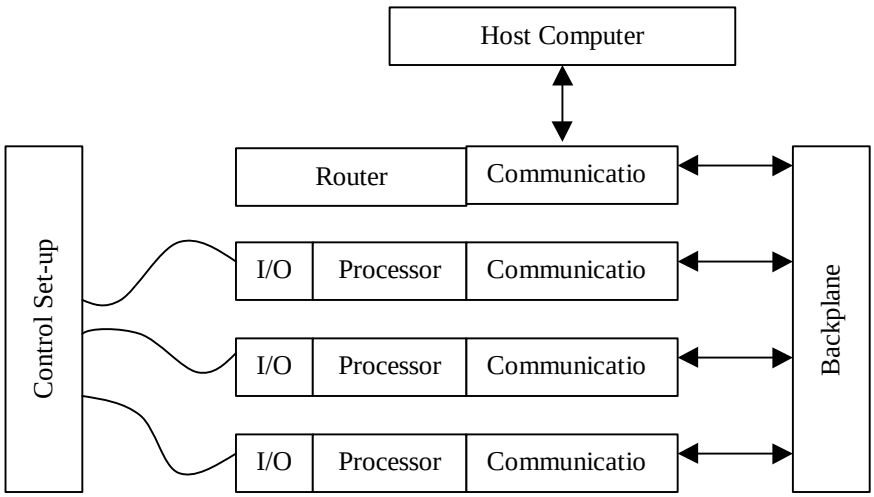

Figure 1: The basic architecture of the control environment

In the new environment we re-used the LINX backplane, which was designed for speeds of up to 20 Mbit/s (the speed of OS-links). Fortunately, tests (Greve, 1998) showed that the backplane is capable of properly handling speeds up to 100 Mbit/s (the speed of DS-links).

All the new application boards will be equipped with (at least) one DS-link adapter, so they can communicate over the backplane using DS-links. Several new application boards will have to be designed for the new high-speed environment. One of the most important boards for a control environment is an A/D D/A board, therefore this is the first new application board which has been designed. Such a board had already been designed for the former control environment (Schwirtz, 1992b), and it performs efficiently (Broenink and Tiernego, 1996). Therefore this board stood model for the Raptor.

In the new environment communication takes place via the *Tarantula* router board, which is currently under development at the University of Twente (Brummel, 1998). This board contains an STC104 router chip, which provides 16 100 Mbit/s DS-link channels between all application boards connected to the LINX backplane. There are also external DS-links

available, which makes it possible to directly connect a second backplane, external application boards and/or a PC (host controller) to the router board.

The basic architecture of the control environment is shown in figure 1. A more detailed picture of the current developments of the control environment is shown in figure 2.

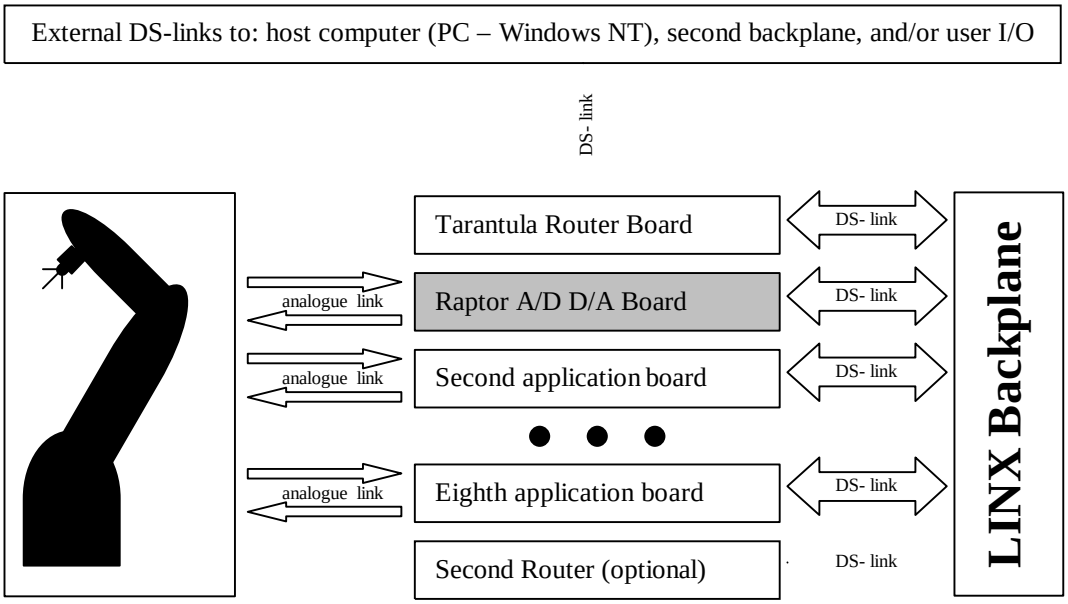

Figure 2: The control environment using the Tarantula and the Raptor

Currently, the interface boards and the router board are being re-designed. The Raptor was designed to become a high-end A/D D/A board, which means that the accuracy of A/D and D/A conversions is of crucial importance. Digital lines are known to cause interference on analogue lines, so the first important design consideration was that there should be a clear separation between the analogue section and the digital section on the board.

In order to make the Raptor universally applicable, several further design considerations were of importance:

- Both analogue and digital I/O lines should be amply available;
- Enough means of communication should be present;
- The amount of SRAM on board should not be chosen small;
- The board should be capable of working in a stand-alone environment.

With these design considerations in mind, figure 3 shows a functional block diagram of the Raptor. Note the clear separation between the analogue and the digital sections of the Raptor.

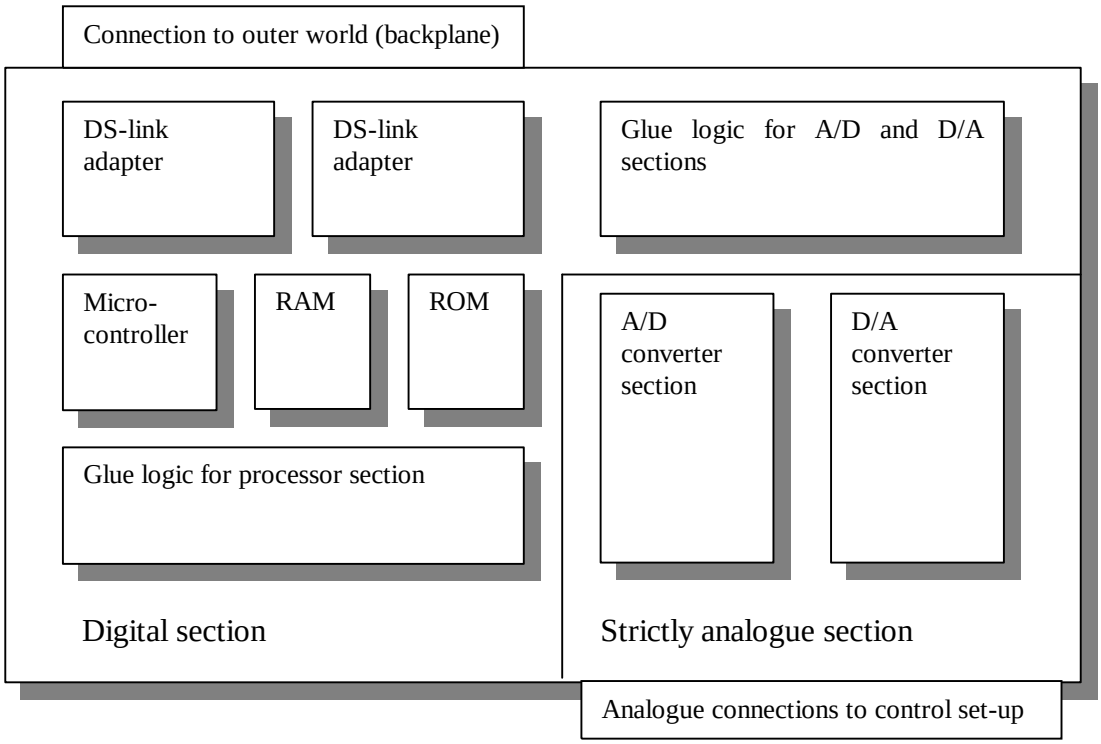

Figure 3: Functional block diagram of the Raptor

3. Sampling with the Raptor

Since software normally can not simultaneously start sampling on more than one converter, samples are typically taken sequentially, initiated by a timer. This situation is shown in figure 4 for sampling instants t = 0, T.

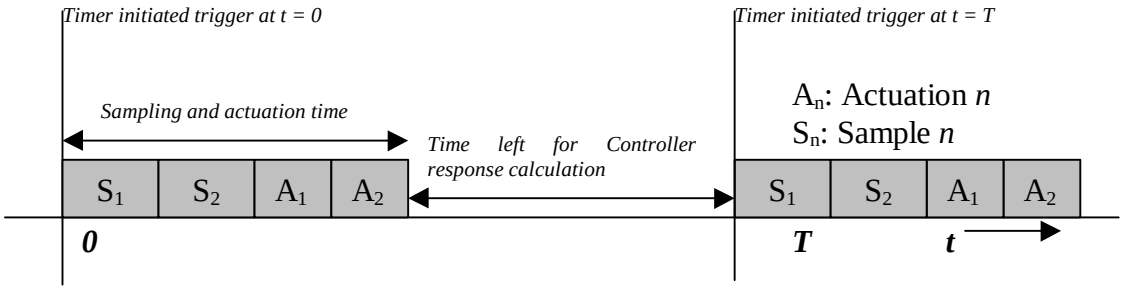

Figure 4: Sequential sampling and actuation instants

However, Sunter (1994) showed that in control environments with high sampling frequencies (≥5 KHz) it is necessary to perform simultaneous sampling on all A/D converters (even if this means oversampling). Also, the D/A conversions should all take place at that moment. By doing this, the sampling and actuation system becomes *time-bounded*, and samples will not be shifted in time.

To properly achieve this, the processes taking care of the sampling and actuation should be executed at precise moments in time. This can be achieved by using a *global external trigger* signal, which starts conversions. This way, jitter caused by timer-initiated triggers is prevented. Figure 5 shows this for sampling instants t = 0, T.

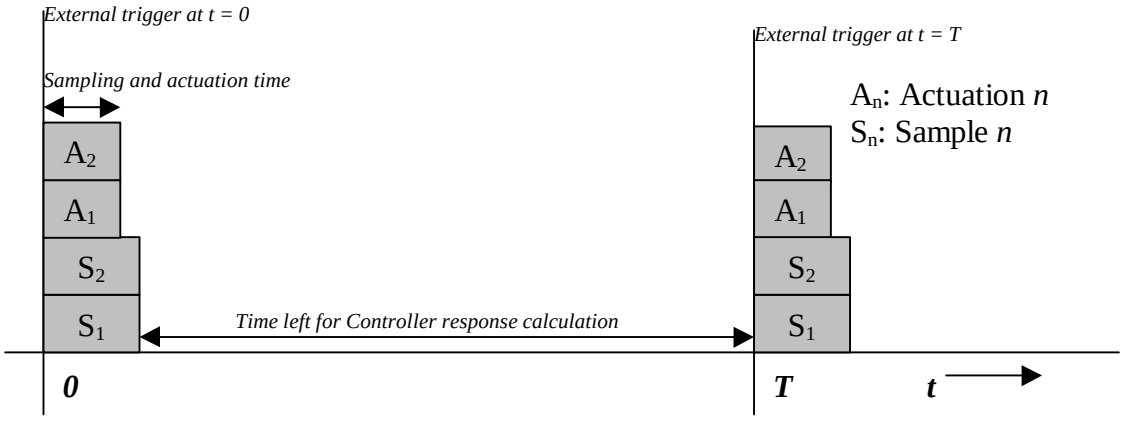

Figure 5: Simultaneous sampling and actuation instants

Making the processes time-bounded creates a more predictable controller, which is a very important property for real-time control environments. In order to achieve the highest level of predictability, the backplane provides a clock signal to which all boards can be *globally synchronised*. In environments where the predictability is not so important, the on-board processor can also refrain from using the global clock signal, and start conversions itself.

4. Realisation of the Raptor

Figure 6 shows the actual Raptor.

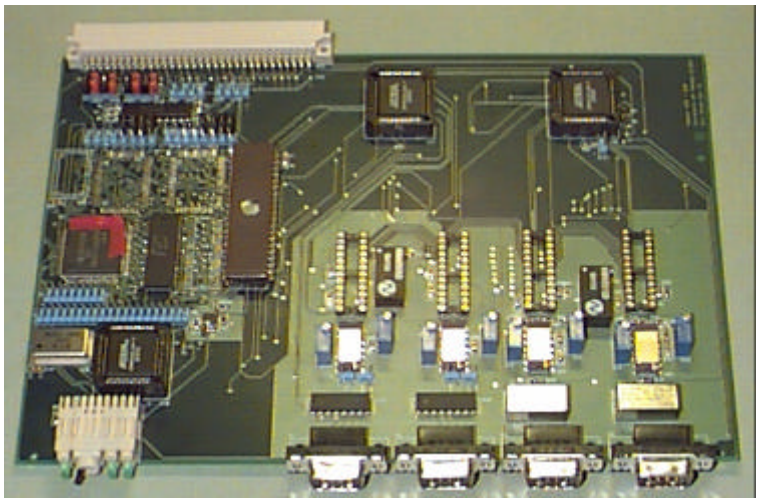

Figure 6: The actual Raptor

The microcontroller chosen for the Raptor is the Hitachi SH7032, it is a fast (20 MHz) microcontroller with an elegant Motorola-based 32-bit architecture. It also provides an elaborate interrupt mechanism, 2 RS-232 serial interfaces, 5 DMA channels, an on-board A/D converter, several timers and more features . Using this microcontroller constitutes one of the first experiments for finding a suitable replacement for the T222 transputer, which was used on the Raptor's predecessor.

12-bit A/D converters and D/A converters (Analog Devices AD7870LN and AD7245ABN, respectively) have been chosen, since they have been used successfully before. In order to get accurate A/D D/A performance, the following precautions have been taken in designing the PCB:

- The analogue parts (A/D converters, D/A converters and instrumentation amplifiers) have a separate power source. This means that the regular power supply which feeds all digital logic, is *not* used for the analogue parts;
- All digital components, especially clock lines, have been kept as far as possible away from the analogue components and power lines;
- Extensive power decoupling has been applied to the analogue power lines to eliminate potential spikes;
- Copper zones (tied to the analogue ground) have been used to further shield the analogue signals from the digital signals.

In order to make the Raptor universally applicable, both analogue and general purpose digital I/O lines have been made amply available. The actual board has two A/D converters and two D/A converters. Additionally, two 4:1 multiplexers in the A/D section provide possibilities for connecting up to 8 analogue sources to the A/D converters. External digital I/O can directly be connected to the board, using a flat-band cable, to either a 16-bit I/O port or to an 8-bit input-only port. Also, for obtaining sufficient means of communication, two DS-links are available on the Raptor. Finally, 128 Kb and 256 Kb SRAM configurations are possible on the Raptor, in order to be capable of running potentially large user code.

The board has been designed to work with the backplane and with an STC 104 router, however, the board can also be used stand-alone. If this is required, care should be taken that the board gets its power over the backplane connector. Also, if communication via DS-links is desired with other boards, this should take place over the backplane connector, since the DS-links are wired to the backplane connector.

The EPROM contains a bootstrap loader for downloading user programs (via the RS-232 serial interface) to the SRAM on the Raptor. This provides a flexible way of re-programming the Raptor. In total the Raptor has two RS-232 interfaces, to which several peripherals can be connected, such as dumb terminals for debugging purposes. It is even possible to directly connect one or more other Hitachi SH7032 microcontrollers to the serial interface, and let them work in multi-processor mode. Eventually, the Tarantula and all application boards should become programmable over the DS-links. One central host computer will then configure the complete control environment.

Finally, the external trigger signal for global synchronisation, is provided over the backplane.

5. Performance

5.1 A/D section

Sampling frequency

The A/D converters have a sampling frequency of 100 KHz, however, in an actual system there is always overhead for retrieving the sampled value, instruction execution latency, etc. Therefore a straightforward test has been conducted to measure the amount of overhead when sampling. A counter of the microcontroller is reset and started (increment 1 per clock cycle), after which the A/D converter is started. When the interrupt occurs signalling the completeness of the A/D conversion, the counter is stopped.

Using this test, the timer counted 221 clock cycles (at 20 MHz), which is 221 X 50 ns = 11,050 ns per sample, yielding a sampling frequency of roughly 90.498 KHz. A breakdown of the sampling time looks as follows:

- Conversion time: 10 µs (data sheets);
- Interrupt response time: between 0.50 – 0.95 µs (data sheets);
- C latency for manipulating the timer and A/D converter: between 0.1 – 0.55 µs (measured).

It is not likely that sampling in this way will occur very often, however, 90.5 KHz should be a good indication of the maximum acquirable sampling frequency per A/D channel.

Accuracy of the A/D converters

In order to determine the accuracy of the A/D converters the following test has been performed. First the input of the A/D converters has been tied to the analogue ground and the converters have been trimmed around the value 0, then 1,000,000 samples were taken (10 times over). A combined set of histograms with the results of this test for the first A/D converter, can be found in figure 7 (the eleventh column (Avg) constitutes the average of the ten measured amounts per conversion value).

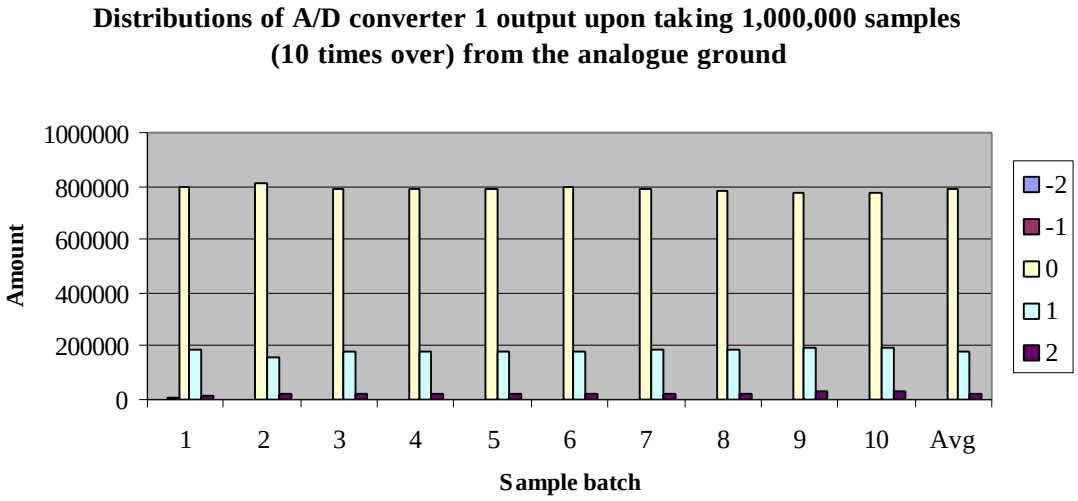

Figure 7: Conversion results for A/D converter 1

Some statistics are of interest for determining the accuracy of the A/D converters, therefore for both converters the expectation value E(X), the variance var(X) and the standard deviation σ_x have been calculated.

When the discrete stochastic variable X is defined to be the measured conversion value, and the average values (Avg) of the ten sample batches are used, the following results have been obtained:

A/D converter	E(X)	var(X)	s_x
1	0.23	0.23	0.48
2	0.09	0.24	0.49

Table 1: Expectation value, variance and standard deviation for both A/D converters

Other tests with the A/D converters (e.g. by connecting a 1.5V battery to them) yielded similar results. The manufacturer of the A/D converters guarantees an accuracy up to ½ LSB, which is consistent with the σ_x we measured, thus the board introduces no further loss of conversion quality due to interference.

5.2 D/A converters performance

<<<To be determined yet , also speed and accuracy>>>

5.3 DS-links performance

<<<To be determined yet >>>

5.4 Processor performance

<<<To be determined yet >>>

6. Conclusions

We expect, using the architecture presented here, that we found a sophisticated set-up for a high-performance real-time control environment for mechatronic systems. Other boards using other types of processors can straightforwardly be added, thus exploiting the feature of heterogeneity.

- The A/D conversions are accurate up to ½ LSB, meaning that the design of the analogue section works very well, and needs no improvement. The maximal achievable sampling time is 11 μs implying that 1 μs is caused by interrupt and software latency (the used A/D chip has a conversion time of 10 μs).
- The D/A converters show an accuracy equal to the specifications of the D/A chip (<<yet to be checked>>). The conversion time is <<to be determined>>.
- The communication via DS-links implements a throughput of XX Mbit/s, using packages of XX bytes (X single precision reals)
- The Hitachi SH7032 microcontroller is capable of handling XX FLOPS per sample at the highest sampling rate, which is sufficient for an average State Variable Filter to determine a rate of a measured signal << to be measured>>.

For further research, it is clear that the total control environment needs to be tested. Besides performance tests and controlling a real heavy application like a complex industrial robot, also tests using different types of processors should be done.

<<If performance turns out to be too low:>>Since the used microcontroller is not powerful enough to perform data processing by floating point digital filtering (to e.g. determine the rate of a measured signal) at the highest possible sampling frequency, a microcontroller with floating point unit is desired when such filtering is needed.

References

Broenink, J.F. and Tiernego, M.J.L. (1996), *Peg-in-hole assembly using impedance control with a 6 DOF robot*, Proceedings 8th European Simulation Symposium, "Simulation in Industry", October 24-26 1996, Genoa, Italy, A.G. Bruzzone and E.H.J. Kerckhoffs (eds.), SCS, pp 504-509.

Bruis, R., Bakkers, A.W.P., and Broenink, J.F. (1993), *A transputer-based modular control environment for mechatronic systems*, Journal A Benelux quarterly journal on automatic control: vol. 34, no 1, April 1993, pp 41-50.

Brummel, M.A. (1998), *Integration of a router in a multiprocessor environment*, M. Sc. Thesis, ref. Nr. 005R98 EL Control Laboratory, University of Twente, Enschede The Netherlands, 1998.

Greve, O.J. (1998), *Integration of a microcontroller in a multiprocessor environment*, M. Sc. Thesis, ref. Nr. 004R98 EL Control Laboratory, University of Twente, Enschede The Netherlands, 1998.

Hilderink, G.H., Broenink, J.F., Bakkers, A.W.P., and Vervoort, W.A. (1997), *Communicating Java Threads*, Proceedings WoTUG-20, "Parallel programming and Java", April 13-16 1997, Enschede, The Netherlands, A.W.P. Bakkers (eds.), IOS Press, pp 48-76.

Schwirtz, M.H., Wijbrans, K.C.J., Bakkers, A.W.P., Hoogzaad, E.P., and Bruis, R. (1992a), *The Twente LINX backplane*, University of Twente, Enschede The Netherlands, 1992.

Schwirtz, M.H. (1992b), *Design and realization of a A/D, D/A converter card for the Twente LINX backplane*, B. Sc. Thesis, ref. Nr. 92R113 EL Control Laboratory, University of Twente, Enschede The Netherlands, 1992.

Sunter, J.P.E. (1994), *Allocation, Scheduling & Interfacing in Real-time Parallel Control Systems*, PhD. Thesis, University of Twente, Enschede The Netherlands, 1994.

Walker, C.P.H. (1996), *Hardware for transputing without transputers*, Proceedings WoTUG-19, "Parallel processing developments", March 31 – April 3 1996, Nottingham, United Kingdom, B. O'Neill (eds.), IOS Press, pp 1-10.