19.2 Frequency Compensation of an SOI Bipolar-CMOS-DMOS Car Audio PA

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The growth of in-car entertainment systems demands smart power devices, including audio power amplifiers. Despite the trend towards class-D systems, integrated class-AB amplifiers are still superior in terms of frequency response, integration level and ease of application. The market drive for lower distortion and higher stability demands good frequency compensation schemes. Still, to the best of our knowledge, no literature exists on frequency compensation of integrated MOS audio power amplifiers.

Audio amplifier design has similarities to general purpose opamp design. A large bandwidth is desired for low distortion, the load is unpredictable, and capacitive loads are especially problematic. Several publications [1-5] address this issue with frequency compensation schemes that are less fit for our purpose in the present form. All these techniques require compensation capacitors (C_m) that are much larger than the circuit parasitics, including the gate-source capacitance (C_{gs}) of the power transistor. In power amplifiers, however, the power transistors occupy most of the chip area, so $C_m >> C_{gs}$ is not feasible. Although $C_m < C_{gs}$ could still work, pole-splitting would be limited and the achievable unity-gain frequency (UGF) would be reduced. Furthermore, parallel g_m paths to the output [2-5] are difficult to combine with proper class-AB control, which is indispensable for audio power amplifiers because they can have a quiescent-to-maximum current ratio of 1:500.

We propose a modification to nested Miller compensation (NMC) [1] that allows us to achieve the same UGF with limited C_m as with large C_m. We can then use the parasitic gate-drain capacitance of the power transistors as C_m and only need a small extra compensation capacitance. This idea is inspired by [6] and is possible when we degenerate the gain of the penultimate stage, although we use more stages and a small, instead of very large, C_m.

Our starting point is NMC as shown in Fig. 19.2.1. The analysis focuses on the output impedance Z_o, as this gives valuable information about the stability for various loads, as well as an indication of the distortion. Since a common-source output stage is mandatory to get maximum output swing, the dominant source of distortion, the power transistor, can be modeled as a distortion current source in parallel with the output. Therefore, lowering the closed-loop output impedance at the same closed-loop gain also yields lower distortion. To get a simple expression for Z_o in Fig. 19.2.1, we neglect the direct contributions of C_{m3} and C_{m2}, which manifest themselves only at very high frequencies. Furthermore, we will ensure that $g_{m1}R_1 >> 1$ and $C_{m2} >> C_1$.

The crucial aspect of our solution is that we now increase g_{m2} while decreasing R_2 (keeping $g_{m2}R_2 = 1$ in our case). By increasing g_{m2} such that $g_{m2}/C_{m3} >> g_{m1}/C_{m2}$ (so that the UGF of the inner loop is much larger than the UGF of the outer loop), the expression for Z_o can be approximated with a Taylor expansion. The resulting Bode plot of Z_o is shown in Fig. 19.2.2. As a reference, the output impedance of a two-stage amplifier with NMC with the same limited C_m is plotted as a dashed line.

For high frequencies (region I), the output impedance is real, so for a small load capacitance (C_L) the opamp is stable. When C_L is increased, the plot of its impedance will cross the output impedance in an inductive region (II). The circuit is resonant at that frequency, leading to peaking in the frequency response. The ratio between the zero and pole that form the borders of region II determines how bad the worst-case peaking is. In our case, where $C_{m3} = C_{dg3} = 20$pF, $C_2 = C_{gs3} = 80$pF and $g_{m2}R_2 = 1$, the ratio is 5, leading to approximately 45° phase margin. Increasing C_L further, the system is more stable again (III), and only for larger C_L (IV) is the stability compromised. Note that the stability of a two-stage amplifier with NMC would already be compromised for C_L larger than indicated in Fig. 19.2.2, a significant factor $g_{m2}R_2(C_2 + C_{m3})/C_{m3}$ (= 5 in our case) lower. In conclusion, we see that the drawbacks of the limited Miller capacitance have been overcome.

One might be tempted to look at this structure as a simple way of driving the gates of the power transistors with a low-impedance source, a kind of resistive broadbanding. It is not that simple, however, because a smaller C_{m3} would then be favorable, as it limits the capacitive load seen by g_{m2}. Our analysis, however, shows that a smaller C_{m3} will actually decrease the phase margin for capacitive loads in Region II in Fig. 19.2.2.

For our purpose, the degenerated amplifier doesn't have enough gain in the audio band, so another gain path (with $g_{m4,5}$) is added in parallel to g_{m1}, dimensioned such that it adds gain (and phase shift) only below $g_{m1}/C_{m2} = 1$MHz (see Fig. 19.2.3). This technique also works with normal NMC, but it can be shown that due to the limited C_m, and consequently low UGF, the contribution would be marginal here.

The amplifier was realized in the Philips A-BCD2 process, an SOI BCD process with 1µm feature size. The chip is targeted as a 4×46W (4Ω, square wave) audio amplifier for automotive applications. Figure 19.2.4 shows the topology of one channel. The 1× gain, $g_{m2}R_2$, is realized by a source follower, which achieves $g_{m2}R_2 \approx 1$ in the frequency range of interest. To achieve a high value of g_{m2}, I_2 must be large, but we need a large I_2 anyway because of the high charge and discharge currents of the gate of M_3 during crossover and clipping. The load is driven by a bridge and a current-mode feedback topology ensures good common-mode stability.

The viability of the calculations and the design are demonstrated by measurements of the output impedance as shown in Fig. 19.2.5. Also, the amplifier is stable for any passive load with a capacitive component less than 50nF without the use of any external stabilizing network. THD+N is typically 0.005% at 1kHz with 10W of output power (Fig. 19.2.6), SNR is 108dB. Features like line driver mode, no-plop startup, standby, soft mute, load detection, and several protection features are all accessible by an I2C interface. A chip micrograph is shown in Fig. 19.2.7.

References:

[1] R. G. H. Eschauzier et al., “100-MHz 100-dB Operational Amplifier with Multipath Nested Miller Compensation Structure,” *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1709–1717, Dec., 1992.
[2] K. N. Leung et al., “Three-Stage Large Capacitive Load Amplifier with Damping-Factor-Control Frequency Compensation,” *IEEE J. Solid-State Circuits*, vol. 35, no. 2, pp. 221–230, Feb., 2000.
[3] H. Lee, P. K. T. Mok, “Active-Feedback Frequency-Compensation Technique for Low-Power Multistage Amplifiers,” *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 511-520, March, 2003.
[4] J. Ramos, M. Steyaert, “Positive Feedback Frequency Compensation for Low-Voltage Low-Power Three-Stage Amplifier,” *IEEE T. Circuits and Systems I,* vol. 51, no. 10, pp. 1967-74, Oct., 2004.
[5] F. You et al., “Multistage Amplifier Topologies with Nested G_m-C Compensation,” *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 2000-2011, Dec., 1997.
[6] R.J. Reay, G.T.A. Kovacs, “An Unconditionally Stable Two-Stage CMOS Amplifier,” *IEEE J. Solid-State Circuits*, vol. 30, no. 5, pp. 591-594, May, 1995.

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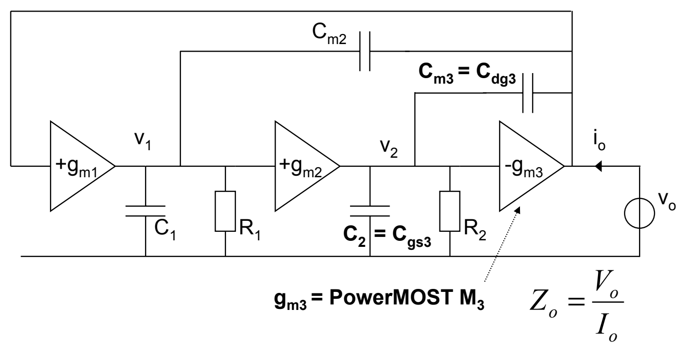


Figure 19.2.1: Nested Miller compensation.

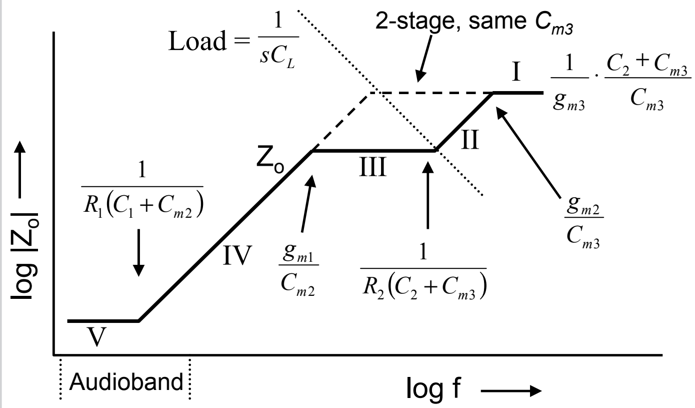
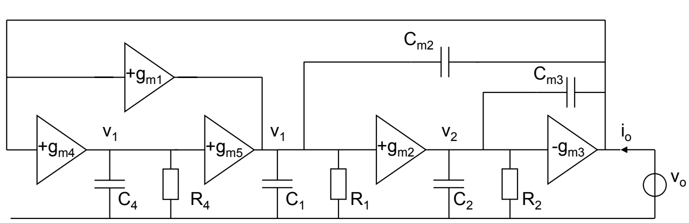


Figure 19.2.2: Z_o of Fig 19.2.1 and of two-stage NMC (dashed).



g_{m4}=30µ	g_{m1}=30µ	R_1=10M	g_{m2}=0.01	C_2=C_{gs3}=80p
C_4=15p	g_{m5}=30µ	C_1=2p	R_2=100	C_{m3}=C_{dg3}=20p
	R_4=10M		C_{m2}=5p	g_{m3}=0.2

Figure 19.2.3: Frequency compensation setup of one half bridge.

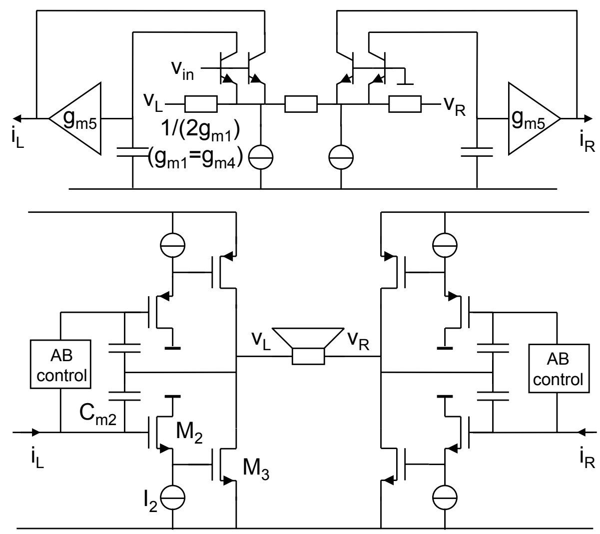


Figure 19.2.4: Basic topology of one channel.

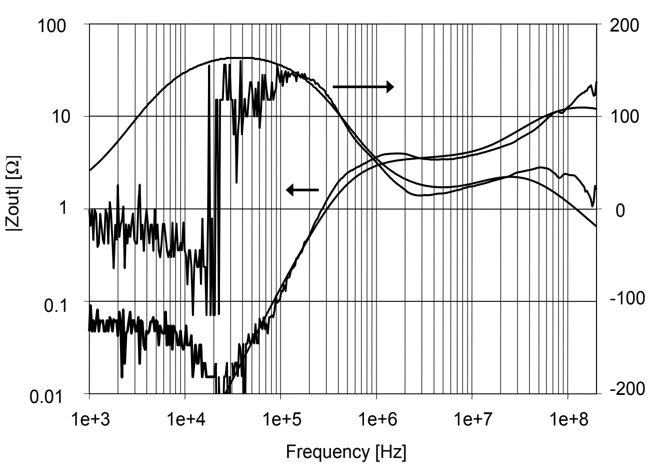


Figure 19.2.5: Z_o simulated (Figure 19.2.3) and measured (packaged product).

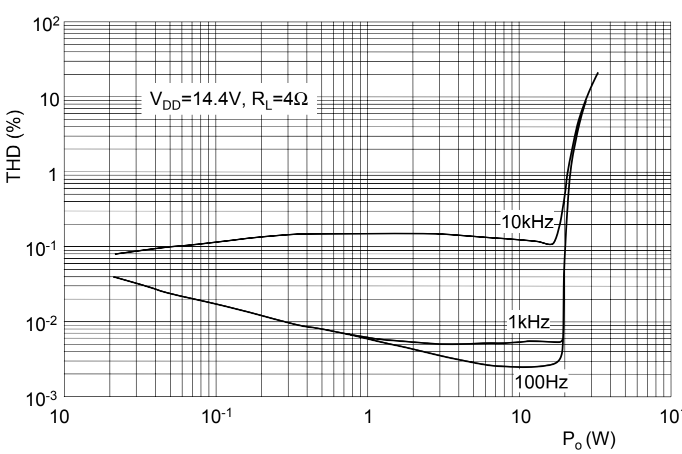


Figure 19.2.6: THD+N as a function of output power and frequency.

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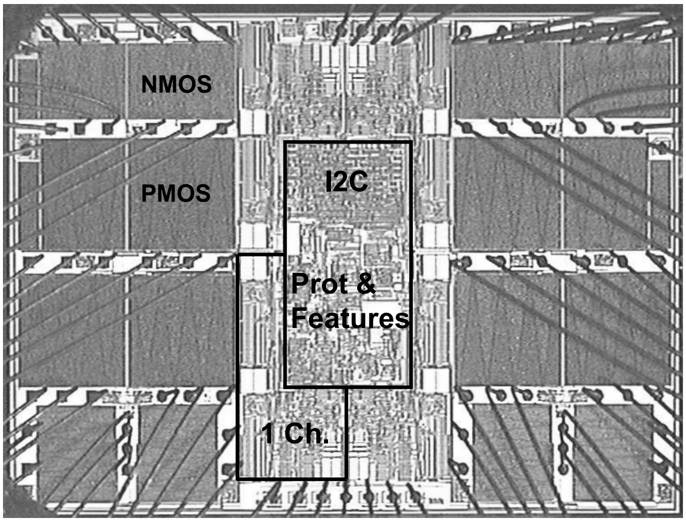

Figure 19.2.7: Chip micrograph.