7.2 Designing Outside Rail Constraints

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This paper discusses a number of significant items for analog design in current and future CMOS processes and a possible way to maintain performance.

A fundamental relation between SNR and required power consumption, including distortion and voltage headroom ΔV (eq.1) shows that the power consumption rises with lowered supply voltage [1].

$$P_{overhead} \propto kT\, f_{sig} SINAD^{7/6} \cdot \sqrt[3]{\frac{\alpha}{V_{DD}-\Delta V}} \cdot \frac{V_{DD}}{V_{DD}-\Delta V} \qquad (1)$$

However, at constant supply voltage the minimum power consumption decreases with newer CMOS generations. Lower V_T's result in lower ΔV while increased f_T-s result in greater linearity (directly or via feedback) and hence in lower α [1]. The simulation results for a typical buffer circuit in Fig. 7.2.1 illustrate these two. Clearly the constant V_{DD} trend is preferable.

Also second order effects in transistors change with CMOS generations and biasing conditions. E.g. the output impedance of transistors (impacting low-frequency gain-per-stage and harmonic drain-current content) depends on technology and voltage headroom. Figure 7.2.2 shows the 1st to 3rd harmonic current components of W/L=1/1 transistors in four technology nodes as functions of effective gate-source overdrive voltages, normalized w.r.t. the DC current (to eliminate transistor-width dependencies). Identical quiescent V_{DS} and voltage swing are assumed, while the curves are derived from non-linearly interpolated measurements. Again changing CMOS technology hardly changes performance.

If, however, the quiescent V_{DS} and the voltage swing are proportionally decreased with the nominal supply voltage, the harmonic content increases markedly with newer process generations. At the circuit level this is compensated for by e.g using (regulated) cascodes that have headroom limitations with decreasing supply voltages.

Gate leakage current [2], dependent on V_{GS} and gate size, is a relatively new constraint in CMOS design. The impact of gate leakage on an MOS transistor follows from its input impedance, consisting of the input capacitance and the "tunnel resistance". These have opposite area dependencies; consequently, an area independent f_{gate} is introduced:

$$f_{gate}(V_{DS},V_{GS}) = \frac{1}{2\pi c_{in} r_{tunnel}} \cong \frac{1.5\cdot 10^{16}\cdot V_{GS}^2}{\exp(13.6\cdot t_{ox})} \exp(t_{ox} V_{gs}) \quad t_{ox}\, in[nm] \qquad (2)$$

For signal frequencies higher than f_{gate} the input impedance is capacitive; below f_{gate} it is resistive. Figure 7.2.3 shows f_{gate} as derived from measurement results, and, using (2), shows the fit for three technologies. Due to gate-leakage, MOS capacitances cannot be applied for certain low-frequency applications like PLL loop filters and hold circuits. Other effects of gate-leakage include input bias currents, gate-leakage-mismatch and shot-noise [3].

Although from a fundamental point-of-view mismatch does not require any power consumption, it is a major challenge to practical implementation. Gate-leakage spread is an extra spread-source and places an upper bound on the area to be used on decreasing mismatch. Initial measurements on gate-current matching indicate that, excluding defect-like outliers, it is proportional to the gate-current level with a proportionality constant $\sigma_{Igs}/Igs = X_{ig} \cong 3\%$, and decreases with the square of gate area.

Incorporating the area-dependency of gate-leakage and noting that the V_T-spread factor A_{vt} saturates at thin oxides around 2-3mVμm [4] this yields an area A_{max} [μm²] for which the total spread is minimal (as function of t_{ox}):

$$\sigma_{total}^2 = \left(\frac{g_m A_{vt}}{\sqrt{WL}}\right)^2 + \left(\frac{X_{igs}}{\sqrt{WL}} I_{GS}\right)^2 \text{ and } \sigma_{vgs,min} = \frac{4mV}{\sqrt{A_{max}}} \qquad (3)$$

For 180nm and 120nm CMOS this A_{max} is very large. However for the 90nm and 65nm (estimated) generations this yields a maximum usable area of 10^4μm² and 10^3μm². Here gate-leakage mismatch is a significant effect, requiring active mismatch cancellation techniques.

Summarizing: transistors get better with newer technology. Only operation at nominal (digital-dictated) supply voltages degrades analog performance and gate-currents yield new limitations. Operating analog circuits outside nominal supply rails solves the low-supply drawback of newer technologies. However care need be taken with respect to lifetime issues of hot-carrier degradation due to high lateral electrical fields and gate-oxide degradation due to high oxide-voltages. Both effects are minimized by a suitable limitation of terminal-pair voltages.

For circuits operating at "high" supply voltages then a number of robust "high voltage tolerant" transistors are used. Figure 7.2.4 shows three examples derived from high-voltage I/O circuits [5]. These "HV-transistors" enable direct re-use of most older designs with supply voltages corresponding to the original design. The simplest way is to use the thick oxide transistor (Fig. 7.2.4c) that is comparable to the 2-generations-ago standard transistor. However, in order to benefit from technology scaling, the use of smaller devices, as in Fig. 7.2.4a and 7.2.4b, is preferable to Fig. 7.2.4c. Transistors for which matching, 1/f noise or output impedance is critical may be realized with the compound structures in Fig. 7.2.4a and b. The disadvantage of these structures is that a suitable cascode voltage must be provided and be present during powering-up. This is realized using internal cascode-voltage generators at the cost of circuit complexity. If only a small part of a system is critical, one may choose to generate high-voltage on-chip using charge pumps.

Figure 7.2.5 lists the conclusions of a comparison of analog properties. In the comparison, the three topologies handle the same maximum drain-source voltages and assume equal drain-current, V_{gs}-V_t, and length for the lower device. In conclusion Fig. 7.2.4a is always preferred to 7.2.4b. Compared to Fig. 7.2.4c, Fig. 7.2.4a has higher R_{out}, lower 1/f noise, better matching, but lower f_t, higher circuit complexity and higher gate current. For applications such as a current source, the circuit of Fig. 7.2.4a is preferred, while for high-speed gate-drain transfers Fig. 7.2.4c is preferred. Note that if the required voltage drop at the output terminals of Fig. 7.2.4a is reduced by the rest of the circuit, then the upper cascode(s) can be removed. Then the circuit in Fig. 7.2.4c has virtually no speed advantage. (See Fig. 7.2.6.)

In conclusion: analog circuits can benefit from scaling CMOS technologies if the supply voltages are not scaled unlike in digital couterparts. High-voltage techniques are then needed; Fig. 7.2.4 shows some ways to create high-voltage tolerant compound transistors.

References:

[1] A.J. Annema, "Analog Circuit Performance and Process Scaling," *IEEE Transactions of Circuits and Systems II*, vol. 46, pp. 711-725, 1999.
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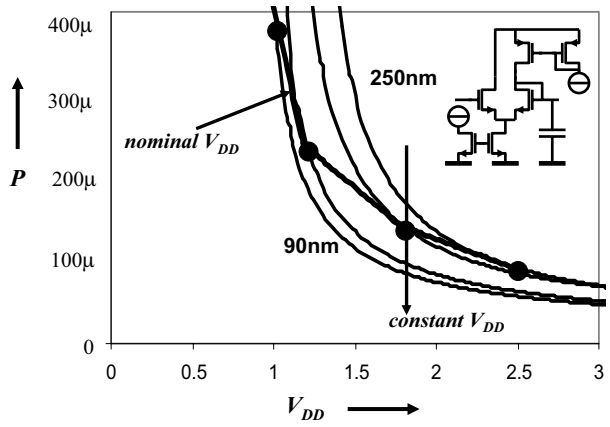

Figure 7.2.1: Simulated typical Vdd-P relation for analog circuits: fixed topology, optimized settings, 60dB SINAD @ 15MHz; in 90, 120, 180 and 250nm CMOS. Reliability issues ignored for comparison reasons.

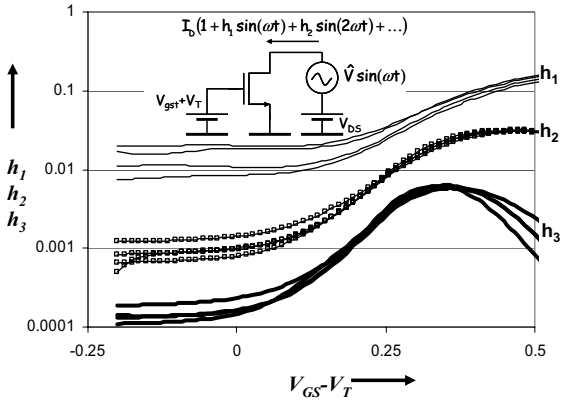

Figure 7.2.2: Simple current-source: 1st (thin), 2nd (boxes) and 3rd (thick) harmonic current component normalized wrt DC current for a 90nm, 120nm, 180nm and 250nm process, fixed VDS and signal swing over processes.

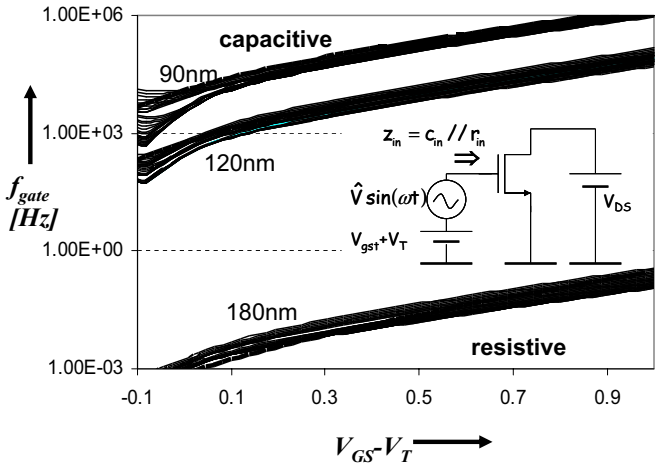

Figure 7.2.3: fgate as function of VGST, for various W/L (minimum/10 … 10/10 and VDS; for 90nm, 120nm and 180nm technologies; fat line corresponds to equation.

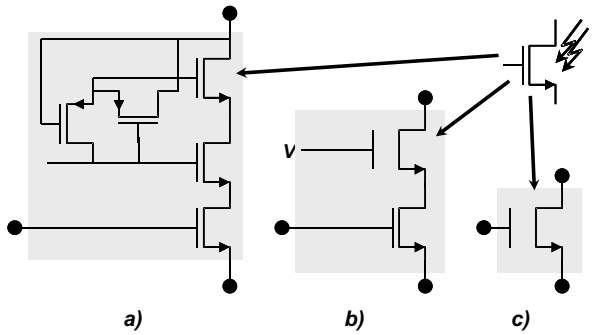

Figure 7.2.4: Ways to implement high-voltage tolerant transistors in standard CMOS: a) retractable cascode b) (thick-oxide) cascode c) thick-oxide transitor

	figure 4a	figure 4b	figure 4c
Drain current	I_D	←	←
V_{GS}-V_T	V_{GT}	←	←
Current factor	$\beta\square$ $\beta\square$ $\beta\square$	- $½\beta\square$ $\beta\square$	- - $½\beta\square$
Transistor lengths	L_{min} L_{min} L	- $2L_{min}$ L	- - L
gm	$2I_D/V_{GT}$	←	←
R_{out}	$\sim Rds_L * \mu_{cas}{}^2$	$\sim Rds_L * \mu_{cas}$	$\sim Rds_L$
Thermal noise	$i_n^2 = \frac{8}{3}kTgm$	←	←
Flicker noise	$i_{fl}^2 = \frac{K \cdot I_D}{C_{ox} L^2 \cdot f}$	←	←*2
Threshold mismatch[1]	$\sigma_{vgs} \approx \frac{A_{VT}}{\sqrt{WL}}$	←	← * $\sqrt{0.5}$ = $\sqrt{2}$
$f_t/f_{t,max}{}^2$ @ L=4L_{min} @L=2L_{min}	*0.04* *0.08*	*0.03* *0.05*	*0.06* *0.25*

Figure 7.2.5: Comparison of some analog parameters for structures in figure 4; 1) depending on classical or saturating A_{VT}; 2) normalized wrt f_t for a single minimum-length thin-oxide transistor.

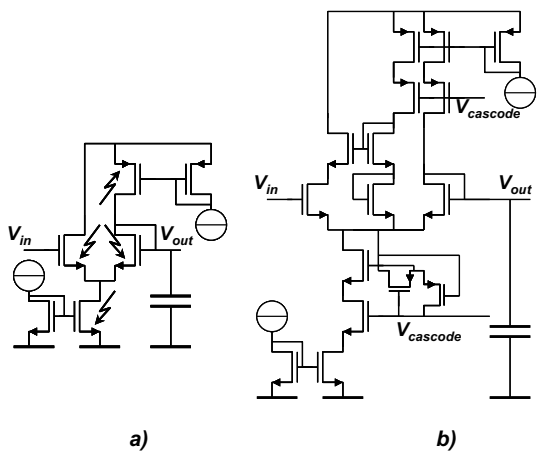

Figure 7.2.6: Example circuit usable at "high" supply voltages: a) single transistors replaced by high-voltage tolerant transistors b) simple implementation.

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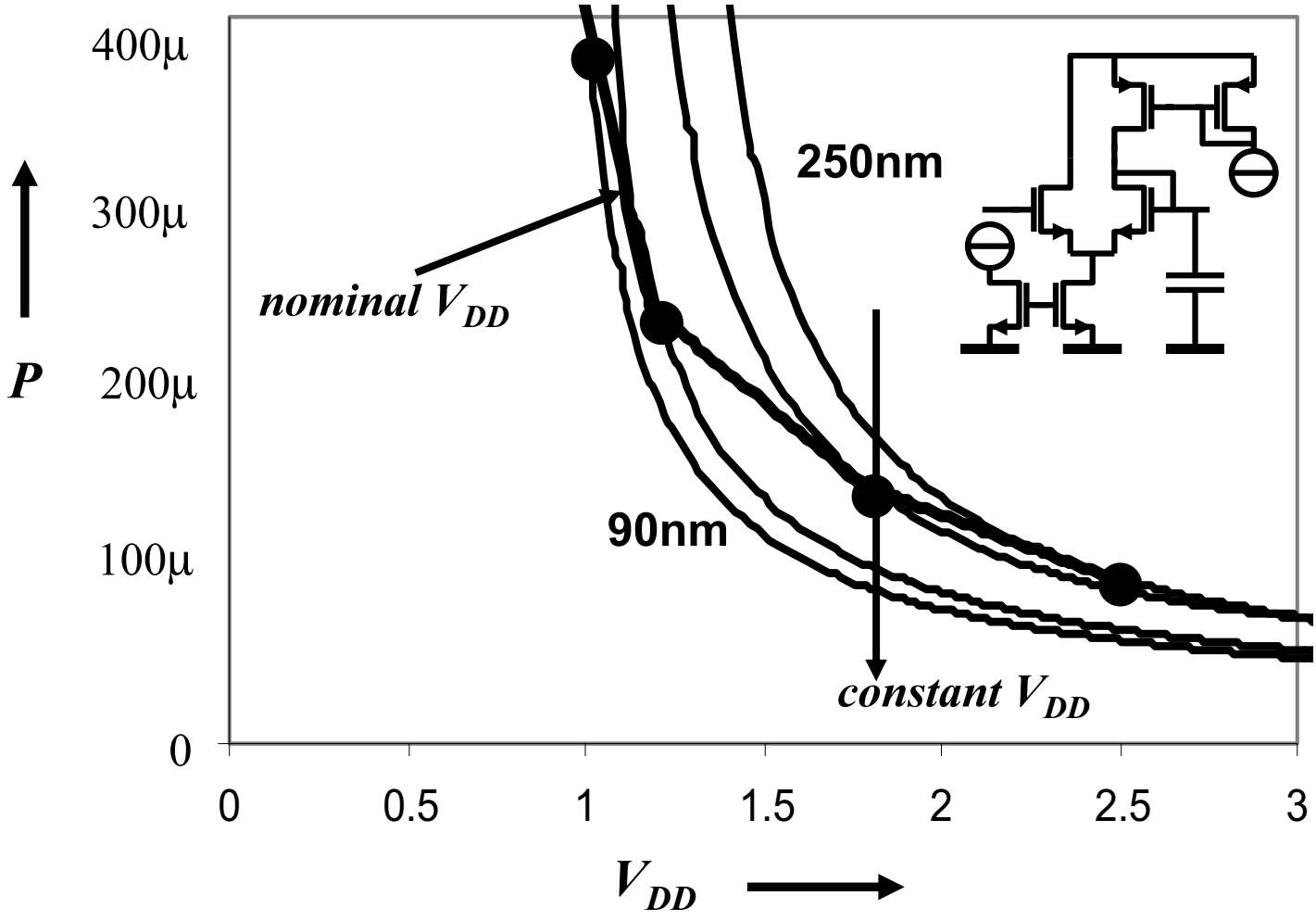

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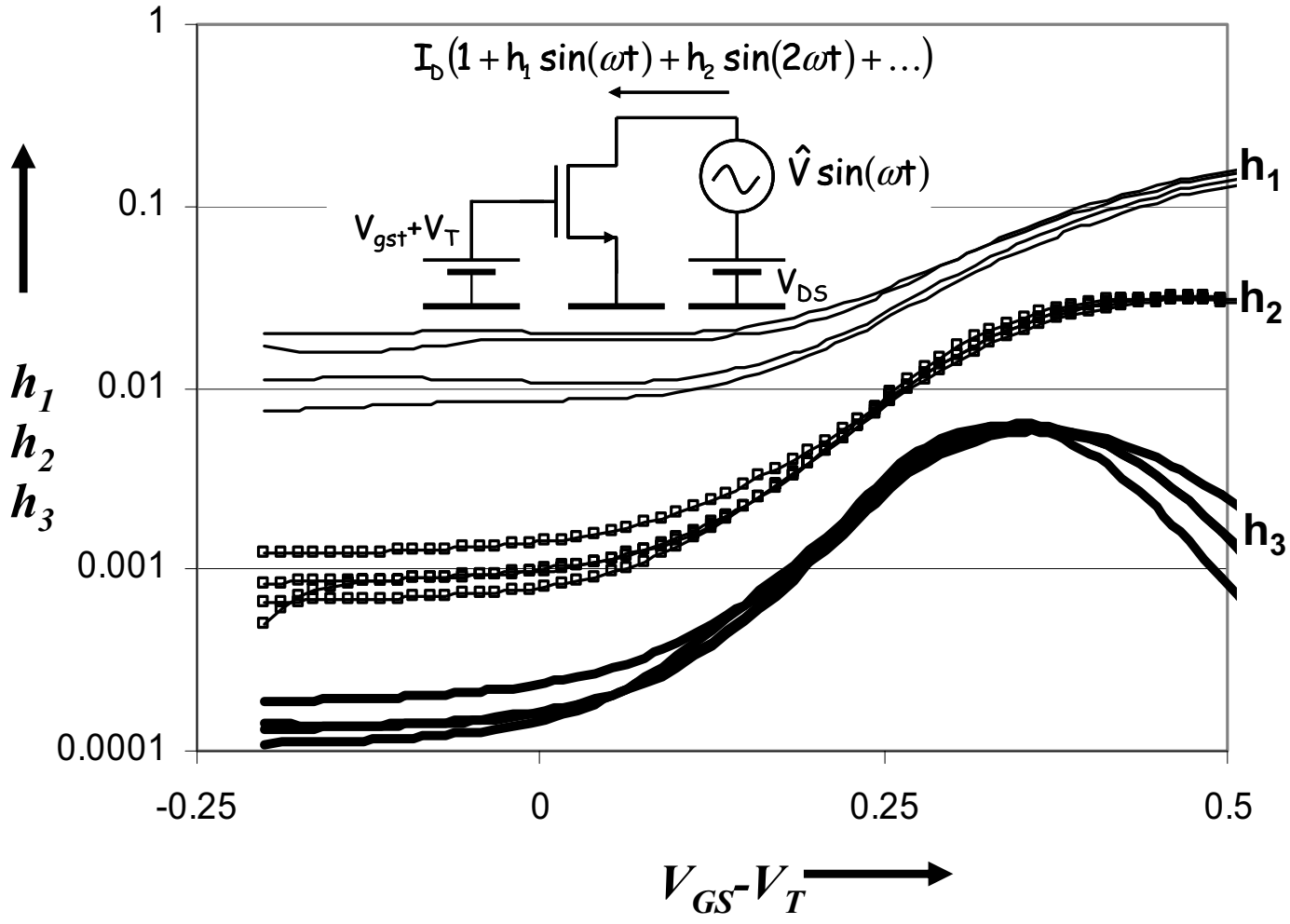

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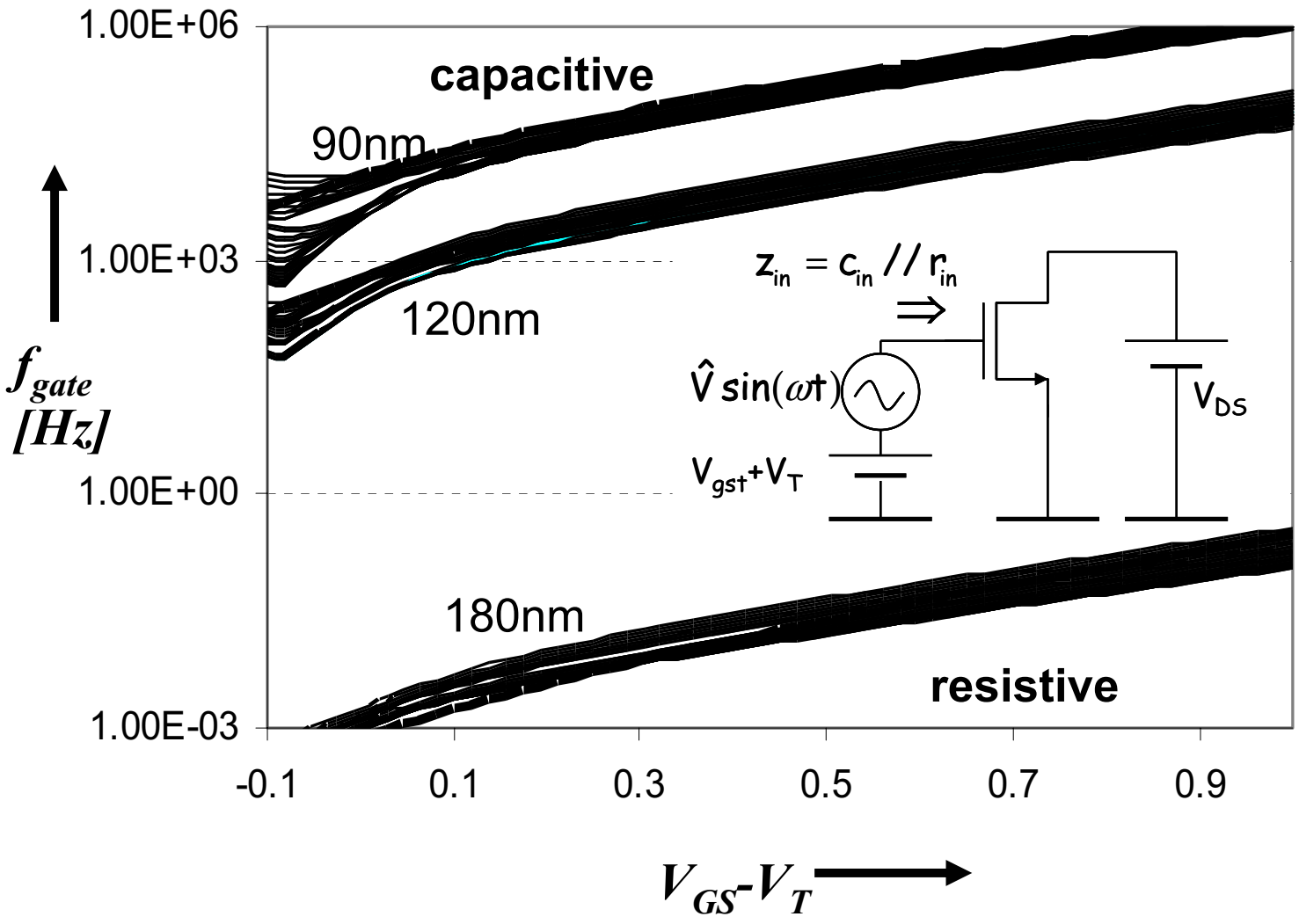

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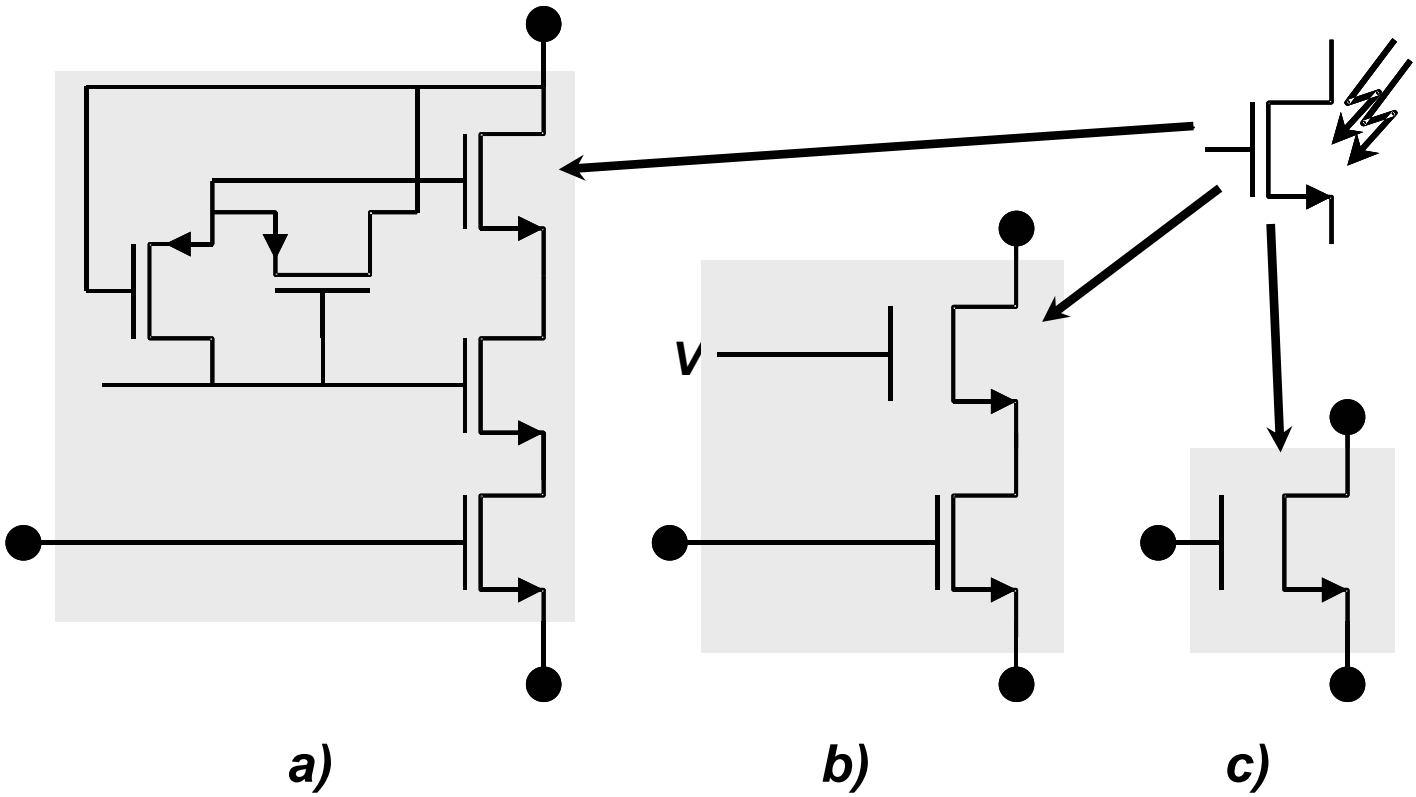

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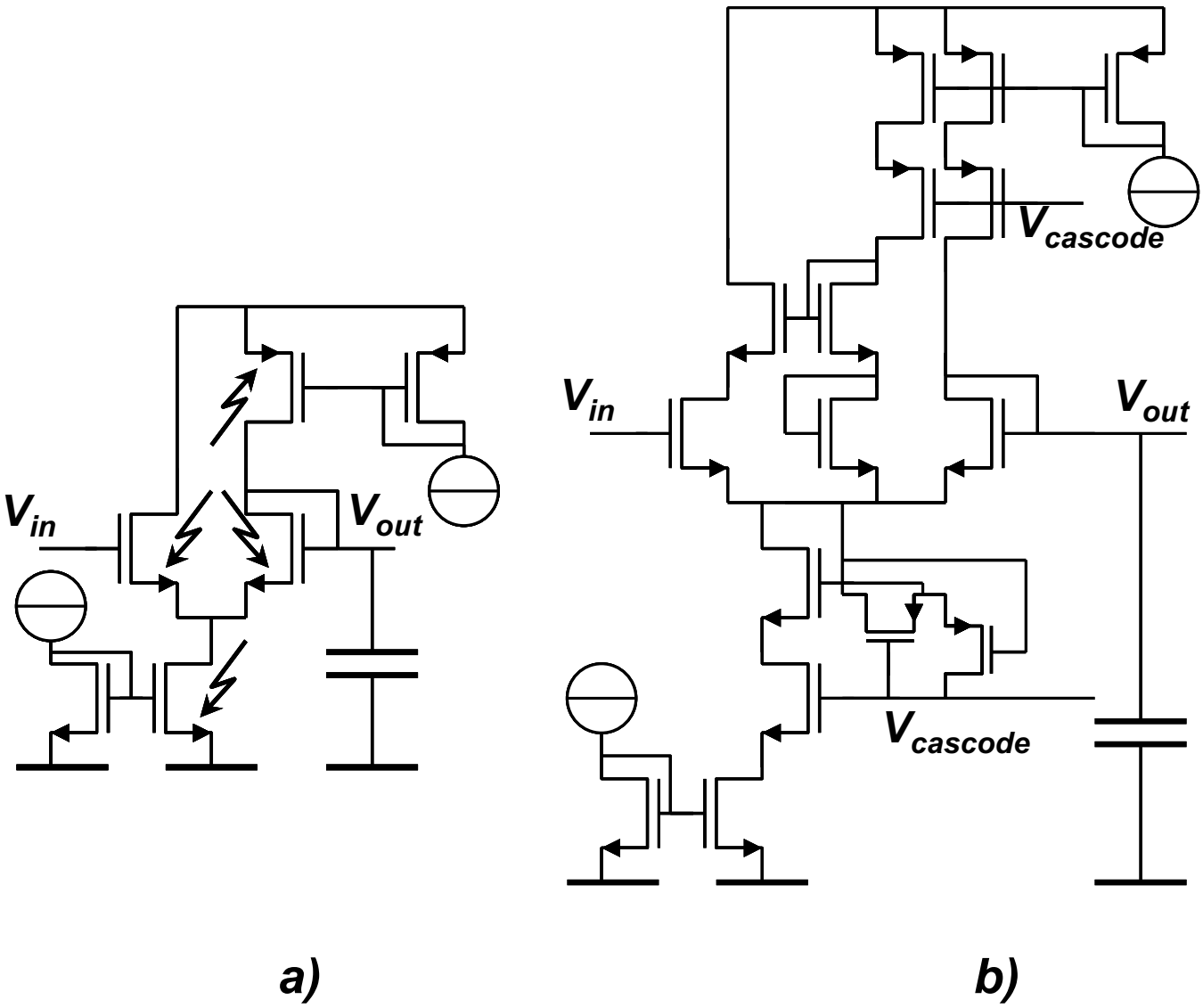

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