A 1.0-to-2.5 GHz Beamforming Receiver with Constant-G_m Vector Modulator Consuming < 9mW per Antenna Element in 65nm CMOS

M.C.M. Soer[1], E.A.M. Klumperink[1], B. Nauta[1], F.E. van Vliet[12]

[1] University of Twente, Enschede, Netherlands

[2] TNO, The Hague, Netherlands

Beamforming phased-array receivers aim to increase receiver sensitivity and reject interferers in the spatial domain [1]. A receiver with programmable phase shift and high linearity is crucial to cope with interference. Switched-capacitor vector modulators can provide adequate phase shift and linearity [3,4], but so far, at the cost of a high power consumption. As power consumption increases linearly with the number of antenna elements, it is one of the bottlenecks hindering commercialization of beamforming. In this paper, we demonstrate several design techniques on architectural and circuit level, to reduce the power consumption per element, while still achieving competitive Spurious Free Dynamic Range (SFDR).

A vector modulator creates a weighted sum of two 90 degrees out-of-phase signals, I and Q, to generate an output with adjustable phase and gain. In the top part of Fig. 1, the classical Cartesian vector modulator is depicted, with separate, digitally controllable transconductors at baseband for I and Q, and current summing. Each constellation point in the phasor diagram is a vector summation of the weighted I and Q vector. By allowing smaller steps in the tunable Gm, a finer resolution in the phasor diagram can be reached, while the polarity switch in I and Q allows for reaching all four quadrants. The phasors for the actual phase shifter are picked as those lying close to a circle. In this architecture, the total Gm varies with the applied phase shift, so the output impedance will vary with the phase shifter setting. We propose a constant Gm vector modulator with fixed transconductances, which are shared *between* I and Q, as is shown on the bottom of Fig. 1. The transconductances are binary weighted and the output is a summation of binary weighted vectors. The reconfiguration switches control the orientation of each of these vectors, along the I+/I-/Q+ or Q- axis. The successive phasor diagrams show how the number of phase points grows as a function of the number of transconductances. More resolution is achieved by adding more, increasingly smaller, transconductances. If N is the number of binary weighted transconductors, a 2^N by 2^N rectangular grid of

points in the phasor diagram can be made. Similar to the traditional Cartesian scheme, a rectangular constellation is generated (a Cartesian modulator has extra points on the axis, corresponding to disabled Gm's), but rotated by 45 degrees. This rotation of the constellation has no impact on the beamforming, since phase *differences* between antennas are required. Since now the total Gm is constant, the impedance on the output are also constant. We will show that this scheme is better suited for our architecture.

With the concept of a constant-Gm vector modulator in mind, we propose the Zero-IF beamforming receiver architecture in Fig. 2. Compared to Fig. 1, the transconductance has now been placed at RF before the I/Q generation done by the mixer [1]. The reconfiguration switches are positioned at baseband, so that their parasitic capacitance can be easily absorbed in the baseband capacitors. This N=4 design (16x16 constellation points) uses thermometer coded unit slices to improve matching, in groups of 1,2,4 and 8, for a total of 15 slices. A slice is worked out in detail in the circuit diagram in Fig. 3. A passive 25% duty cycle current-mixer converts the RF transconductor current to zero-IF, while also providing single to differential conversion to I+, I-, Q+ and Q- (allowing for image rejection). Note that good 1/f noise can be expected as the transconductor operates at RF and passive mixers are used. As the inverter transconductor amplifies the RF signal first, the impedance level seen by the passive mixer can be much higher than the 50Ω antenna impedance. Therefore, compared to a mixer-first design [3,4], the mixer switches can be smaller, resulting in a large reduction in dynamic power consumption in the clocks. It's important to note that the current of the transconductor is always steered to only one of the outputs and the baseband capacitors retain their voltage when the current is routed to another path. If the transconductance were to be implemented in baseband instead of RF, each of the four outputs would needs its own, resulting in four times the total Gm.

The inverter transconductor in Fig. 3 is self-biased, and consists of standard-Vt transistors, but is supplied with a low 1.0 V supply voltage. This biases the transistors in moderate inversion for a better transconductance/current ratio at the cost of some increased capacitive parasitics. Impedance matching is realized by the bias resistor without extra static power consumption. The passive mixer upconverts the lowpass filtering in baseband, to a bandpass filtering on the inverter output node. This lowers the out-of-band RF voltage swing on the inverter output node, improving out-of-band linearity and compression.

The RF input of the mixer is AC coupled and biased at 0V. Full-swing inverters directly drive the mixer gates without any AC coupling or bootstrap circuits that would otherwise increase dynamic power consumption. Moreover, the AC coupling at RF helps in filtering IM2 products of closely spaced interferers which could otherwise potentially feed through the mixer to baseband. Conveniently, the element summing required for beamforming is automatically achieved by connecting the element outputs to shared capacitors [3]. The baseband bandwidth is defined by the output resistance of the transconductor (Rout), the baseband capacitance and the mixer duty cycle [5]. Due to the constant Gm principle, the output resistance is constant, resulting in a well-defined bandwidth. Moreover, the voltage swing at the outputs of the inverters is also constant, resulting in a constant input impedance of the IC. This prevents phase shifter dependent gain errors caused by a change in input matching, so that no calibration is required (in contrast to [1]) and the resolution of the vector modulator is optimally used.

The 4-element beamforming receiver was implemented in 65nm CMOS (see Fig. 7). The measured phase shifter constellation is plotted in Fig. 4. Also, phase and gain errors respective to uniform, constant amplitude phase steps are shown. These errors are mostly due to the mapping of the ideal phase shifts to a quantized constellation with a finite number of points. The measured gain, Fig. 5 top, of 12 dB falls off by 1 dB in an RF bandwidth from 1.0 to 2.5 GHz. Over this frequency range, the S11 matching is better than -10dB. The NF of 6 dB fits to simulation and is constant over the phase shifter settings. The in/out-of-band input-referred IP3 and 1 dB compression point are plotted in Fig. 5. The baseband capacitors are digitally tunable and can change the baseband bandwidth from 30 to 300 MHz. In this figure, the bandwidth was set to 30 MHz and the increase in out-of-band linearity is clearly visible in the measurement. In/out-of-band IIP2 was measured to be >52 dBm.

Figure 6 shows a comparison table with high SFDR low-GHz beamforming receivers. Only [3] achieves higher SFDR (but for 13dB lower gain), while its phase shifter resolution is low. In comparison to [2,4], the presented receiver achieves similar or better SFDR, at a significantly lower power consumption of 6.5-to-9 mW per element for 1.0-to-2.5GHz.

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Captions:

Figure 1: Traditional Cartesian (top) and proposed Constant Gm (bottom) vector modulator, example for N=3.

Figure 2: Architecture of the 4-element beamforming receiver.

Figure 3: Circuit diagram of a vector modulator slice.

Figure 4: Measured phase shifter constellation and phase/gain errors.

Figure 5: Measured single-element gain, NF (top), IIP3, compression point (bottom) and chip power consumption (top).

Figure 6: Comparison table.

Figure 7: Chip micrograph.

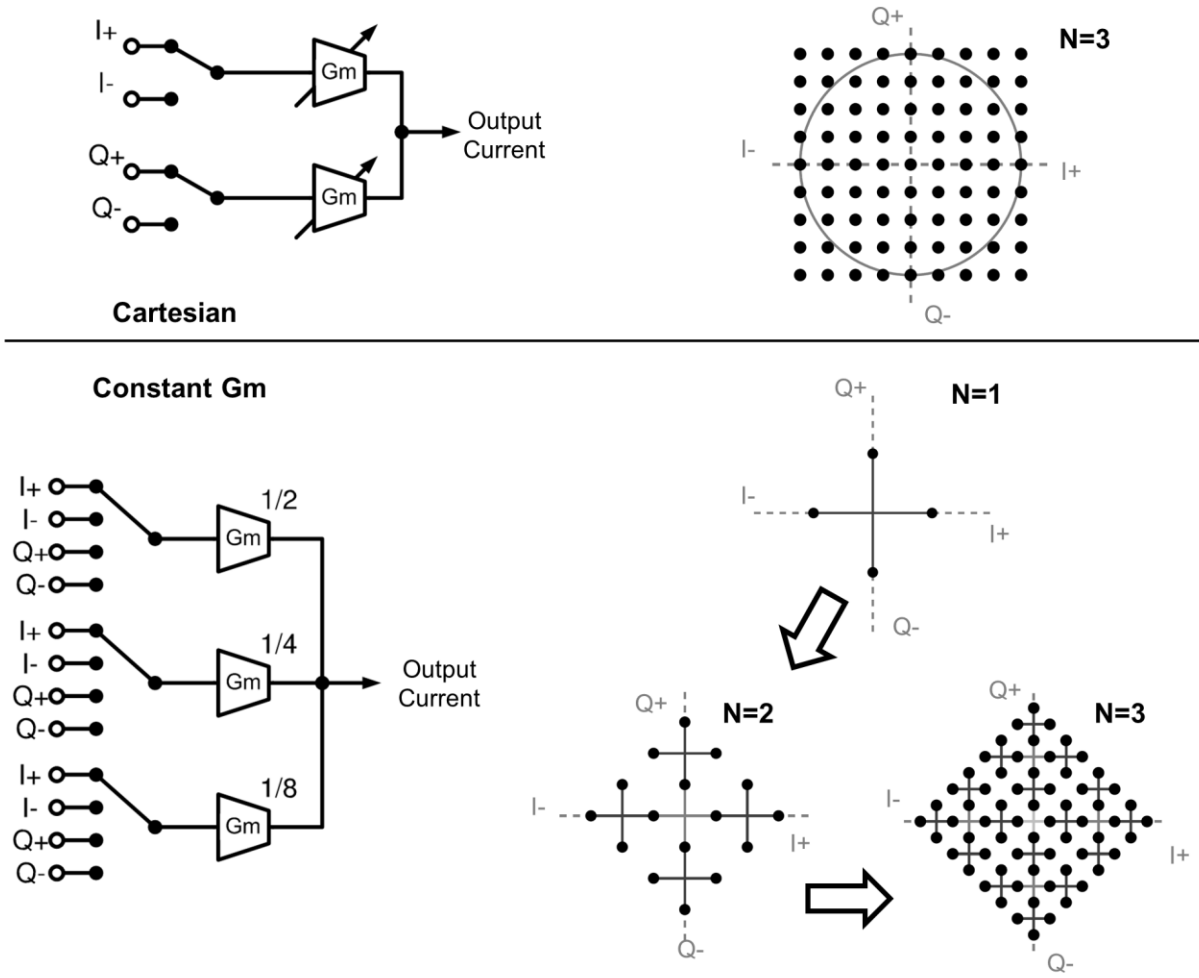

Figure 1: Traditional Cartesian (top) and proposed Constant Gm (bottom) vector modulator, example for N=3.

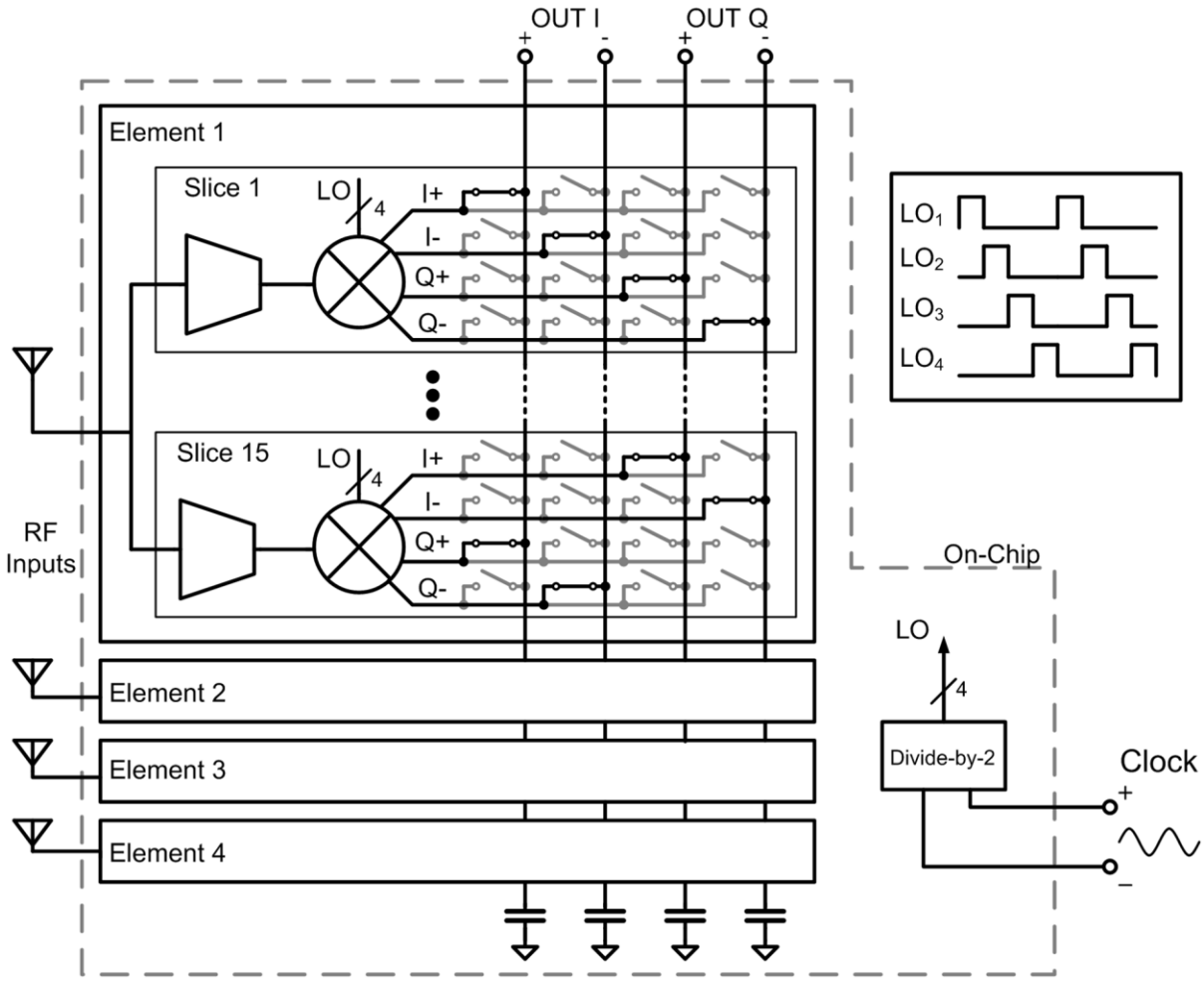

Figure 2: Architecture of the 4-element beamforming receiver.

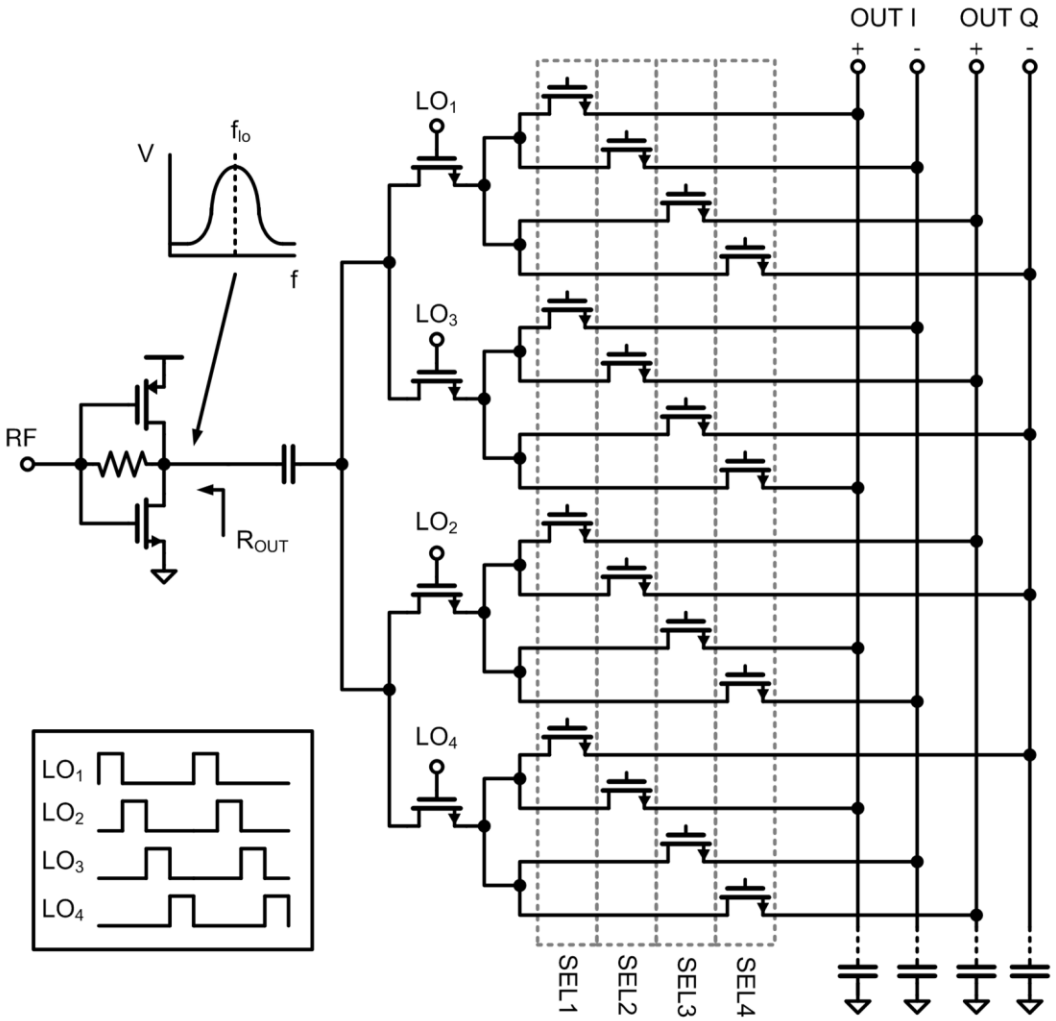

Figure 3: Circuit diagram of a vector modulator slice.

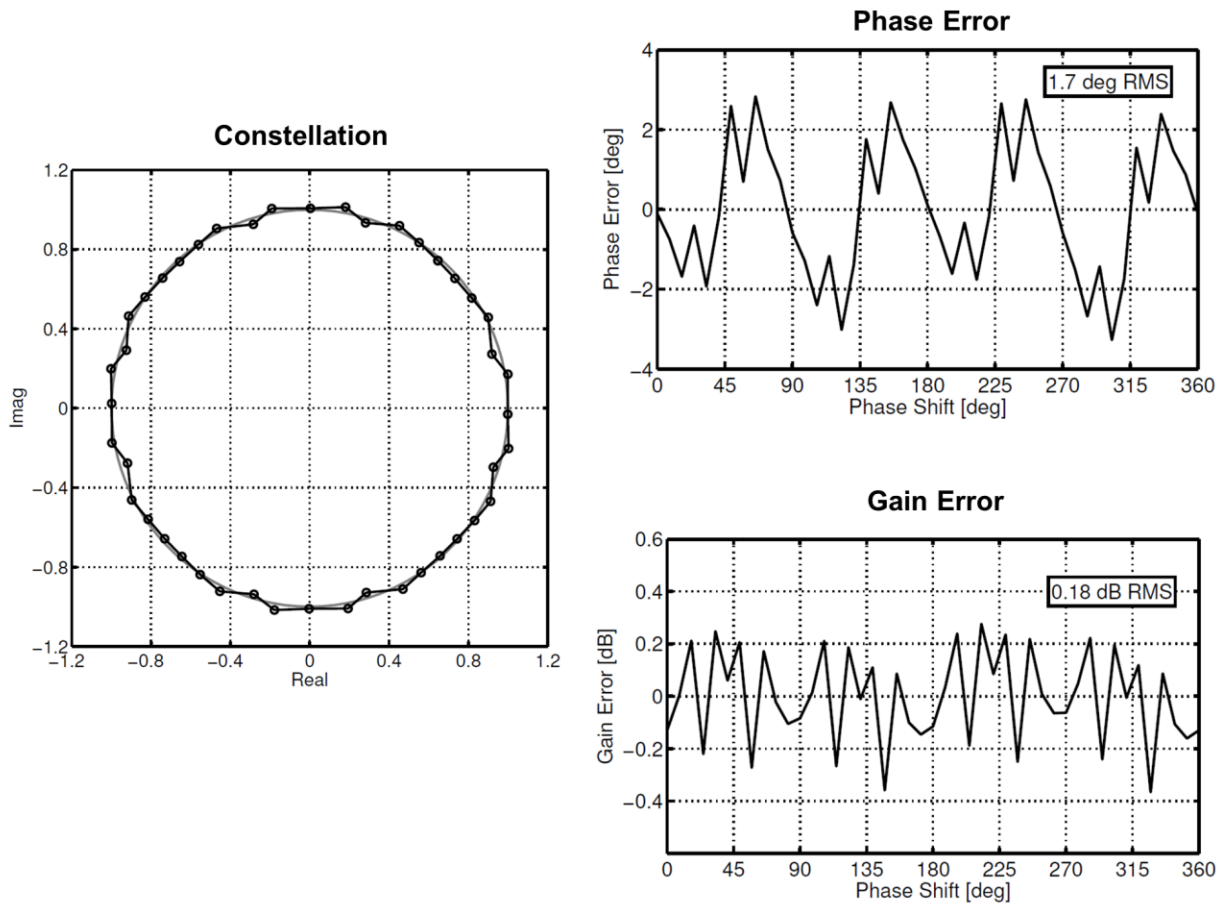

Figure 4: Measured phase shifter constellation and phase/gain errors.

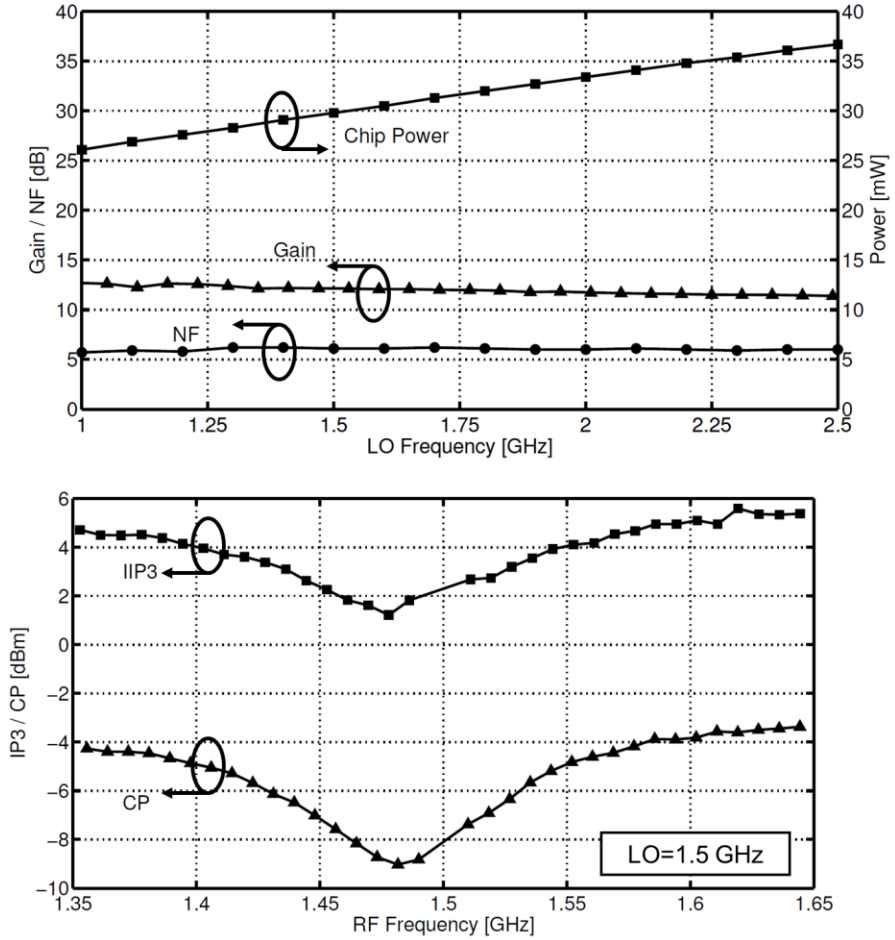

Figure 5: Measured single-element gain, NF (top), IIP3, compression point (bottom) and chip power consumption (top).

		[1]	[2]	[3]	[4]	This Work	
Technology		90nm	90nm	65nm	65nm	65nm	
Active area		1.3 [a]	1.4 [a]	0.97	0.18	0.20	mm^2
Supply voltage		1.4	1.2	1.2	1.0 - 1.2	1.0	V
RF frequency band		5.0	4.0	0.6 - 3.6	1.5 – 5.0	1.0 – 2.5	GHz
Power consumption		140	166	68 – 195	65 – 168	26 - 36	mW
Array elements		4	4	4	4	4	
Single Element Performance:	@		4.0	2.0	3.0	1.5	GHz
Gain		N/A	15	-1	-6	12	dB
Noise figure		N/A	13	4 [c]	18	6	dB
Compression point	in-band	N/A	N/A	-5	2	-9	dBm
	out-of-band			10	N/A	-3	
IIP3	in-band	N/A	2	6	13	1	dBm
	out-of-band			N/A	N/A	5	
In-band SFDR in 1MHz BW		N/A	69	77	73	73	dB
# Phase shifter steps		N/A	32	8	32	44	
Phase error (RMS)		N/A	N/A	N/A	2.0	1.7	deg
Amplitude error (RMS)		N/A	N/A	N/A	0.2	0.18	dB
Vector modulator EVM		N/A	2 [b]	N/A	4	4	%

[a] Estimated from chip photo.
[b] After calibration of the LO phases.
[c] Degraded by 2 dB for 4 elements, due to correlated noise.

Figure 6: Comparison table.

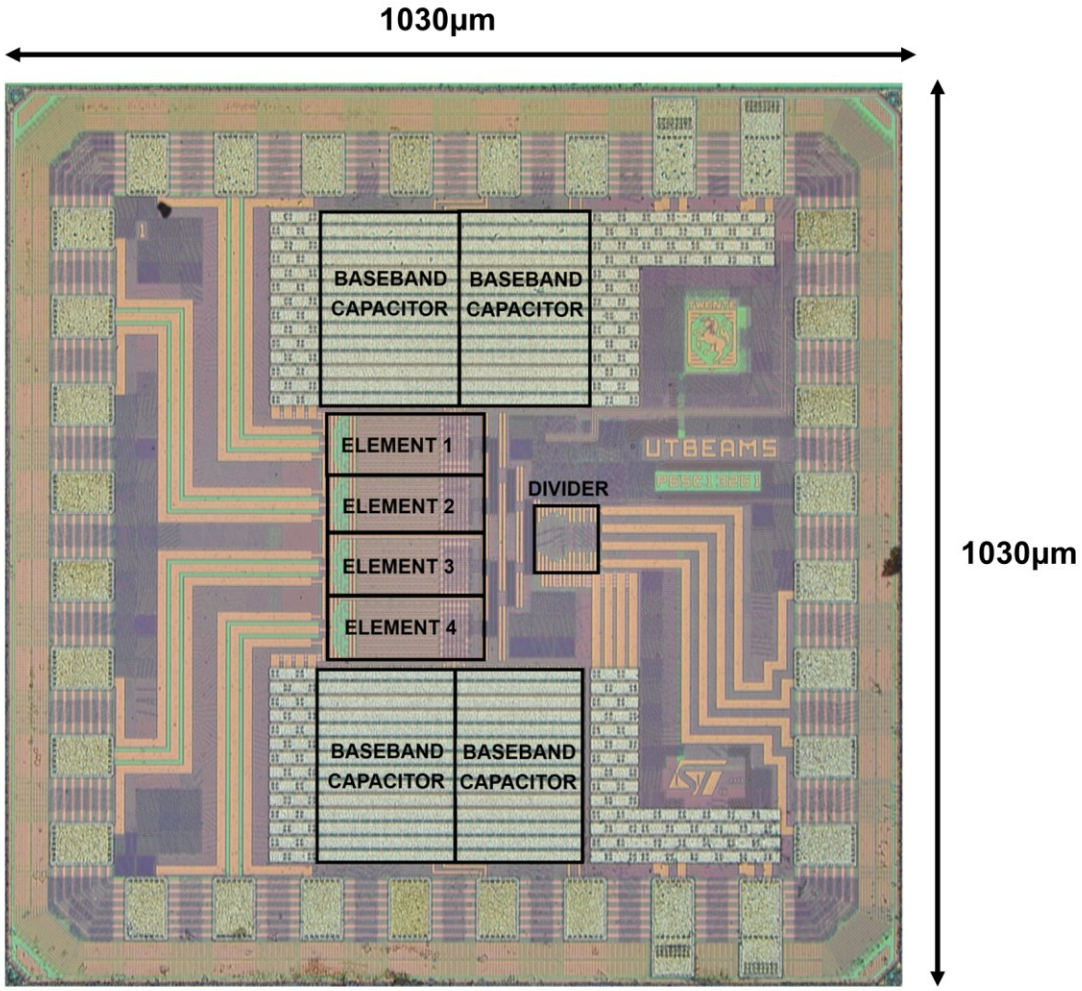

Figure 7: Chip micrograph.