Low-cost Multi-channel Underwater Acoustic Signal Processing Testbed

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***Abstract*—Current systems for multi-channel underwater signal processing suffer from a tied relation between the hardware and physical layer software or require a large amount of engineering work. To provide a low-cost, small form factor and flexible solution, this work presents a multi-channel testbed consisting of an off-the-shelf FPGA board and a simple expansion board. Nonetheless, the proposed testbed provides the flexibility and processing power to evaluate novel multi-channel physical layer algorithms.**

***Index Terms*—underwater communication; phased arrays; Field Programmable Gate Arrays (FPGAs)**

I. Introduction

A growing interest in underwater monitoring systems leads to an increasing amount of research focused on underwater communication techniques. Envisioned is a course-grained monitoring architecture consisting of multiple sensor nodes operating in an area of two square kilometer. To evaluate novel physical layer algorithms for these sensor nodes, a testbed is built as a means to speed up the development of the final sensor nodes.

Underwater communication (mainly) uses acoustic pressure waves for communication. Challenging channel characteristics are low propagation speed, frequency dependent attenuation and time-varying multipath propagation [1]. To compensate for these channel effects different types of temporal and spatial equalization, multi-carrier modulation and spread spectrum techniques can be employed.

Evaluation of physical layer algorithms for acoustic underwater communication requires a flexible hardware setup. This work presents an underwater testbed consisting of an (up to eight element) array connected to an off-the-shelf FPGA board via an easy to build extension board. The use of a readily available FPGA board reduces the amount of engineering work before any practical underwater experiment can be performed. Nonetheless, the testbed provides enough flexibility to evaluate different types of equalization and modulation techniques.

A simplified schematic of the complete multi-channel underwater testbed can be seen in Figure 1. Acoustic pressure waves are converted to voltages by piezoelectric underwater transducers. After amplification and low-pass filtering all analog signals are digitized synchronously and copied to the on-board memory of the FPGA board. Currently, the on-board memory content is copied to a PC for further analysis.

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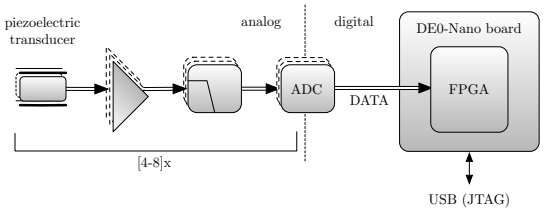

Fig. 1. Overview of the multi-channel underwater testbed.

Related multi-channel systems for underwater acoustic processing are discussed in Section II. Design decisions during construction of the testbed are based upon the characteristics of underwater acoustic propagation and phased array processing theory. Therefore, these topics and their implications on the hardware design are discussed in Sections III and IV. An overview of the complete hardware design is given in Section V. Underwater experiments were performed to verify the functionality of the testbed. These experiments are discussed in Section VI. An overview of the most significant results and directions for future work can be found in Section VII.

II. Related work

We have found two other systems that are related to our multi-channel testbed: the Woods Hole Oceanographic Institution (WHOI) Micro-modem and the reconfigurable Modem (rModem) from the Massachusetts Institute of Technology (MIT) [2] [3]. Although both systems are capable of multi-channel signal reception, they are primarily designed to provide a means for rapid testing and development of algorithms higher up the OSI stack.

The Micro-modem is an autonomous modem to build an underwater (wireless) communication network. The main processing board of the Micro-modem uses a fixed-point DSP. For Phase-Shift Keying (PSK) based communication, as well as multi-channel signal reception, separate expansion boards are available. The main disadvantage of the Micro-modem is the tied relation between the physical level software implementation and the hardware itself. This obstacle triggered MIT to design their so-called rModem. The rModem is a small form factor mainboard that uses both an FPGA and a DSP for processing. The board has four configurable input and output channels. Although the rModem is a good alternative for the Micro-modem, it is not available off-the-shelf.

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In contrast to the Micro-modem and the rModem our testbed uses an off-the-shelf FPGA (main) board. Our testbed is by no means an autonomous multi-channel modem. However, it provides a large amount of processing power and enables full control of the raw datastreams from the transducers. To test novel physical layer algorithms in real time or offline, this can be regarded as a necessity.

III. Underwater acoustic propagation

An important property of the aforementioned characteristics of underwater communication channels is the frequency dependent attenuation. This property results in a dependence between the desired distance and the upper frequency limit of the useful bandwidth. The lower frequency limit of the useful bandwidth is the consequence of colored ambient noise.

In [4], Stojanovic discusses the Attenuation $\times$ Noise (AN) product that can be used to determine the optimum frequency for which the maximum (narrowband) Signal-to-Noise Ratio (SNR) is obtained. After a short recall of frequency dependent attenuation and colored ambient noise in underwater channels, the AN product is used to find the upper and lower frequency limits and determine the appropriate transducer.

A. Frequency dependent attenuation

In general, the path loss $A(l,f)_{\text{dB}}$ in an underwater acoustic channel over a distance l in km for a frequency f in kHz is given by:

$$A(l,f)_{\text{dB}} = k \cdot 10\log_{10}\left(\frac{l}{l_0}\right) + l \cdot a(f) \tag{1}$$

herein, k represents the spreading factor, l_0 a reference distance and $a(f)$ the frequency dependent absorption coefficient (in dB/km). The equation for the absorption coefficient $a(f)$ is known as 'Thorp's equation' [5]:

$$a(f) = \left(\frac{0.11f^2}{1+f^2}\right) + \left(\frac{44f^2}{4100+f^2}\right) + \left(3\cdot 10^{-4}f^2\right) \tag{2}$$

B. Ambient noise

Underwater ambient noise refers to the noise that remains after excluding all easily identifiable sound sources [6]. Typically, the ambient noise in the underwater channel is caused by: turbulence, shipping, waves and thermal noise. The following approximation of the noise power spectral density $N(f)_{\text{dB}}$ as a function of frequency can be found based on [7]:

$$N(f)_{\text{dB re } \mu\text{Pa}^2\text{Hz}^{-1}} \approx 62.5 - 17\log(f) \tag{3}$$

herein, f is given in kHz. This approximation is valid within 1kHz-100kHz and accounts for moderate shipping and the Dutch average wind speed of 4.9 m/s [7][8].

C. AN product

Based on the model for path loss and the approximation of ambient noise, the narrowband SNR over a distance l in km for a frequency f in kHz assuming a transmit power P in μPa^2 (measured at l_0) is given as:

$$SNR(l,f) = \frac{P/A(l,f)}{N(f)\Delta f} \tag{4}$$

where Δf is the receiver noise bandwidth. Note that $A(l,f)$ and $N(f)$ in Equation 4 are not on a decibel scale.

Given unit power and unit receiver noise bandwidth the AN product in the factor $1/\left(A(l,f)N(f)\right)$ fully determines the frequency dependent part of the SNR. The factor $1/\left(A(l,f)N(f)\right)$ can be used to find the optimum frequency given a certain distance.

Our envisioned course-grained monitoring architecture consists of multiple underwater sensor nodes. The worst-case distance is $2\sqrt{2}$ km. Eventually multiple nodes will be used, therefore the typical communication distance will be much smaller. Figure 2 shows $1/\left(A(l,f)N(f)\right)$ for 0.5, 1 and $2\sqrt{2}$ km.

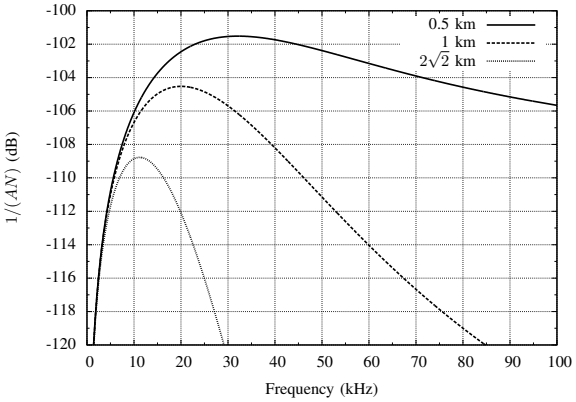

Fig. 2. $1/(AN)$ for several interesting distances.

D. Underwater acoustic transducer

Based on the assumption that it is likely to have communication distances smaller than $2\sqrt{2}$ km, the relatively low-cost HAARI WBT-30 transducer is chosen, which has an operating frequency starting at approximately 20 kHz. The WBT-30 has a flat frequency response in the 20-40 kHz region. To comply with the low-cost nature of the testbed a transducer is chosen instead of a separate projecter and hydrophone.

IV. Underwater beamforming

A purpose of the multi-channel testbed is to evaluate and test a class of spatial equalization algorithms, called (adaptive) beamforming algorithms. To collect samples, an array of upto eight transducers is used. Coherent summing of these samples results in angular directivity of the array. The directivity of the array can be steered electronically. Creation of these angular regions of directivity is called beamforming.

Characteristics of the underwater channel and the transducer affect design decisions related to beamforming. The next sections clarify the implications of these characteristics.

A. Wideband nature

The type of processing that needs to be performed for beamforming depends on the bandwidth of the received signal with respect to the carrier frequency of the signal. In underwater communication, the acoustic bandwidth of a signal is (often) in the order of its carrier frequency. This type of signals is called wideband.

A variety of techniques can be used to implement wideband beamforming, e.g. delay-sum beamformers, interpolating beamformers and Tapped Delay Line (TDL) based methods [9]. Our research will (initially) focus on TDL based beamformers because their structure offers a lot of flexibility. A TDL structure typically uses a large number of multipliers. The FPGA in our testbed offers flexibility and tens of embedded multipliers to perform this type of processing.

B. Physical limitations

The spacing between elements of an array d (in m) is generally expressed in terms of fractions of the wavelength λ (in m) of the highest frequency f_h (in Hz) in the received signal. Ideally, wideband beamformers are spaced at $d \leq \frac{1}{2}\lambda$ [9]. However, due to the relatively large diameter of the WBT-30 transducer (44 mm) the array cannot be ideally spaced. The array spacing in the testbed is shown in Figure 3.

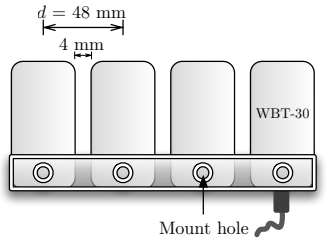

Fig. 3. Uniform Linear Array (ULA) made of four WBT-30 transducers.

A non-ideal spacing ($d > \frac{1}{2}\lambda$) leads to spatial aliasing, which can be recognized as grating lobes in the array pattern. Based on the average underwater acoustic propagation speed (1500 m/s) and the current spacing, the highest frequency without grating lobes (assuming full angular coverage) is 15.625 kHz. This a serious complication because the flat frequency response of the transducer commences at 20 kHz. Fortunately, by limiting the angular coverage of the array the impact of complete grating lobes can be reduced.

The maximum steering angle θ_0 before a complete grating lobe appears at $\theta_g = \pm 90^\circ$ follows from [10]:

$$\pi \frac{d}{\lambda}[\sin\theta_g - \sin\theta_0] = \pm n\pi \quad \text{(find first alias, use } n\text{=1)} \quad (5)$$

$$[\sin\theta_g - \sin\theta_0] = \pm\frac{\lambda}{d} \quad \text{(use } \theta_g = \pm 90^\circ\text{)} \quad (6)$$

$$\theta_0 = \sin^{-1}(\pm\frac{\lambda}{d} \pm 1) \quad (7)$$

If a signal with f_h equal to 20 kHz (λ=0.075 m) impinges at the current setup, Equation 7 has real solutions for $\theta_0 = \pm 34^\circ$. Thus, by limiting the angular coverage to $|\theta_0| < 34^\circ$ (for this scenario) complete grating lobes do not appear.

V. Hardware design

A brief description of the electronic hardware of our testbed is presented in this section. At the time of this writing Terasic has a small form factor, low-cost development kit available with a relatively large FPGA and SDRAM memory (DE0-Nano). To reduce engineering work only a simple expansion board was added to fully constitute the electronics of our testbed. Essential operations for data acquisition (amplification, filtering and sampling) are performed on the expansion board. All other operations are carried out in the digital domain on the FPGA. Figure 4 shows our expansion board stacked on top of the DE0-Nano. Upcoming sections discuss the major components of the expansion board and the digital components instantiated in the FPGA.

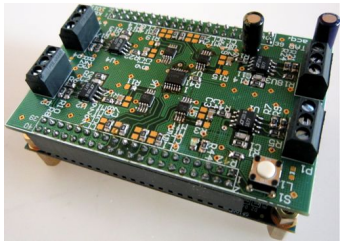

Fig. 4. Multi-channel expansion board stacked on top of the DE0-Nano.

A. Expansion board hardware

The multi-channel expansion board physically connects to four transducers. Two expansion boards can be stacked to provide upto eight channels. The WBT-30 transducer consists of piezoelectric ceramics encapsulated in a polyurethane housing. These piezoelectric ceramics generate electrical charges proportional to underwater pressure disturbances. Typically output voltages of the transducers are small and preamplifiers are used. Initially, the electronics are positioned above water and connected by long cables (20 m) to the transducers in the water. Because of these long cables charge mode amplifiers are used. A charge mode amplifier is a high gain operational amplifier with a feedback capacitor. The advantage of this configuration is that the output voltage is independent of the cable capacitance and other parasitic capacitances [11].

After amplification, first-order anti-alias filters are used before the data is synchronously sampled by 12-bit ADCs (Analog Devices AD7276). Currently the sampling speed of these converters is set to 150 kHz. However, these ADCs have a maximum sampling frequency of 3 MHz. Therefore, if necessary oversampling can be applied to improve resolution.

Data is transferred from the ADCs to the FPGA via Serial Peripheral Interface (SPI) busses. The input signal of an AD7276 is sampled at the falling edge of the active-low chip select ($\overline{\text{CS}}$). To guarantee synchronous sampling, a single $\overline{\text{CS}}$ signal is generated on the FPGA and branched to all ADCs on the expansion board(s).

B. FPGA System on Chip (SoC)

In the current testbed, raw sample data from the ADCs is immediately copied to the SDRAM (on the DE0-Nano) and stored for further processing. To support these data transfers the System on Chip (SoC) from Figure 5 is instantiated in the FPGA. To increase comprehensibility, the eight synchronization clock signals that are part of the SPI busses are not shown. The SoC uses off-the-shelf IP cores from Altera and can therefore easily be constructed.

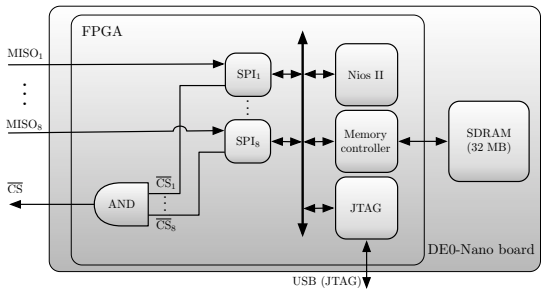

Fig. 5. SoC for (synchronous) multi-channel data acquistion and storage.

The $\overline{\text{CS}}$ output that branches to all ADCs is generated in the FPGA by combining the $\overline{\text{CS}}_{1\ldots8}$ signals using an AND gate. The SPI controllers are sequentially activated by software running on the Nios II processor. After activation, SPI_1 assigns $\overline{\text{CS}}_1$ a logic low, which results in a logic low $\overline{\text{CS}}$ output. The falling edge of this $\overline{\text{CS}}$ output initiates sampling of all ADCs. Due to the sequential activation of the SPI controllers and overlap of the corresponding data transfers, $\overline{\text{CS}}$ stays low until all sample data from all ADCs is read .

Raw data is copied to the SDRAM until the 32 MB memory limit is reached. For now, JTAG over USB is used to make a local copy of the SDRAM.

VI. Experimental results

In November 2011, underwater experiments were performed at SUASIS Underwater Systems in Kocaeli, Turkey. The main purpose of these experiments was verification of the functionality of the testbed and determination of the array pattern of the multi-channel receiver.

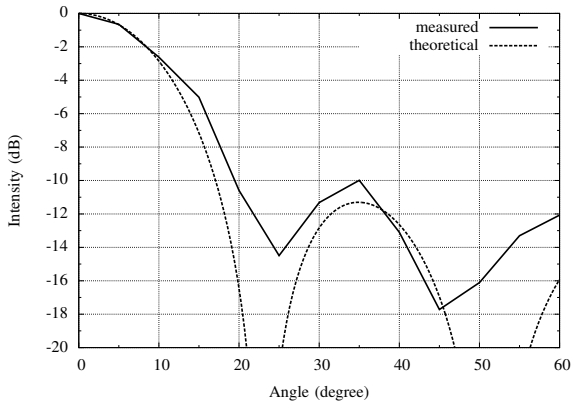

Fig. 6. Theoretical and measured four-channel array pattern.

An array of four WBT-30 transducers, as in Figure 3, was placed in the test pool and connected by long cables (20 m) to the multi-channel expansion board. Another transducer was placed in the far-field of the array and connected via a power amplifier to a signal generator producing short bursts (3 cycles) of a 20 kHz sinusoid.

For twelve different angles, starting from broadside, sample data of a burst was stored in the SDRAM of the DE0-Nano. Afterwards, for every angle, the power of the beamformer output is determined by summing the four channels and taking the mean-square of this sum.

The normalised results of our experiment and the expected theoretical array pattern are shown in Figure 6. The main lobe, side lobe and grating lobe of the measured array pattern can clearly be recognized. Furthermore, a measured side lobe level of -10dB is close to its theoretically expected level.

VII. Conclusion and future work

An underwater acoustic testbed for evaluation of novel multi-channel physical layer algorithms is presented in this work. Based on our use case and the physical limitations of the underwater channel the appropriate transducer is chosen. To provide a low-cost, small form factor and flexible solution, an off-the-shelf FPGA board and a simple expansion board is used to interface with the transducers. Currently, in the FPGA a SoC of readily available IP components is instantiated to provide (synchronous) data acquisition, storage and retrieval. In an underwater experiment the array pattern of the testbed was measured. The measured pattern resembles the exact pattern with side lobe levels close to theoretical levels.

Further work focuses on limiting the directivity of the transducers such that the array attains a large angular coverage for wideband signals. Also, methods for streaming sample data to a PC in real-time are investigated. Our main research goal is evaluation of multi-channel underwater physical layer algorithms in a practical setting.

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